3.1 CORE STACK

Storage in the B461 Core Memory is based on the principle of magnetizing a toroid core in one direction to record the storage of a binary "one" and in the opposite direction to record a "zero".

The ferro-magnetic material used in the construction of the core has a nearly rectangular hysteresis loop. Since the entire operation of storage in a core is based on the hysteresis loop, an understanding of the magnetic characteristics of a ferro-magnetic material is essential.

Ferro-Magnetism

A current flowing through a conductor will cause a magnetic field to be built up around the conductor. The magnetic lines of force are concentric and lying in a plane which is perpendicular to the plane of the conductor. See Figure 3.1-1.

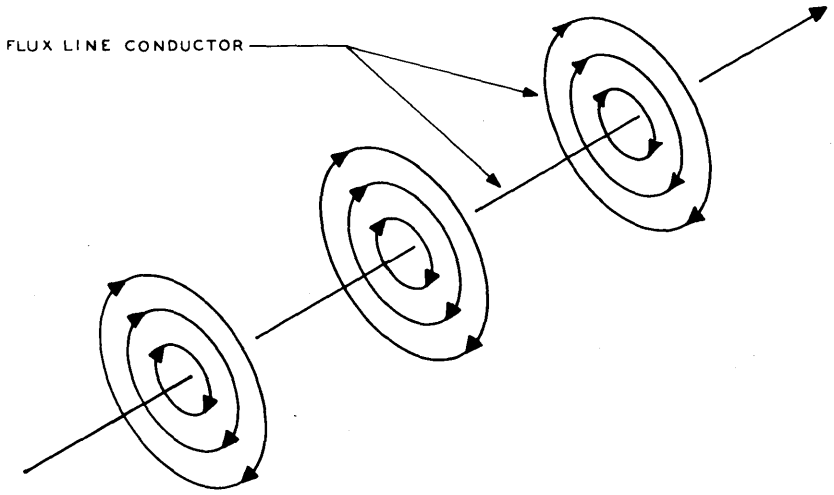


FIGURE 3.1-1
MAGNETIC FIELD

An easy method of determining the direction of the magnetic lines of force is to imagine grasping the conductor with the right hand so that the thumb points in the direction of the current flow. The fingers will then encircle the conductor in the direction of the flux lines.

When a ferro-magnetic material is introduced into the magnetic field, the field becomes distorted in the manner shown in Figure 3.1-2B. This is because the material offers a low resistance path in comparison to the space that surrounds the inductor. The magnetic field will pass through the ferro-magnetic material following the contour of the material as illustrated in Figure 3.1-2C.

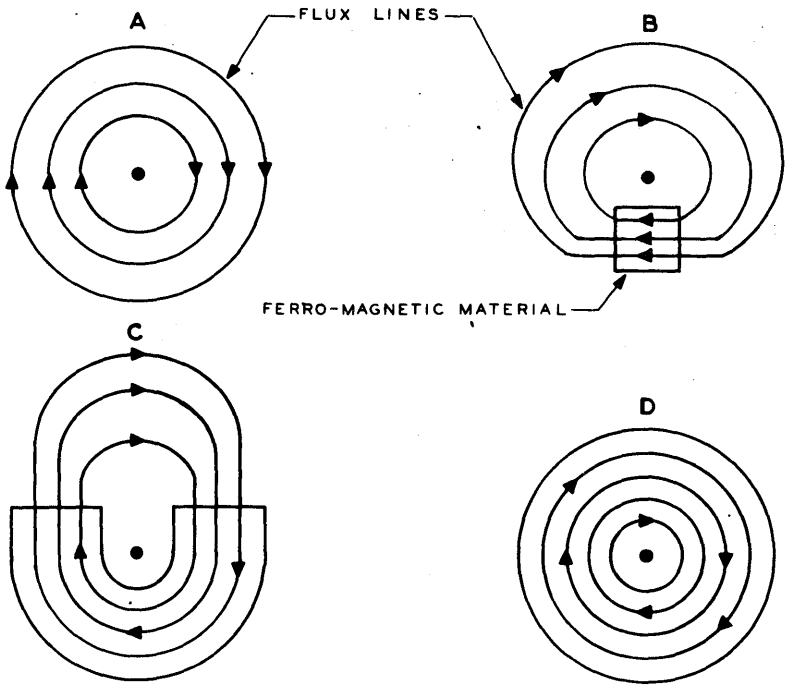


FIGURE 3.1-2
FIELD DISTORTION

When the ferro-magnetic material is fashioned into the form of a closed ring, the magnetic field set up by a magnetizing current is wholly confined to the interior of the ring. No lines of magnetic induction pass through the surface of this material to the space outside the ring. See Figure 3.1-2D. The magnetic intensity (H) in the material of the ring is equal to the product of this magnetization current and the number of turns in the magnetizing winding, divided by the mean circumference of the ring.

$H = Ni/c$

H = Magnetic Intensity
N = Number of Turns
i = Current in the Winding
c = Mean Circumference of Ring

Note that the magnetic intensity does not depend on the type of material of which the ring is formed.

The magnetic flux density (B) within the ring is the product of the magnetic intensity (H) and the permeability (μ) of the ring material.

$B = H\mu$

B = Magnetic Flux Density
H = Magnetic Intensity
μ = Permeability of the Material

The flux density (B) is not a linear function of the magnetic intensity. This is because the permeability of a material is not a constant value. Permeability depends on the type of material, the temperature

of the material, and on how much the material has been previously magnetized.

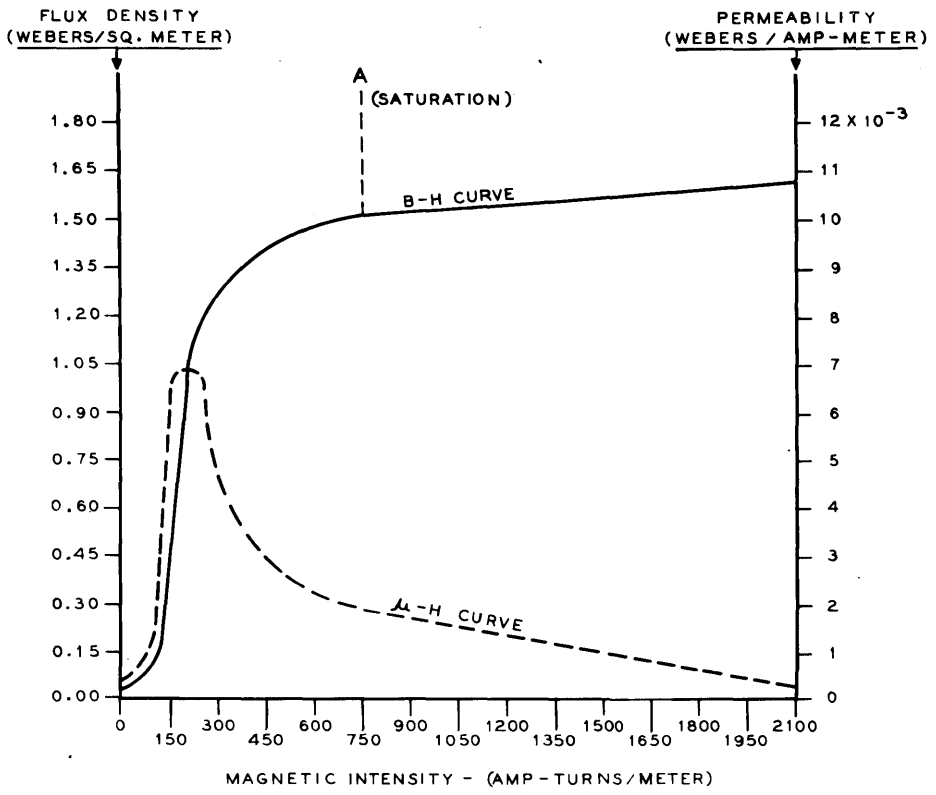


FIGURE 3.1-3
TYPICAL MAGNETIZATION CURVE

Figure 3.1-3 shows the relationship between B, H, and μ for a typical ferro-magnetic material. Notice that beyond point A, even though H is increasing, B remains almost constant. This is the magnetic saturation of the material and is due to the permeability (μ) decreasing at the rate that H is increasing.

Hysteresis

Figure 3.1-3 shows the relationship between the B and H only if the material is initially unmagnetized and H is always increasing.

The magnetization curve shown in Figure 3.1-4 expresses the relationship of B and H for the following conditions.

1. The magnetization current is increased from zero until the magnetic intensity (H) is equal to value A. The flux density (B) for this value of H is given to point B.
2. The magnetization current is increased from 0 until the value of H is D, and then decreased until the value of H is A. Now the flux density for the H value of A is given to point E.
3. The magnetization current is decreased to 0. The value of H falls from point A to 0. The flux density has a value of C

when H has returned to 0.

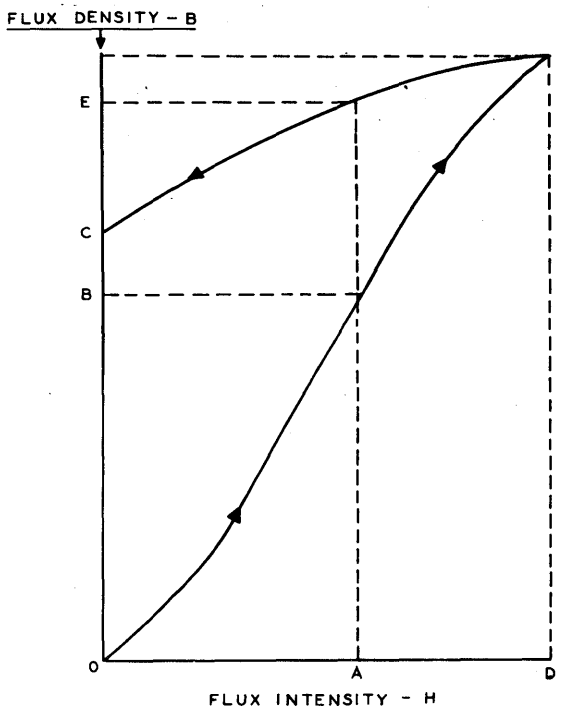


FIGURE 3.1-4
B-H CURVE

The flux density in the material is shown to depend not only on H, but also on the degree that the material has been previously magnetized. This behavior of the material, which causes the curve for a decreasing value of H to depart from the curve for an increasing value of H, is called Hysteresis.

When H is increased from 0 to some maximum value in the opposite direction, then decreased to 0; increased to the same maximum value in the opposite direction, then decreased to 0; the flux density reverses in the manner shown in Figure 3.1-5. This closed magnetization curve is called a hysteresis loop. Points C and F indicate the flux density that remains in the material after H is decreased to 0. These points are usually labeled +Br and -Br and are called the magnetic retentivity of the material. Points A and D show the amount of H required to reduce B to 0 after the material has been magnetized in the opposite direction. This is called the Coercive Force.

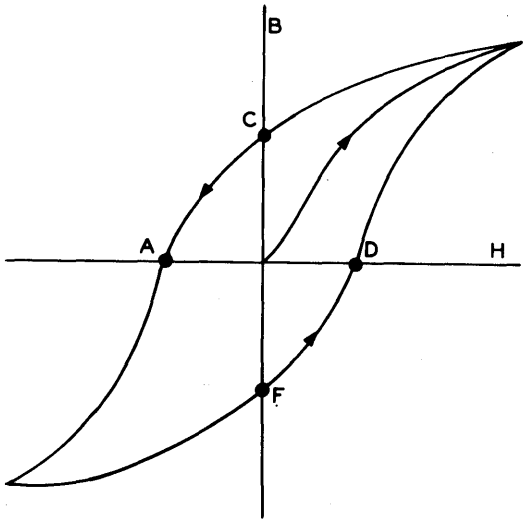


FIGURE 3.1-5
HYSTERESIS LOOP

Square Hysteresis Loop

Ferrite cores are made of special materials that will produce a hysteresis loop which is almost square. This square-loop characteristic allows the ferrite to act as a bi-stable storage element. If the ferrite core whose hysteresis loop is shown in Figure 3.1-6 is magnetized in the negative direction (-Br), and we pulse the winding with a current value of +I/2, the flux density in the core will be changed from -Br to -BrI/2. As illustrated, the change in residual flux is very small, and the core is still highly magnetized in the negative direction. However, if we pulse the winding with a current value of +I, the core will rapidly switch from -Br to +Br and will now be highly magnetized in the positive direction.

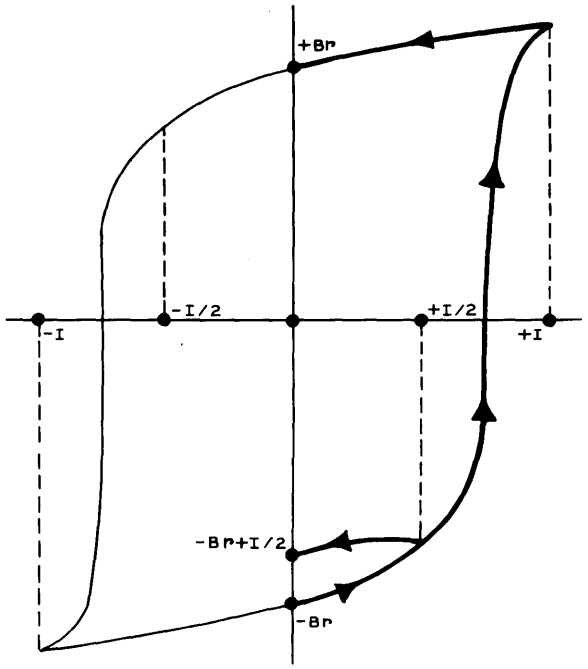


FIGURE 3.1-6
SQUARE LOOP

The square loop discriminates against small values of current in the windings. There is no appreciable change in flux density unless the winding current reaches a value which will cause an H value beyond the knee of the curve. The H current value of + or - I/2 is referred to as a half-select current; and an H current value of + or - I is referred to as a full select current.

Temperature Effect

The permeability of a ferro-magnetic material decreases as the temperature increases. The flux density (B) is the product of the flux intensity (H) and the permeability (μ); therefore, if the permeability decreases, then the shape of the material's hysteresis loop will be changed. This temperature problem demands that the core storage system be operated within a specified range of temperatures.

A core's hysteresis loop tends to become less square as the temperature of the material increases. This means that a winding current of I/2 will cause a larger change in the flux density of the core. To insure that the change in flux density will remain the same within the range of operating temperatures, the core winding drive current is decreased as the temperature is increased.

Core Windings

Each of the cores in the Memory are threaded by four wires, each wire serving as a one-turn winding. See Figure 3.1-7. In order to understand the function of the windings, assume that the core is magnetized in the negative direction and that the X and Y windings have a current

flow that tends to establish a flux density in the positive direction.

To write a binary "one" into the core, that is to switch the state of the core from -Br to +Br, both the X and Y currents must occur at the same time and have a combined value which will cause a sufficient magnetizing force to switch the polarity of the core's flux density.

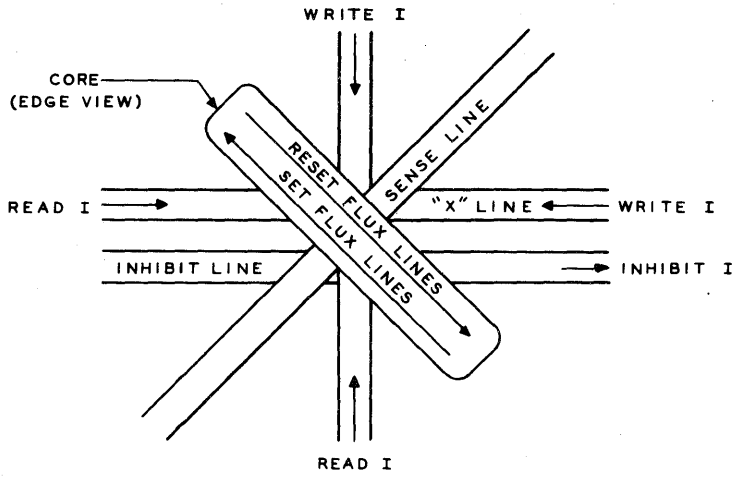


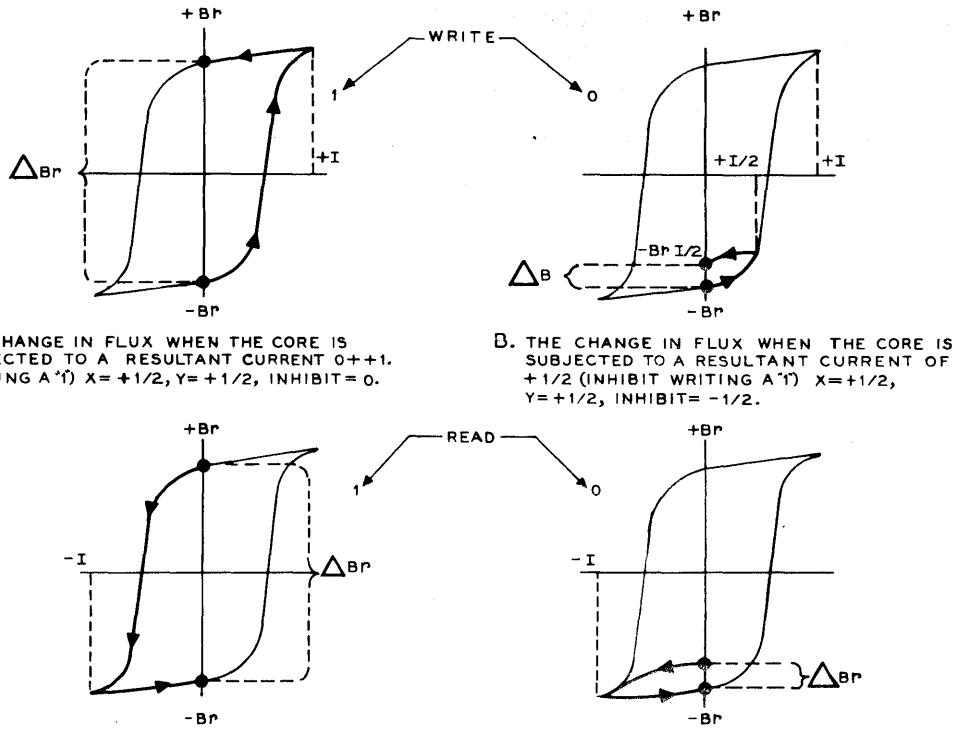
FIGURE 3.1-7
CORE WINDING

If the current flowing through each individual winding is equal to I/2, then the combined value is I. This means that the core will switch states when both currents are present; but, if only one of the currents is present, there is very little effect on the flux density of the core (See Figure 3.1-8A and B), and the core is half-selected.

As shown in Figure 3.1-7, the Inhibit winding current flow when present, will oppose that of the Write currents in the X and Y lines. When all three currents are present, the resulting effect on the core is +I/2 since the -I/2 due to the Inhibit winding current will cancel one of the Write +I/2 currents. See Figure 3.1-8B. The Inhibit-winding Driver is gated by the Information Register and is used to prevent the writing of a binary "one" into the core.

During the Read phase of a Memory cycle, the direction of current flow in the X and Y lines is reversed. If the core is in the "ones" state, coincident currents in the X and Y windings will cause the core to switch its magnetic state. This is shown in Figure 3.1-8C. This rapid change in the flux density of the core will cause a current to be induced into the Sense winding. This is a Read out of a binary "one".

If the core has been originally in the "0" state, the coincident Read currents would merely drive the core further into saturation. As shown in Figure 3.1-8D, there will be very little change in the flux density and little current induced into the Sense winding.



A. THE CHANGE IN FLUX WHEN THE CORE IS SUBJECTED TO A RESULTANT CURRENT 0++1. (WRITING A "1") X= +1/2, Y= +1/2, INHIBIT= 0.

B. THE CHANGE IN FLUX WHEN THE CORE IS SUBJECTED TO A RESULTANT CURRENT OF +1/2 (INHIBIT WRITING A "1") X=+1/2, Y= +1/2, INHIBIT= -1/2.

C. THE CHANGE IN FLUX WHEN A CORE WHICH IS STORING A "1" IS SUBJECTED TO TWO HALF-SELECT READ CURRENTS.

D. THE CHANGE IN FLUX WHEN A CORE WHICH IS STORING A "0" IS SUBJECTED TO TWO HALF-SELECT READ CURRENTS.

FIGURE 3.1-8
READ/WRITE FLUX CHANGES

A core is storing a "one" when it is magnetized in some predetermined direction. Whether it is magnetized in a positive or negative direc-

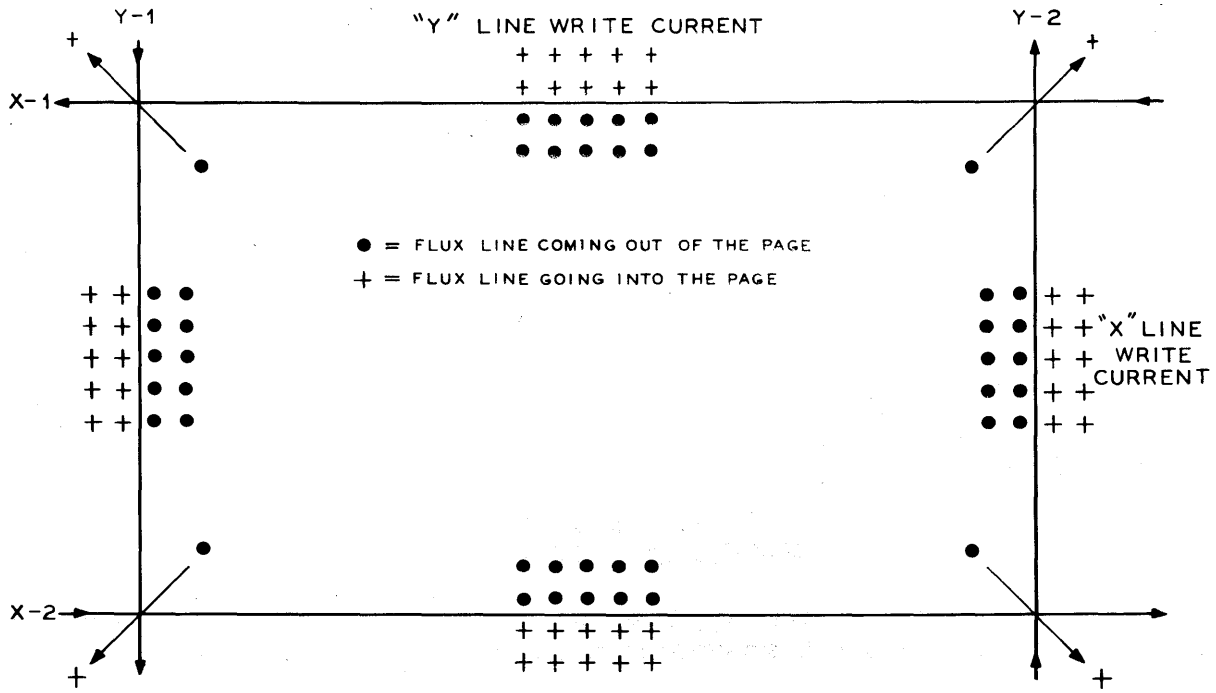


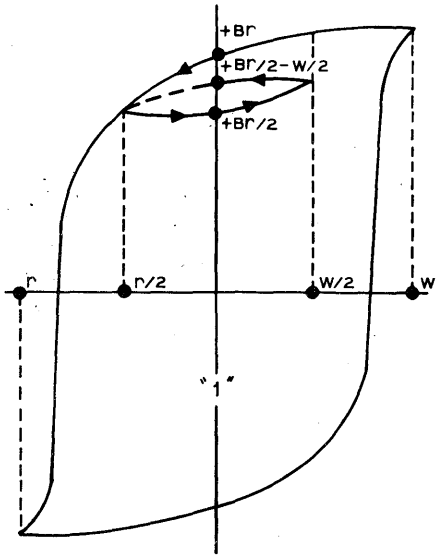
FIGURE 3.1-9
ALTERNATE LINE WRITE CURRENTS

tion will depend on the direction of the Write currents flowing in the X and Y lines. Notice in Figure 3.1-9 that due to the alternate X and Y line Write currents, two of the cores are magnetized in the positive direction and two are magnetized in the negative direction. It does not make any difference in what direction a core is magnetized, since during the Read out of the information, the X and Y line current is reversed.

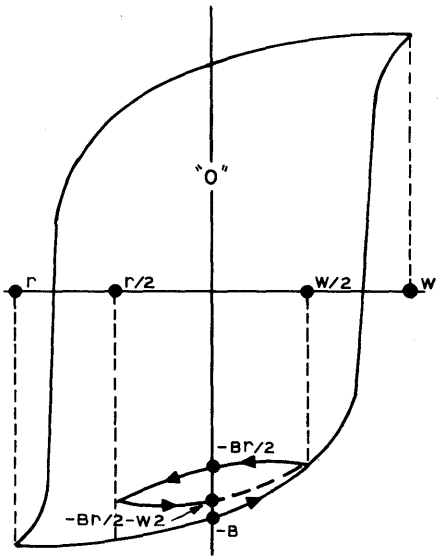
Noise

Figure 3.1-10 shows a typical hysteresis loop. Because of the curved portions of the loop, a half-select current will disturb the magnetic state of the core. A core is subjected to half-select currents each time another core on the same X or Y line is selected for a Read or Write operation.

When a core that is storing a "one" is subjected to a half-select Read current, the state of the core is changed from +B to +Br/2. Similarly, a core that is storing a "zer0" will be changed from -B to -Br/2. When the information is written back into the selected core, the half-selected cores are subjected to a half-select Write current. This half-select Write current goes from +Br/2 to +Br/2-w/2 and from -Br/2 to -Br/2-w/2 respectively.



A. THE CHANGES IN FLUX OF A CORE STORING A "1" WHEN IT IS SUBJECTED TO A HALF-SELECT READ (r/2) FOLLOWED BY A HALF-SELECT WRITE (W/2).



B. THE CHANGES IN FLUX DENSITY OF A CORE STORING A "0" WHEN IT IS SUBJECTED TO A (r/2) FOLLOWED BY A HALF-SELECT WRITE (W/2).

FIGURE 3.1-10
HALF-SELECT FLUX CHANGES

When half-select currents are applied alternately in the Read and Write directions, the core will transverse a minor hysteresis loop as shown in Figure 3.1-10.

Previously, only the selected core's contribution to the Sense line

current has been considered. However, the same Sense line passes through every core in a plane. Unavoidably, each of the cores threaded by the selected X and Y lines receives a half-select Read current which also contributes to the Sense line current. In a 64 x 64 matrix, 63 cores along the X line and 63 cores along the Y line would receive a half-select current. This accumulation of induced currents from the half-selected cores can amount to an induced current which is much greater than that due to the selected core, thereby causing a Read error if the accumulated half-select induced currents are out of phase with the induced current from the co-selected core.

To minimize this undesirable current flow, the Sense winding is arranged through the cores in a checkerboard pattern so that half of the cores will produce a negative-going pulse in the Sense line, and the other half will produce a positive pulse in the line. See Figure 3.1-11.

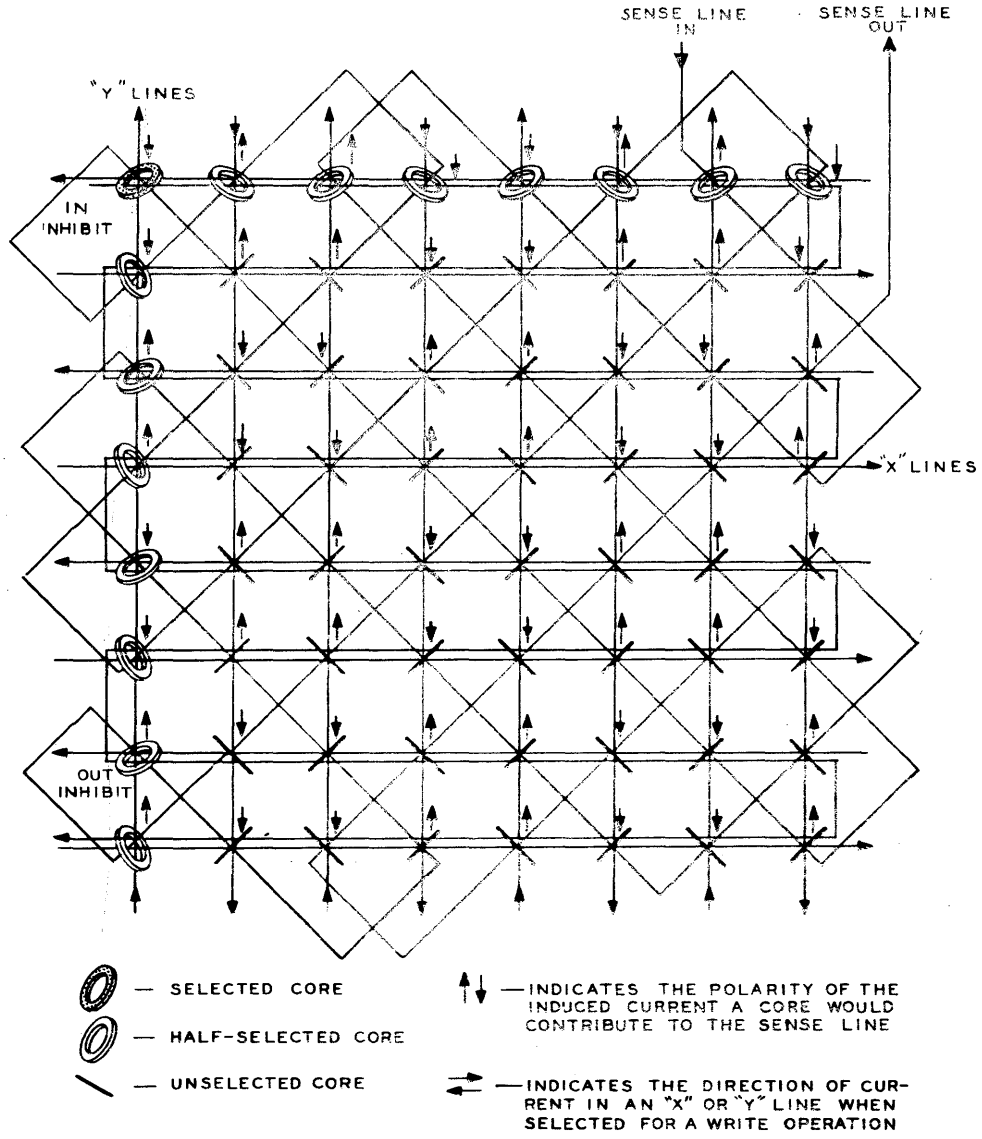


FIGURE 3.1-11
8 x 8 CORE PLANE

When all cores contain the same information (1 or 0), the positive induced current which is contributed by one half of the half-selected cores, will be cancelled by the negative induced current from the other half of the half-select cores.

In actual practice, there is not a complete cancellation of the half-select signals. This is because it is not possible to manufacture cores that all exhibit exactly the same magnetic characteristics. This is also due to the physical layout of the Sense line. There will be two half-select cores left unopposed.

There are 63 half-select cores on each selected line. Of these cores, 32 are contributing a pulse of one polarity and 31 are contributing a pulse of the opposite polarity. This leaves one core on each line that is unopposed. Both of these cores are contributing a pulse that is out of phase with the pulse from the selected core. The resultant signal in the Sense line is the contribution of the selected core, minus the two unopposed half-select cores contribution, plus or minus the difference noise from the remaining half-selected cores.

$R = S - 2hs \pm dn$

R = Resultant Signal

S = Signal due to the selected core

hs = Signal due to the two unopposed half-selected cores

dn = The difference noise signal due to 31 half-selected cores not completely cancelling the other 31 half-selected cores

The worst pattern of storage information would be to have all the cores producing positive-going currents in one state and the other half in the opposite state. In this case, the term dn takes on a maximum value. The reason for this is that at the time that they are both subjected to a half-select Read current, the change in flux density of a core storing a "one" is not equal to the change in flux density of a core storing a "zero".

The cores storing zeros have been subjected to one more half-select current than the cores storing ones. This additional half-select current was applied at the time that the cores storing "ones" were fully selected. Because of this additional half-select current, the residual flux density of a core storing a "one" is not equal to the residual flux density of a core storing a "zero".

One of the factors that determines the permeability of a material is the degree that it has been previously magnetized. Since a core storing a "one" is not magnetized to the same degree as a core storing a "zero", the changes in flux density as the result of the half-select Read will not be the same.

Stack Construction

All the cores for the Memory are mounted into a unit referred to as the Core Stack. The Core Stack is sub-divided into planes. Each plane corresponds to one bit of information in each of the words. As there are 48 Information bits and one Parity bit in a word, the stack consists of 49 planes, plus one blank plane for a total of 50 planes. Each plane has its own Sense and Inhibit windings to make a total of 49 Sense and 49 Inhibit windings, one for each bit in a word.

Every time a Memory cycle is initiated, one core in each plane is selected to access all 49 bits of a word. This is accomplished by the X and Y lines. There are 4096 cores in each plane arranged in a 64 x 64 Matrix, or, each plane is accessed by 64 X lines and 64 Y lines. Any one X line will intersect any one Y line only once in each plane; (refer to Figure 3.1-12), but the X and Y lines are wired to all planes in the Stack. By driving current into one X line and one Y line, both currents being in coincidence, one core will be selected in each plane; a total of 49 cores for an entire word.

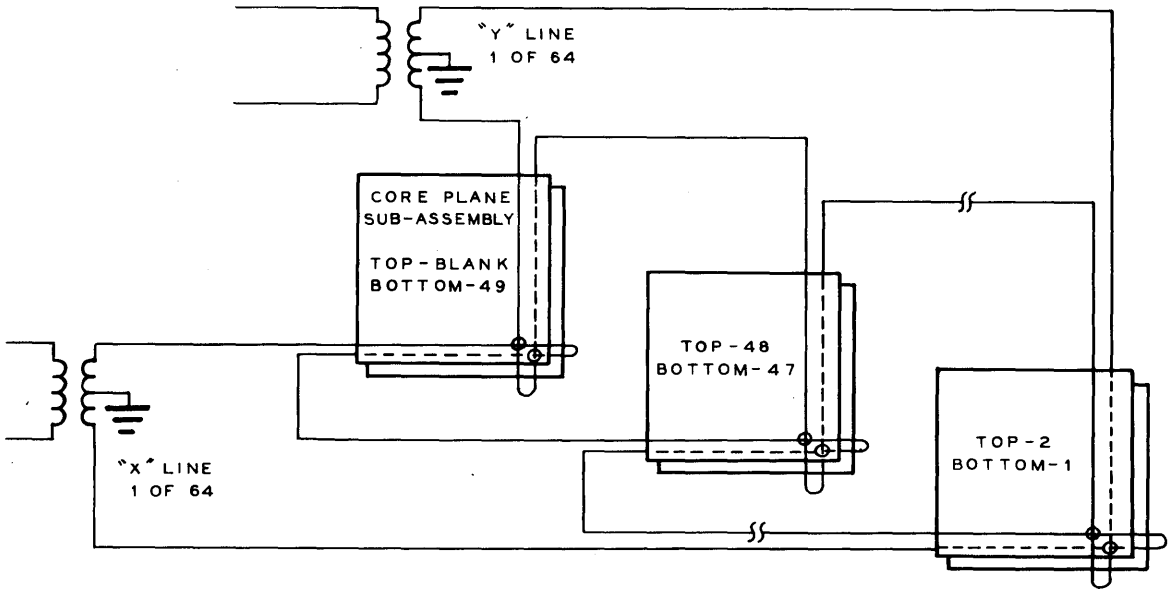


FIGURE 3.1-12
X - Y LINE INTERSECTION

Each X and Y line originates from one side of the secondary of a transformer, loops through the entire stack, and returns to the other side of the same transformer secondary. See Figure 3.1-12. There is one transformer for each of the X lines and each of the Y lines. By driving current through the transformer primary in one direction for a Read, and the other direction for a write, the current in the secondary will also change direction. This in turn will drive current in the X or Y line in one of two directions, depending upon Read or Write.

For a detailed description of the transformer operation, refer to Section 3.2 of this manual.

3.2 ADDRESSING

Addressing is the function of selecting a particular "X" line and "Y" line to access one of the 4096 words in the Core Stack. Figure 3.2-1 is a diagram of the Logical Units of the Core Memory.

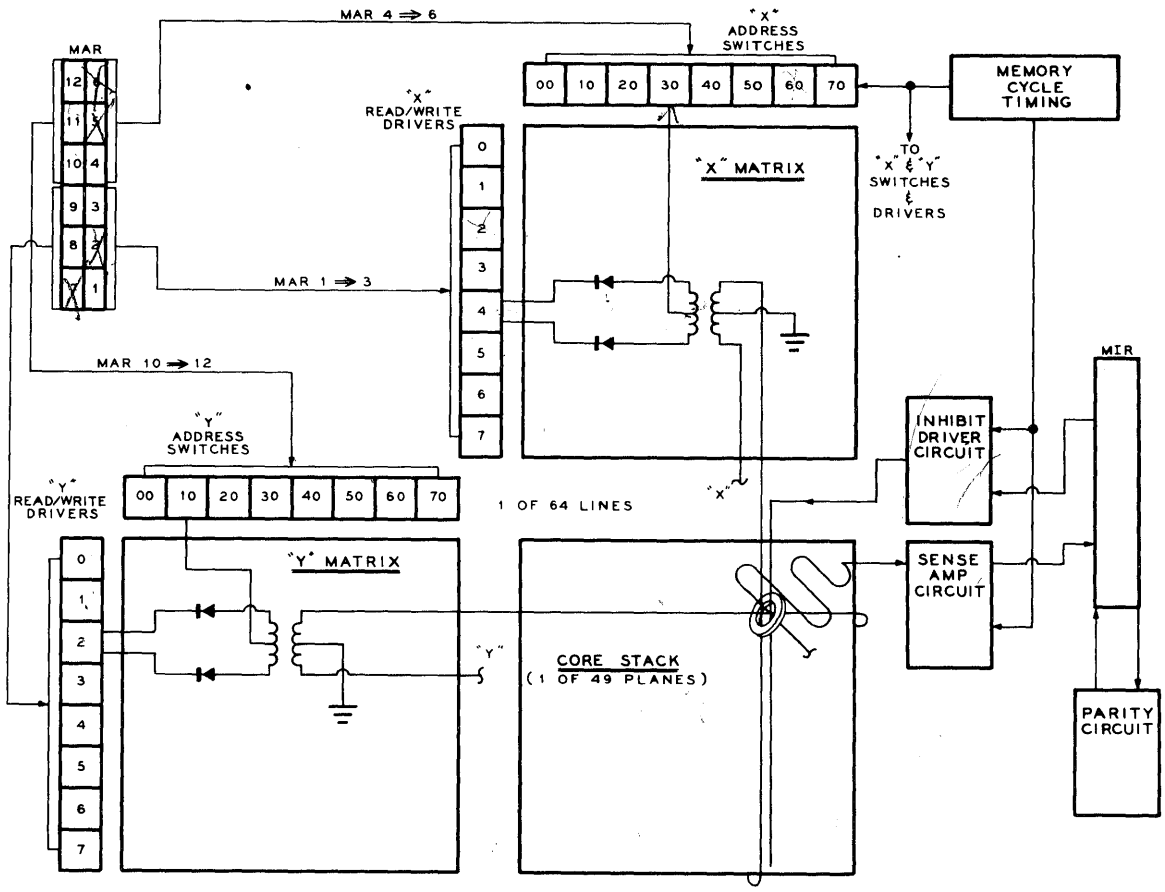


FIGURE 3.2-1
LOGICAL UNITS

The Addressing portion of this diagram consists of the Address Register (MAR), "X" and "Y" switches, "X" and "Y" Read/Write drivers, the "X" and "Y" Transformer Matrices, and the "X" and "Y" lines to the Stack. The Memory Timing circuits go to the "X" and "Y" Address switches and Read/Write drivers as an enabling level to indicate when they are turned ON.

"X" and "Y" line selection is under control of the Address Register which can be of any octal value of 0000 thru 7777. For decoding purposes, the Address Register can be divided into four sections. Refer to Figure 3.2-2.

The six Low order bits of the Address Register (bits 1 thru 6) are used to select the "X" line to the Stack. The six High order bits of

the Address Register (bits 7 thru 12) are used to select the "Y" line to the Stack. The six bits of "X" or "Y" are in turn separated into two groups, Tens and Units, which are also referred to as High (Tens) and Low (Units). The following is a description of the Address Register usage.

MAR 1 thru 3 Units X (Low-X)
Selects "X" Read/Write drivers.

MAR 4 thru 6 Tens X (High-X)
Selects "X" Address switches.

MAR 7 thru 9 Units Y (Low-Y)
Selects "Y" Read/Write drivers.

MAR 10 thru 12 Tens Y (High-Y)
Selects "Y" Address switches.

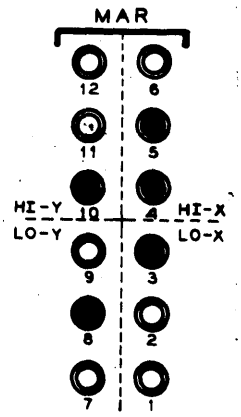


FIGURE 3.2-2
MEMORY ADDRESS REGISTER

Figure 3.2-1 shows the MAR usage with MAR 1 thru 3 gating the "X" Read/Write drivers to select one of the seven drivers (X0 thru X7). MAR 4 thru 6 gates the "X" Address Switches to select one of the seven switches (X00 thru X70). Likewise, the six High order bits of MAR are used to select one "Y" Read/Write driver (MAR 7 thru 9) and one "Y" Address switch (MAR 10 thru 12).

"X" & "Y" Numbering

Core Addresses are comprised of four octal digits of which the "Y" is always the two High order digits, and the "X" is always the two Low order digits. For example: If the Address Register contained the configuration of bits as indicated by the black circles shown in Figure 3.2-2, then the Stack location being accessed is Address 1234. The six High order bits of the Address Register contain a value of Tens 1 and Units 2 for an octal value of 12. This will result in the "Y"-12 line of the Stack being selected.

The six Low order bits of the Address Register contain a Tens 3 and a Units 4 for an octal value of 34. This will result in the X-34 line in the Stack being selected. The Core Address 1234 is located where the "X" and "Y" lines intersect each other in the Stack, once in each Core Plane.

The "X" and "Y" lines are numbered to correspond to the values available in the Address Register. The possible combinations for the "X" or "Y" are 00 thru 77 in the Address Register. The "X" and "Y" lines are also numbered 00 thru 77, with the number of the particular "X" or "Y" line selected corresponding to the configuration in the Address Register.

Matrix Transformers

Each "X" or "Y" line originates at the secondary of a Transformer in the "X" or "Y" Transformer Matrix. Refer to Figure 3.2-1. There are 64 "X" and 64 "Y" Transformers (one for each "X" line and one for each "Y" line) numbered to correspond to the "X" and "Y" lines 00 thru 77.

The Matrix Transformers are mounted on four Transformer boards located at each end of the Core Stack. See Figure 3.2-3.

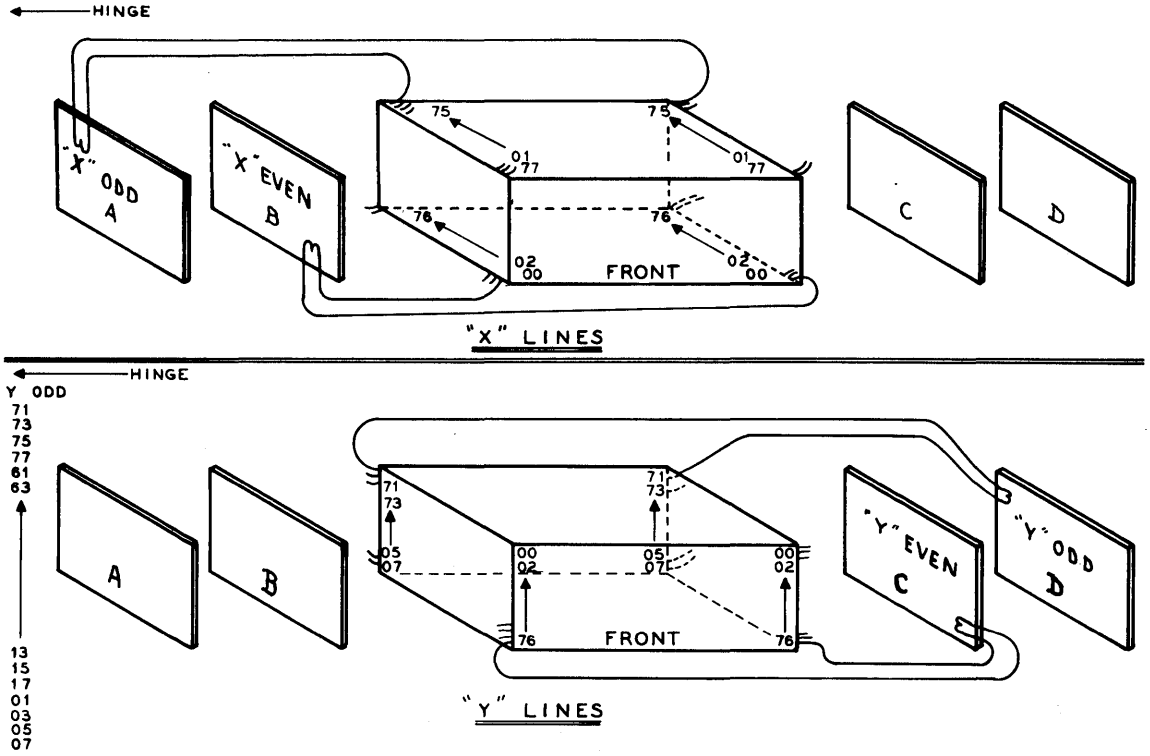


FIGURE 3.2-3
TRANSFORMER BOARD LOCATION

The boards labeled A and B are for the "X" lines, and boards C and D are for the "Y" lines. The two Transformer boards for either the "X" or "Y" contain 32 Transformers on each board. The odd numbered Transformers are on the Odd "X" board A and Odd "Y" board D. The even numbered Transformers are on the Even "X" board B and Even "Y" board C. In both cases ("X" or "Y"), the Odd numbered boards are located furthest from the Stack.

The Transformers on each of the Transformer boards is arranged in a 4 x 8 Matrix with two of the boards combining to form an 8 x 8 Matrix for either the "X" or "Y" line selection. See Figure 3.2-4.

The secondary of each Transformer has its center tap grounded for elimination of noise, and a resistor across the secondary to dampen the signal going into an inductive load. They are grounded through their respective Address Switch Package (SWAD) via the ground lines labeled X00G thru X70G.

The primaries of the Matrix Transformers are connected to the outputs of the Address switches and the Read/Write drivers (DRAC). Each of the SWADs goes to the primary center taps via the lines labeled X00S thru X70S. Each side of the Transformer primary goes to the Read/ Write drivers, one side for the Read (XR0D thru XR7D), and the other side for the Write (XW0D thru XW7D).

Each side of the Transformer primary of each Transformer has a diode (also mounted on the Transformer boards) for isolation purposes. These diodes prevent current from flowing in any Transformer except the Transformer selected by the SWADs and DRACs.

Memory Address Switch (SWAD)

Each SWAD has five inputs, four Address inputs and one Timing input. Refer to Figure 3.2-4. The Address inputs consist of one input from A05F and A06F, and both outputs from A04F of the Address Register. A05F and A06F select which of the SWAD packages will be used, and A04F determines which of the two switch circuits within each of the packages will be used.

X00S = A04F/ · A05F/ · A06F/ · MS1M

X10S = A04F · A05F/ · A06F/ · MS1M

In the X00 SWAD, the Address inputs are A04F, A04F/, A05F/ and A06F/. The above logic indicates that if A04F/ is TRUE, then the switch output X00S will be enabled. If A04F is TRUE, indicated in Odd Tens, then the switch output X10S will be enabled.

The Timing input of MS1M is TRUE during the entire Memory operation, Read and Write portion, to enable the selected switch for the entire Memory operation.

When a SWAD output is enabled, it places +30V at the center tap of each of its Transformers. When the SWAD is NOT enabled, the package output is an open circuit. For a detailed description of the SWAD package, refer to Section 3.7.

Read/Write Drivers (DRAC)

There are 16 DRAC packages in the B461 Core Memory, eight "X" drivers and eight "Y" drivers. Each of the Driver packages has five inputs, three Address inputs and two Timing inputs. The "X" Read/Write Drivers in Figure 3.2-4 are gated by the three Low order bits of the Address Register (A01F, A02F and A03F). The configuration of these bits determines which DRAC package is selected. For example: If the Units "X" position of the Address Register contained a value of 2, then the Address levels A01F/ and A03F/ will be TRUE to select the DRAC with the XR2D and XW2D outputs.

XR2D = A01F/ · A02F · A03F/ · MR2M

XW2D = A01F/ · A02F · A03F/ · MW2M