

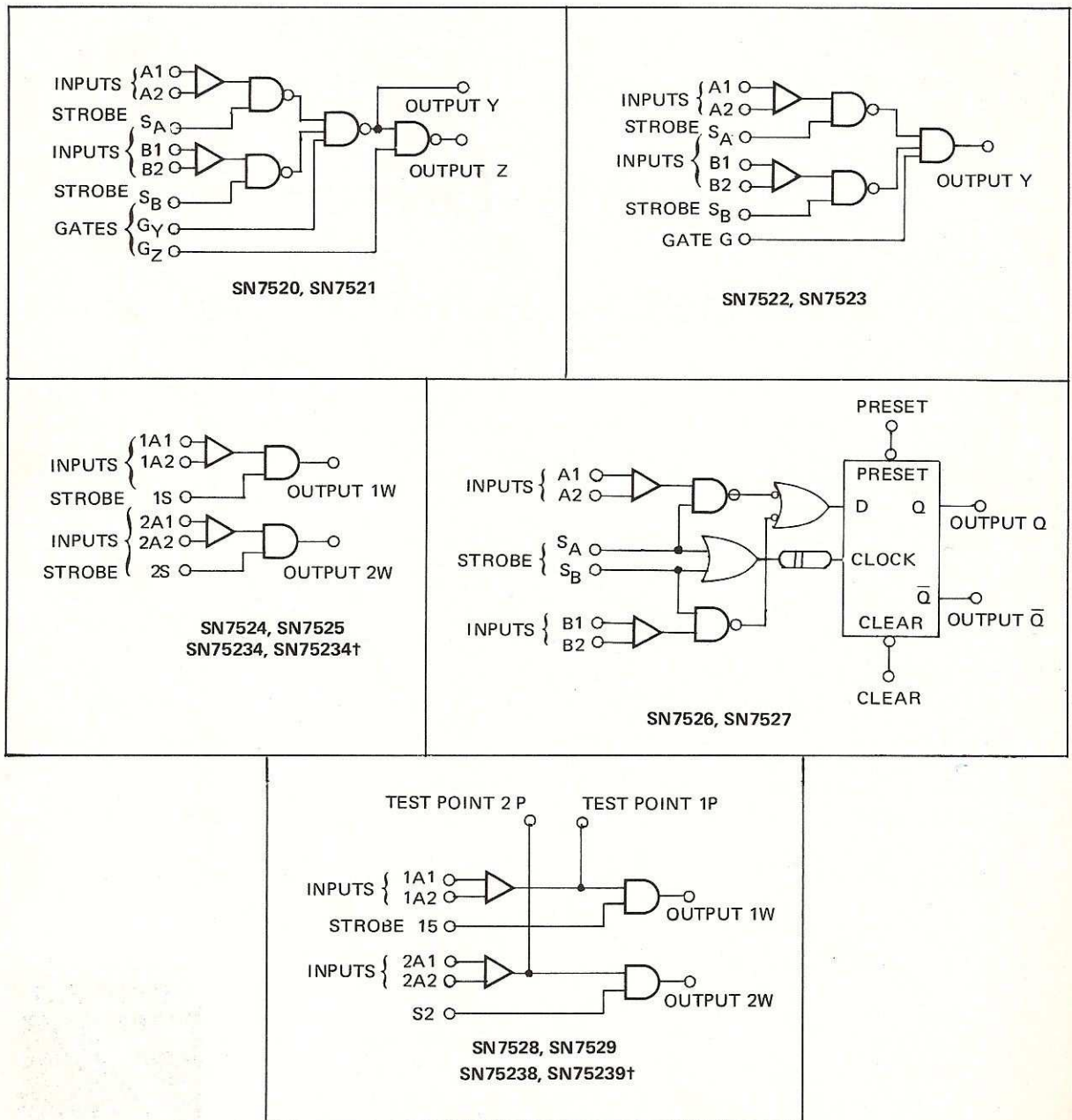
Memory Drivers and Sense Amplifiers



SENSE AMPLIFIERS

TYPE	SN7520, SN7521	SN7522, SN7523	SN7524, SN7525 SN75234, SN75235†	SN7526, SN7527	SN7528, SN7529 SN75238, SN75239†
Features	* Provide Memory Data Register * Complementary Outputs	* Open-Collector Output Stage * High Fan Out	* Dual Sense Channels * Independent Strobes	* Complete Memory Data Function * Effective Strobe Width of Less than 10 ns	* Test Points for Strobe Timing Adjustment * Dual Sense Channels
No. of Pins	16	16	16	N	N
Applications	Large Memories	Large Memories	General Purpose Sense Amplifiers	High Performance Sense Amplifiers	General Purpose Sense Amplifiers

BLOCK DIAGRAMS



† Types SN75234, SN75235, SN75238, and SN75239 are identical to types SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output.

MEMORY DRIVERS

TYPE	SN75324 DRIVER WITH DECODE INPUTS	SN75325 DRIVER WITH DECODE INPUT
Features	<ul style="list-style-type: none"> * Four 400-mA Transistors * TTL-Compatible Inputs * Internal Decoding and Timing Gates * Single 14 V Supply 	<ul style="list-style-type: none"> * Four 600-mA Transistors * TTL-Compatible Inputs * Internal Decoding * 5 V Supply * 24 V Output Capability
Application	* Core Memories	<ul style="list-style-type: none"> * Core Memories * Plated-Wire Memories * Hammer Driver
No. of Pins	14	16

General Considerations

Sense Amplifiers

1. Power supplies should be regulated to $\pm 5\%$ or better and should have low-inductance by-pass capacitors as physically close as possible to each sense amplifier.
2. The data input/sense line should be terminated in its Characteristic Impedance and should be as short as possible. It should be kept as far away as possible from any lines carrying high level logic signals.
3. If the input signal from the memory does not have a high enough slew-rate the output of the sense amplifier may oscillate.
4. Strobe inputs to unused channels should be grounded, failure to do this may cause a malfunction in the used channel, due to unused channels switching on noise signals. Care should be taken in the timing of the strobe signals, allowing for the propagation delay through the device.

Memory Drivers

5. Circuit-board mounting of memory drivers should be carefully considered, with special regard for heat sinking, signal transmission, and noise. Furthermore, because memory drive and logic currents may share the same electrical ground in a direct-coupled system, special care is necessary to minimise ground noise. In the case of the SN75324 this is especially so because the logic and driver are monolithic.

Application of Series SN7520 Sense Amplifiers

General

Series 7520 sense amplifiers are designed specifically for use in coincident current memories organized in the 3D (three dimensional) and 2 1/2D configurations. In these applications, memory output information is transformed from low-level (10-60mV)

bipolar pulses into high-level digital logic levels. Memory information is categorized as representing stored logical "0" or "1" information on the basis of signal amplitude and position in time, regardless of signal polarity.

In these memories, it is common practice to limit the number of cores on each sense line to about 4K. Large core planes are sectored into small sub-planes of approximately 4K bits as shown in Figure 1 with separate sense lines for each sub-plane.

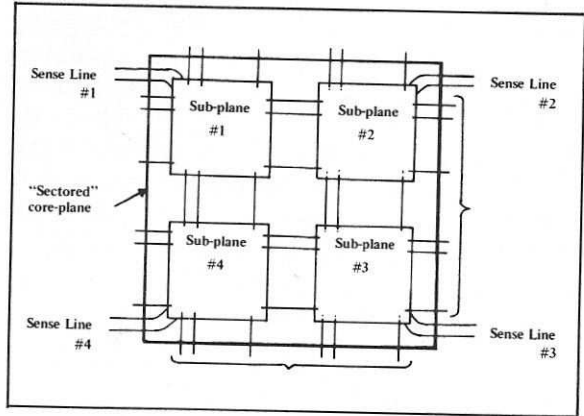


Figure 1.

Discrete sense amplifier designs usually utilize reactive components such as inductors and capacitors to eliminate problems due to d.c. bias level drift. Integrated sense amplifiers usually use capacitive coupling for the same reason. Or, a d.c. comparator is used with a complicated input resistor network to obtain threshold action. These methods, however, introduce additional problems:

- (1) Reactive coupling usually results in threshold shift with increased repetition rates
- (2) Reactive coupling results in excessive overload recovery time
- (3) Input resistor networks degrade the common-mode rejection of the design and require expensive, precision components.
- (4) Redundant circuitry results in excessive power
- (5) High package or component count uses excessive board area, excessive interconnections, and reduces reliability.

Series 7520 devices incorporate the necessary circuitry to perform sensing for two sense lines without the above undesirable characteristics. This performance results from the unique Series 7520 "matched-amplifier" circuit design which utilizes the inherent matching and tracking characteristics of integrated circuit components. This design permits an all d.c.-coupled circuit without the associated d.c. drift problems. The result is close matching of all the sense channels for maximum system performance.

This results in a much higher signal-to-noise ratio than can be obtained with a larger number of cores on a sense line. Also, delays from various bit locations are more uniform, allowing more precise strobing.

The following sections show some of the applications for which the Series 7520 devices were designed.

SN7520/21N Applications

The SN7520/21N Sense Amplifier is a complete monolithic sub-system incorporating all the necessary threshold, strobing, and logic functions for sensing, gating, and storing information from up to 8K cores in the memory. The output circuit of the SN7520/21N is composed of two cascaded NAND gates. External inputs are available as logic inputs to each of the gates. The gates may be connected in a cross-coupled gate latch configuration, (\bar{Q} output to Gate Q input), as shown in Figure 2, thus enabling the output circuit to function as part of the Memory Data Register (MDR). Information extracted from the sense lines during the strobe enable pulse can be retained as long as desirable for use with the computer logic section. A negative going pulse applied to the Gate Q input clears the latch prior to the next strobe enable pulse.

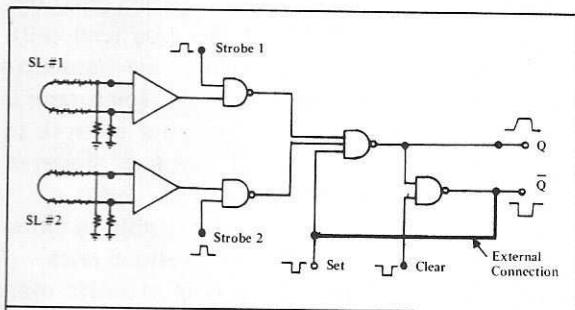


Figure 2.

In those applications where output pulse stretching is desirable, the gates in the output section of the SN7520/21N may be capacitively coupled, as shown in Figure 3.

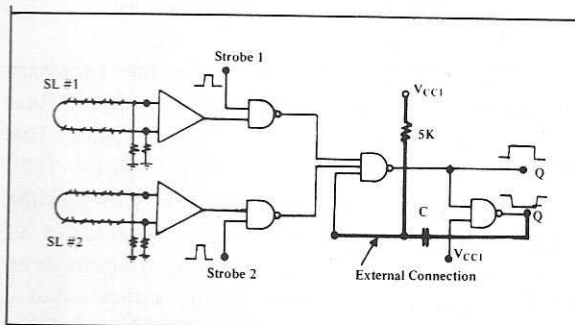


Figure 3.

In some applications, neither the latch configuration or output pulse stretching may be required. In these applications, the gates in the output of the SN7520/21N may be used as a part of the logic unit, supplying complementary output logic levels with standard TTL fan-out capability.

In applications that do not utilize the external gate inputs (Gate Q and Gate \bar{Q} inputs) these terminals should be tied to the positive supply (V_{CC1}) to prevent capacity coupling at these terminals from affecting delay times. Strobe inputs should be treated similarly.

In some memory applications, more than 8K words may require sensing. The dual sense input function of the SN7520/21N may be expanded to four sense inputs by the addition of a dual-input SN7522/23N sense amplifier. (The 4K bits per sense line referred to in this report is a good rule of thumb, resulting in a good signal-to-noise ratio, thereby permitting good system performance. However, in especially clean (low noise) memory designs, it may be possible to have 8K or more bits per sense line). Details in using the SN7522/23N as an expander will be considered in detail in the next section.

SN7522/23N Applications

The SN7522/23N has as its output circuit an open-collector gate that may be connected to perform the Wire-OR logic function, thus permitting a level of logic to be implemented without additional gate delays. Each SN7522/23N also has an internal load resistor of value approximately $2K\Omega$. One end of the resistor is internally connected to the positive supply (V_{CC1}) while the remaining end is brought out through a separate pin. The resistor may be used as a collector pull-up resistor in those applications where its value is acceptable. Load resistors from several SN7522/23N packages may be connected in parallel for lower impedance.

The output gate of the SN7522/23N is designed to have a very high sink current capability. Although the specifications indicate a limit of 0.4 volts maximum output logical 0 voltage level while sinking 16 milliamps, this limit is conservative as indicated by the typical curve for this parameter, shown in the data sheet.

The high output sink current capability increases the versatility of the SN7522/23N in a variety of applications. Several SN7522/23Ns may be Wire-OR connected in order to provide the necessary number of sense-inputs for large memory applications. Also, the output may be Wire-OR connected with other sense amplifiers such as the SN7520/21N. In this application, shown in Figure 4, the output of a single SN7520/21N is connected as a latch to function as

part of the Memory Data Register. As many SN7522/23Ns as necessary are connected to provide additional sense inputs to the MDR. The Gate Input terminal of each of the SN7522/23Ns, in this application, serves as an external set input for the MDR, allowing information to be entered into the MDR from the logic section. The Gate \bar{Q} input of the

SN7520/21N serves as the Clear input for the latch in this application.

The output of the SN7522&23N may also be Wire-OR connected with logic gates that feature this capability. This includes most diode-transistor logic (DTL) gates and the Series 74, SN7401N, quad two-input positive NAND gate.

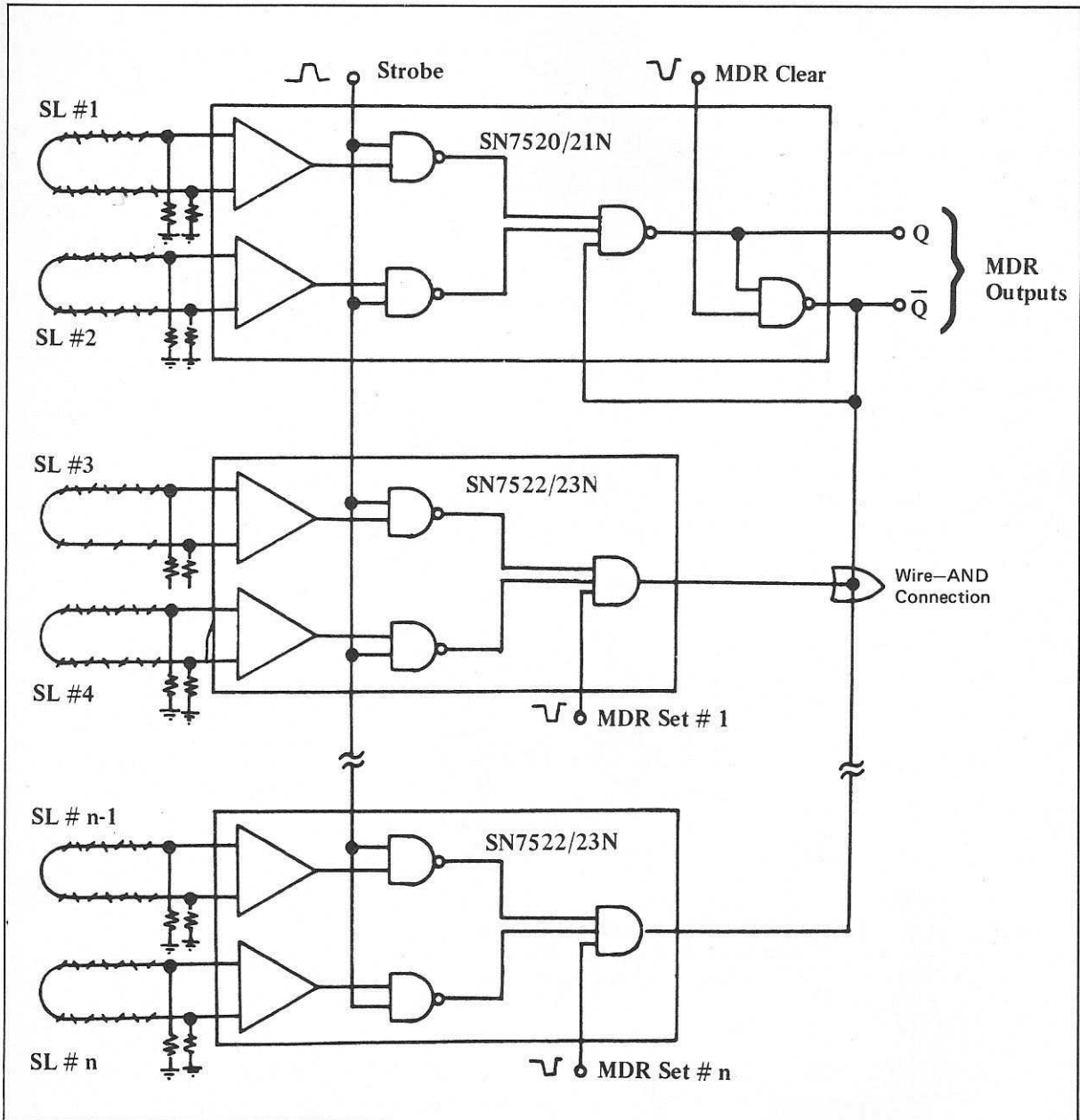


Figure 4. USE OF THE SN7522/23N AS AN INPUT EXPANDER FOR THE SN7520/21N

In applications in which more than a simple latch is desirable for the MDR, several options may be considered. For example, the SN7474N dual D-type edge-triggered flip-flop is an excellent device for use with the SN7522/23N. The SN7474N features direct clear and preset inputs and complementary outputs.

Input at the D input is transferred to the Q output of the SN7474N on the positive edge of the clock pulse. The outputs of one or more SN7522/23Ns can be connected as shown in Figure 5 to provide inputs to the SN7474N.

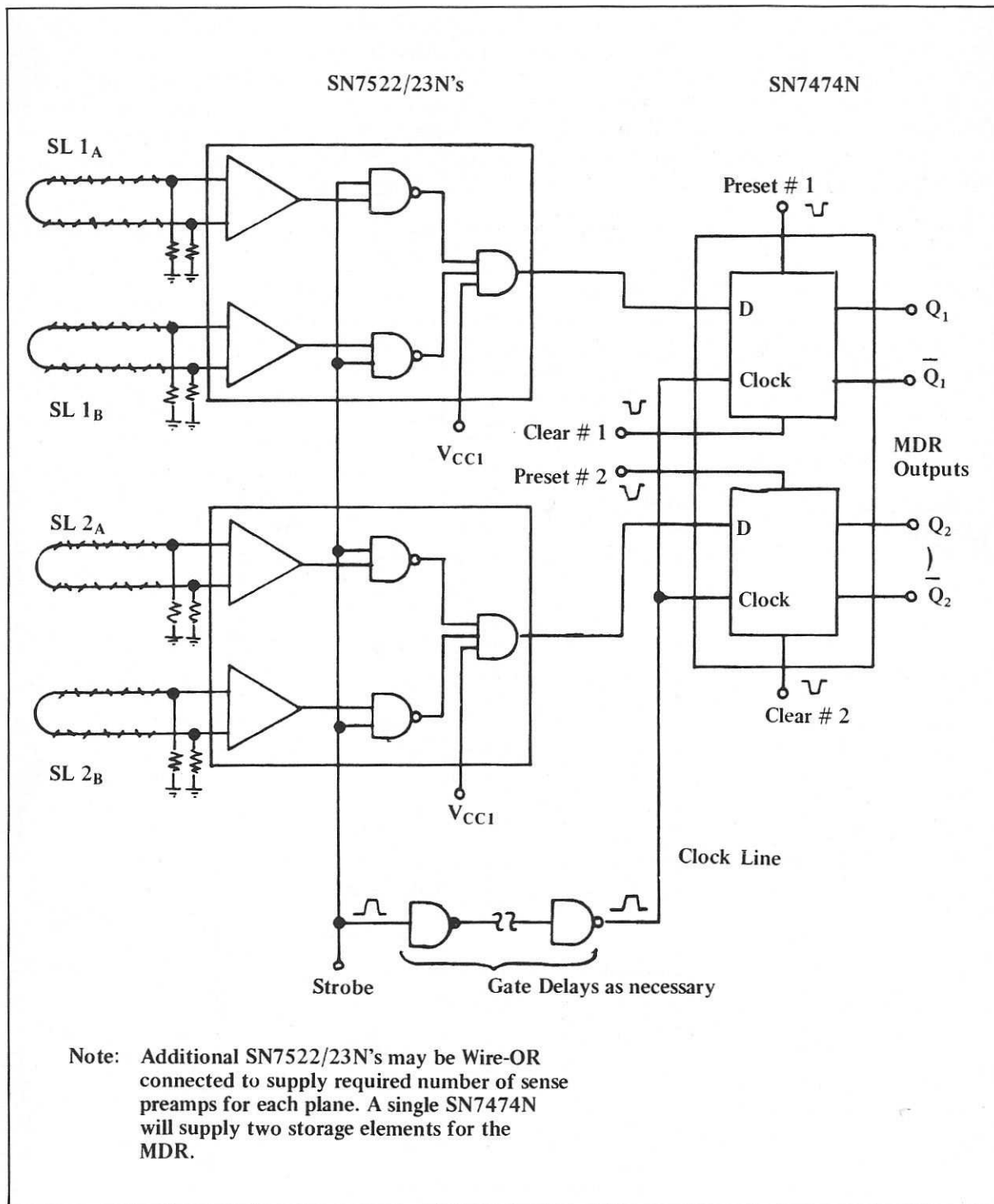


Figure 5. USE OF SN7522/23N WITH SN7474N AS MEMORY DATA REGISTER

A single SN7474N can provide two storage elements for the MDR. If a separate clock pulse is undesirable, the clocking function can be provided by the strobe input. Proper delay must be provided to ensure that the D input is set-up at clock time. In this

application, an inversion occurs from the sense inputs to the flip-flop output. Logical 1 sense inputs ($> V_T$) will enter logical 0 levels into the Q output. This is due to the negative-going output from the SN7522/23N.

SN7524/25N Applications

The SN7524/25N sense amplifier is, in actuality, two separate sense amplifiers in a single package. Separate inputs, strobes, and outputs permit a single SN7524/25N package to service two separate bit-planes in a memory as shown in Figure 6. Since the outputs of the SN7524/25N cannot be Wire-OR connected because of its normally-low output level, the SN7524/25N finds its widest application in small memories of up to about 4K words. In this application, the SN7524/25N will result in one-half the package count normally required. It also increases reliability and reduces the memory size by fewer interconnections, less board area, and less power than other sensing schemes.

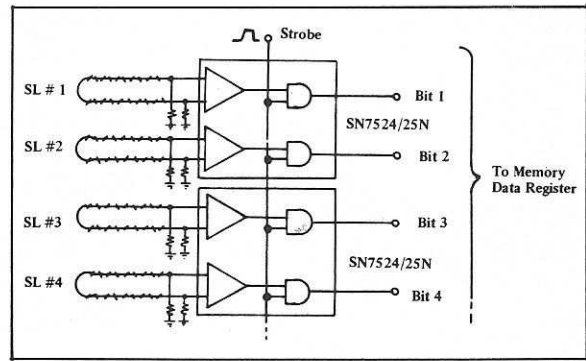


Figure 6.

A useful application of the SN7524/25N is in conjunction with the SN7475N quadruple bistable latch, as shown in Figure 7.

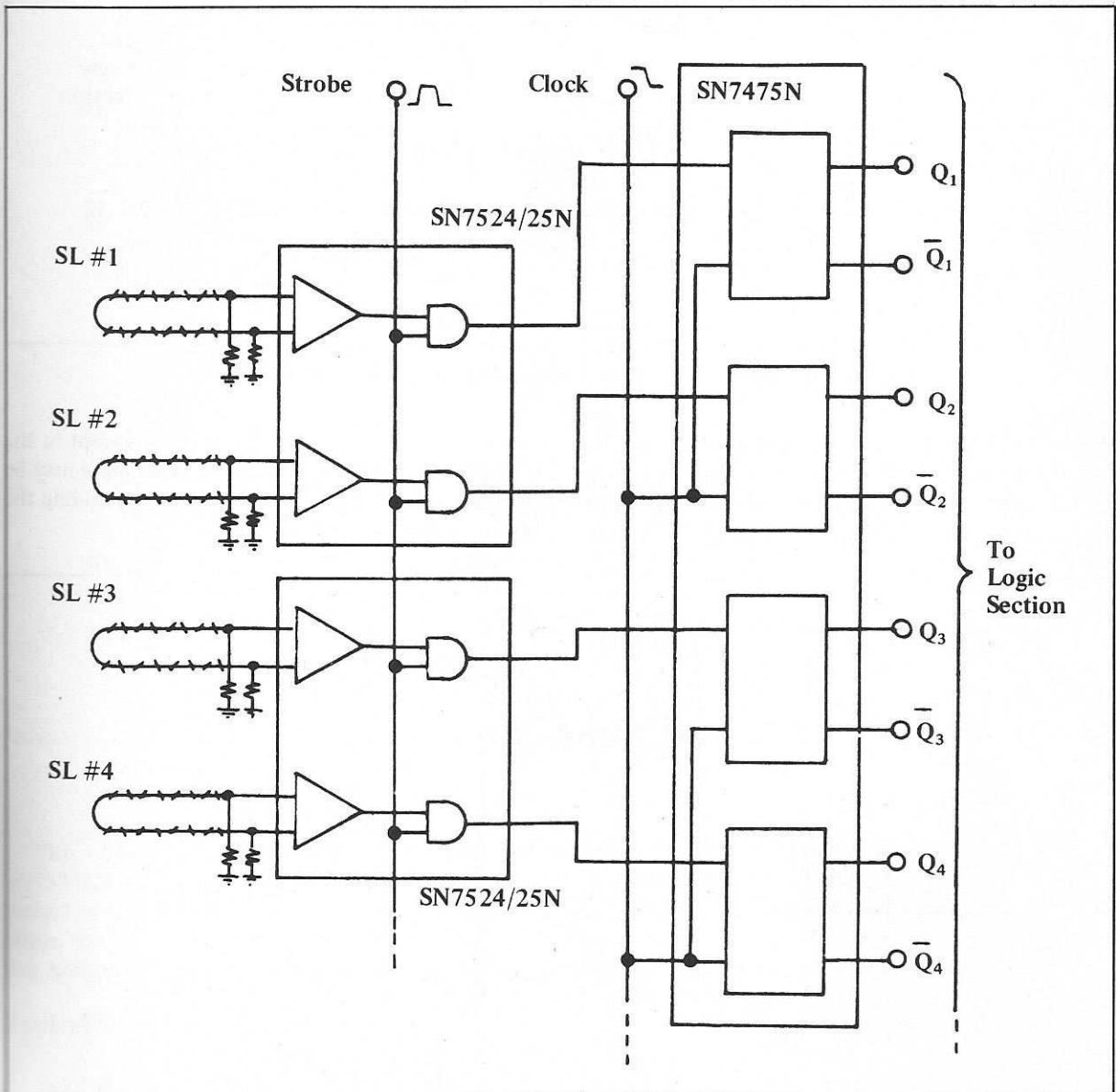


Figure 7.

In this application, the SN7475N functions as the memory data register (MDR) for two of the SN7524/25N packages. Four bits of the memory word can thus be sensed and stored with only three integrated circuit packages. Operation can be explained as follows. As long as the clock input to the SN7475N is high, the Q output follows the D input. When the clock input goes low, the information contained in the latch is retained until the clock input is permitted to return to the high state. When used

with the SN7534/25Ns the SN7475N can be used to retain information read from the memory for as long as is desirable. The negative edge of the clock must be timed so that it occurs while the desired information is present at the output of the SN7524/25N sense amplifiers.

For a more exotic application, a SN7474N dual d-type flip-flop may be used with a SN7524/25N in Figure 8.

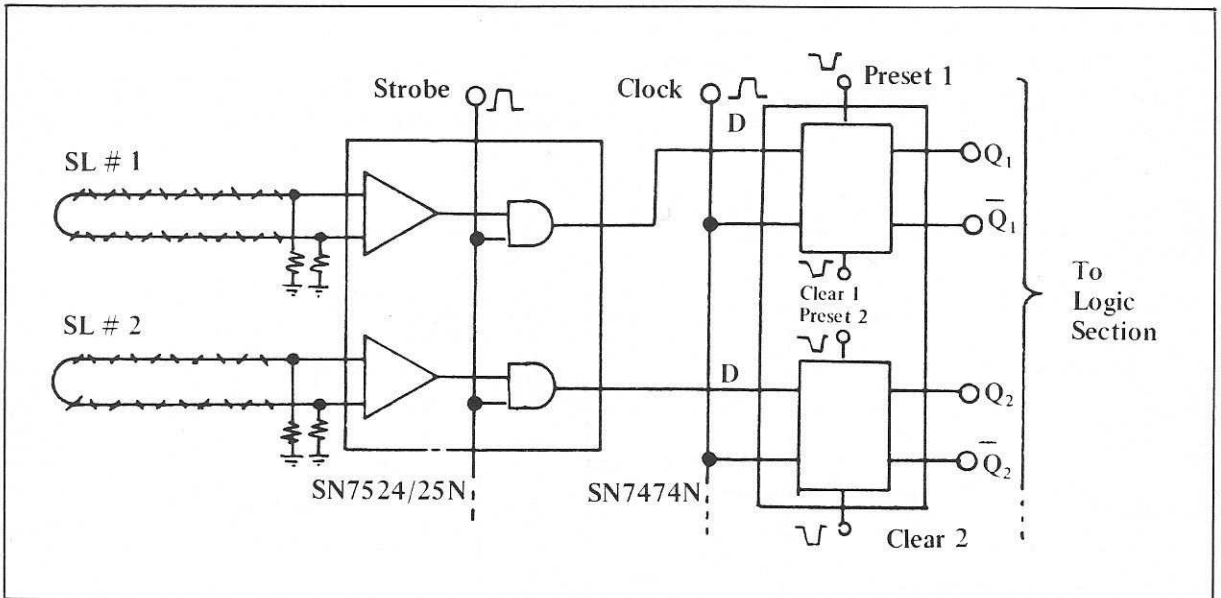


Figure 8. THE SN7474N FUNCTIONS IN A MANNER SIMILAR TO THE SN7475N

The SN7474N functions in a manner similar to the SN7475N. Operation is as follows. The positive edge of the clock pulse shifts the information present at the D input to the Q output of the flip-flop. The Q

output does not "follow" the D input except in the clock pulse command. The strobe input pulse may be used to supply the clock input pulse by adding the proper delays, see Figure 9.

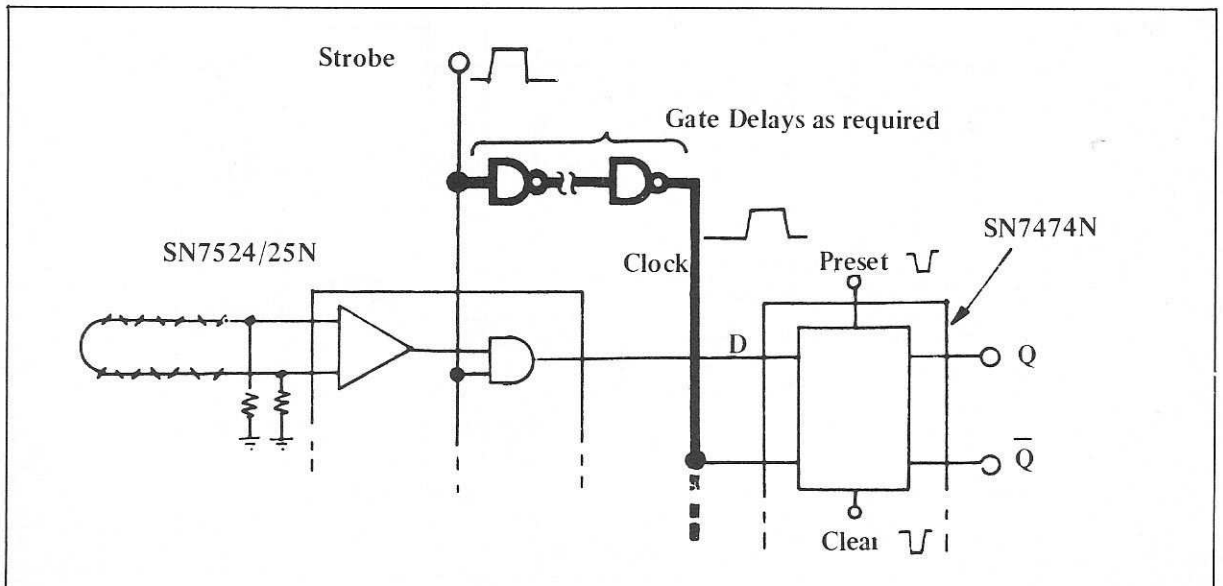


Figure 9.

The positive edge of the strobe pulse should occur during the input pulse. The delays introduced from the strobe input to the clock input will allow the sense information to propagate to the D input of the flip-flop, thereby insuring that the clock pulse is properly timed with respect to the D input information. Since each SN7474N contains two D-type flip-flops two planes can be serviced by a single SN7474N and a single SN7524/25N. The SN7474N

may be desirable over the SN7475N since it includes external set and clear inputs, allowing entry into the two bits of the memory data register (formed by the SN7474N) from an external source.

If it becomes desirable to "OR" the outputs of the SN7524/25N, this can readily be accomplished with the addition of a positive NOR gate, such as is a part of the SN7402N TTL device, as shown in Figure 10. This device is a quadruple 2-input positive NOR gate.

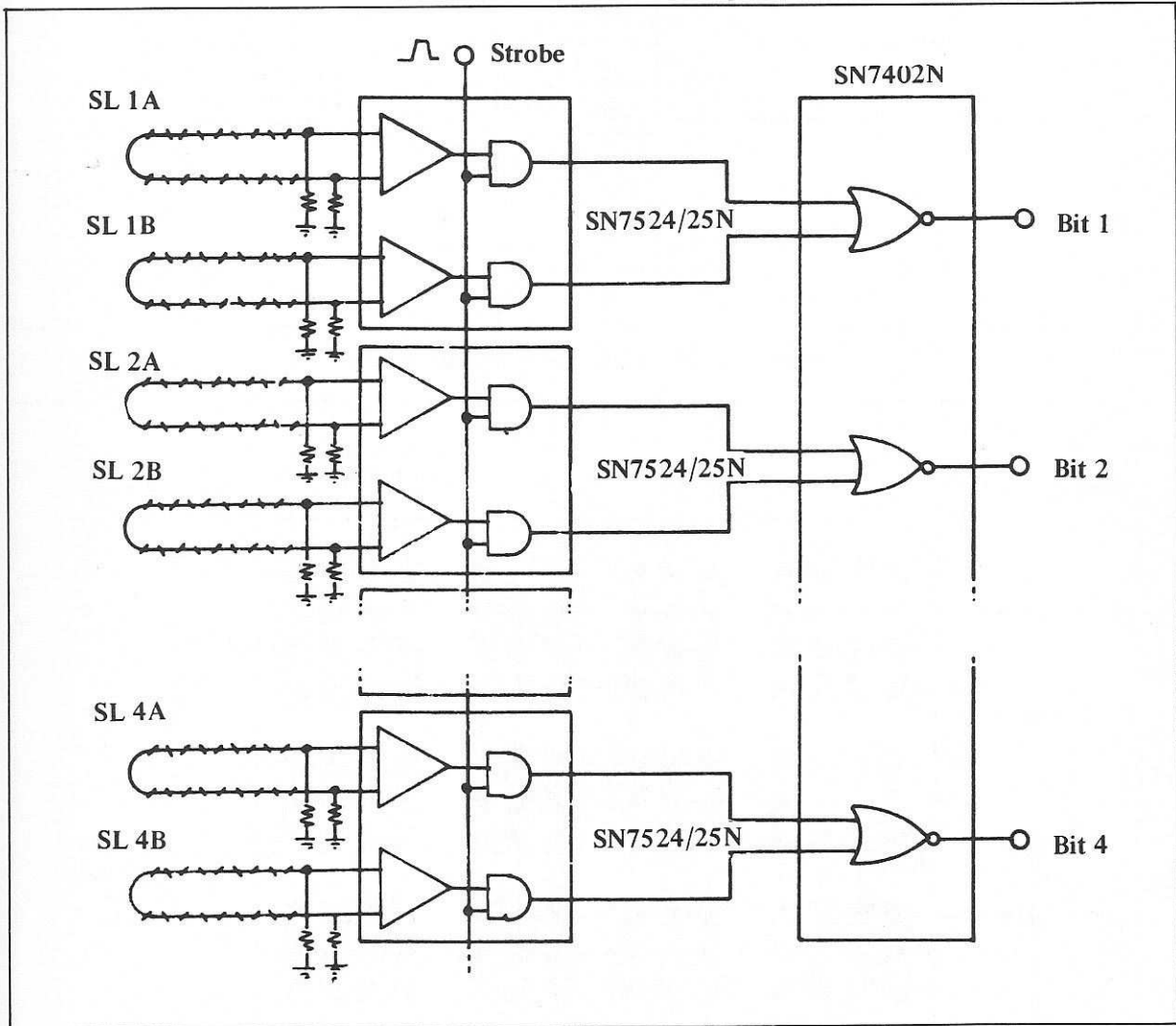


Figure 10.

The SN7402N can "OR" four pairs of SN7524/25N outputs. If more than two outputs are desired in the OR connection, it is more desirable to utilize the Wire-OR capability of the SN7522/23N in this application.

Typical System Applications

The following figures (Figures 11 to 14), show in detail how the Series 7520 sense amplifiers can be used in either 3D or 2 1/2D memory applications.

These are representative memories and may not apply to all memory configurations of the 3D or 2 1/2D type. However, the basic sense amplifier application can be seen.

In either application, the most optimum threshold level can be determined for the memory by adjusting the threshold levels of the sense amplifiers. In extremely "tight" designs, it may be desirable to adjust sense amplifier threshold levels on an individual package basis. On less stringent applications, all threshold levels may be adjusted in parallel.

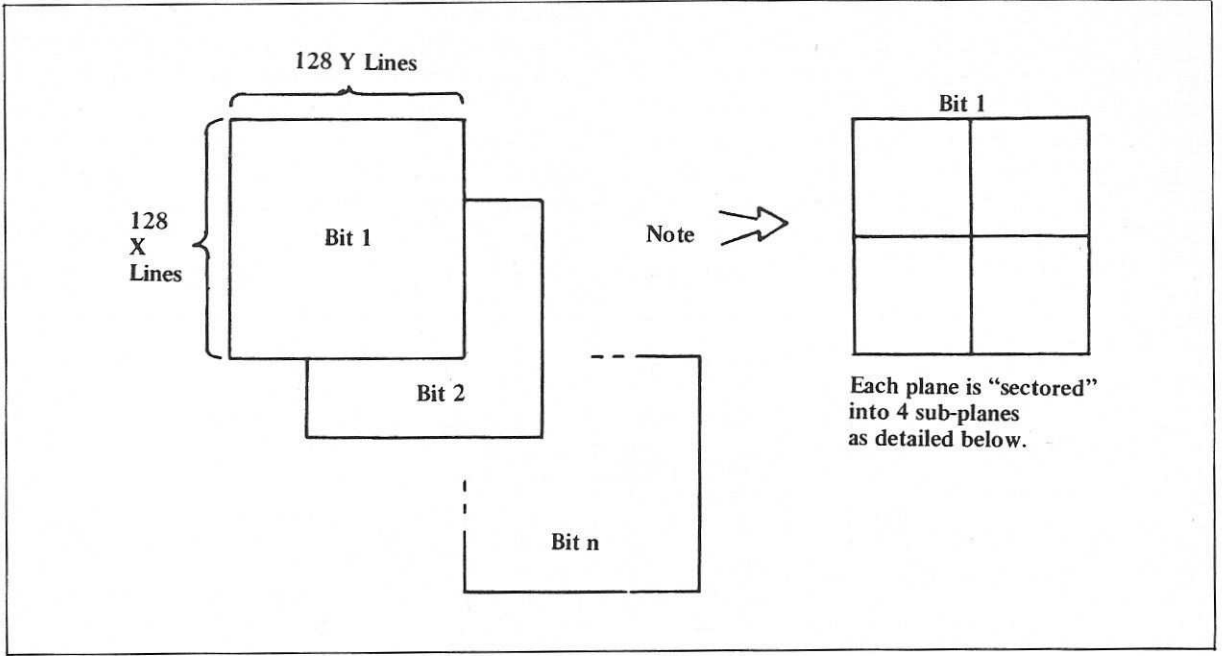


Figure 11a. LOGICAL MEMORY ORGANIZATION

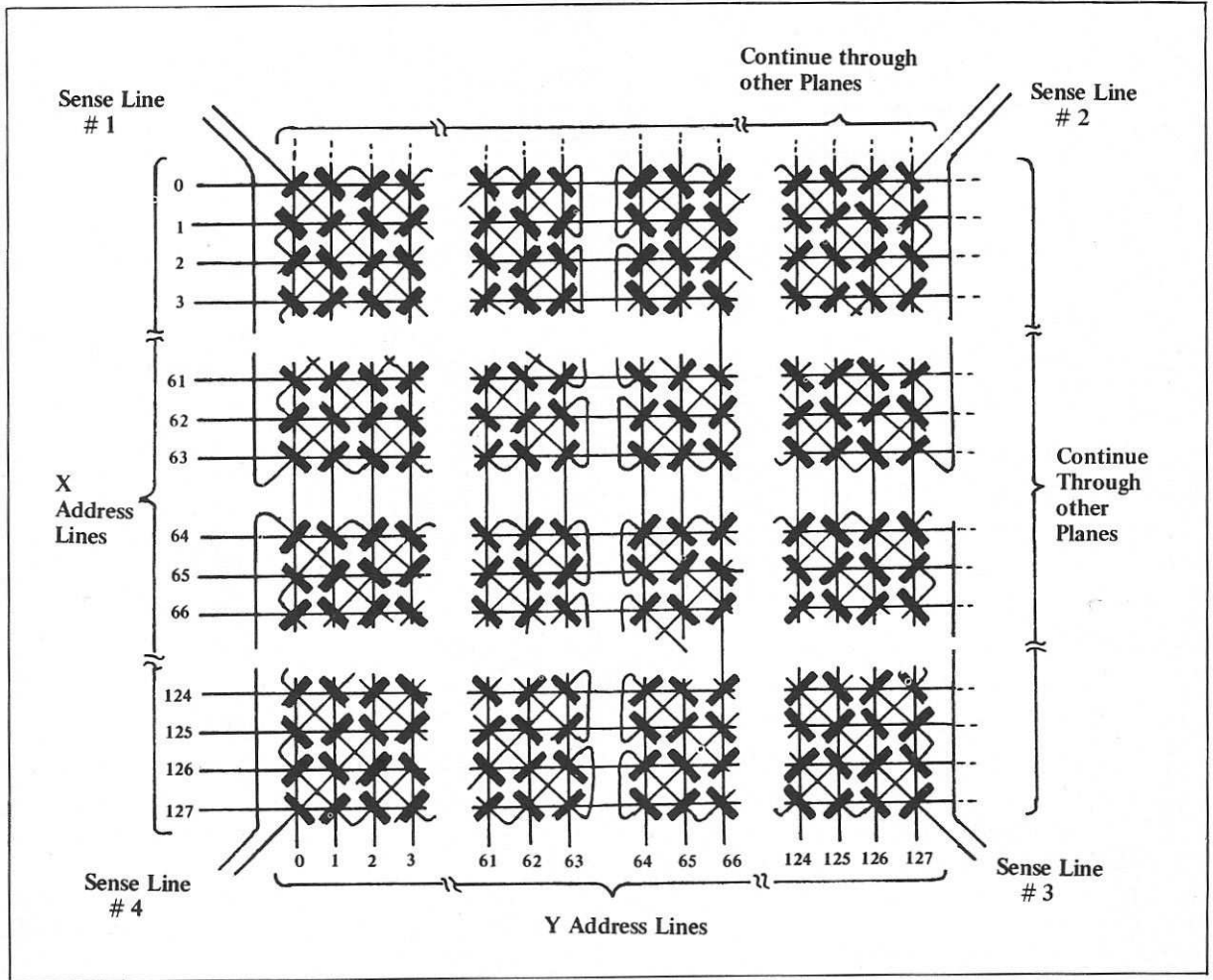


Figure 11b. DETAILED MEMORY WIRING

Figure 11. TYPICAL 3D MEMORY APPLICATION (16K N-BIT WORDS)

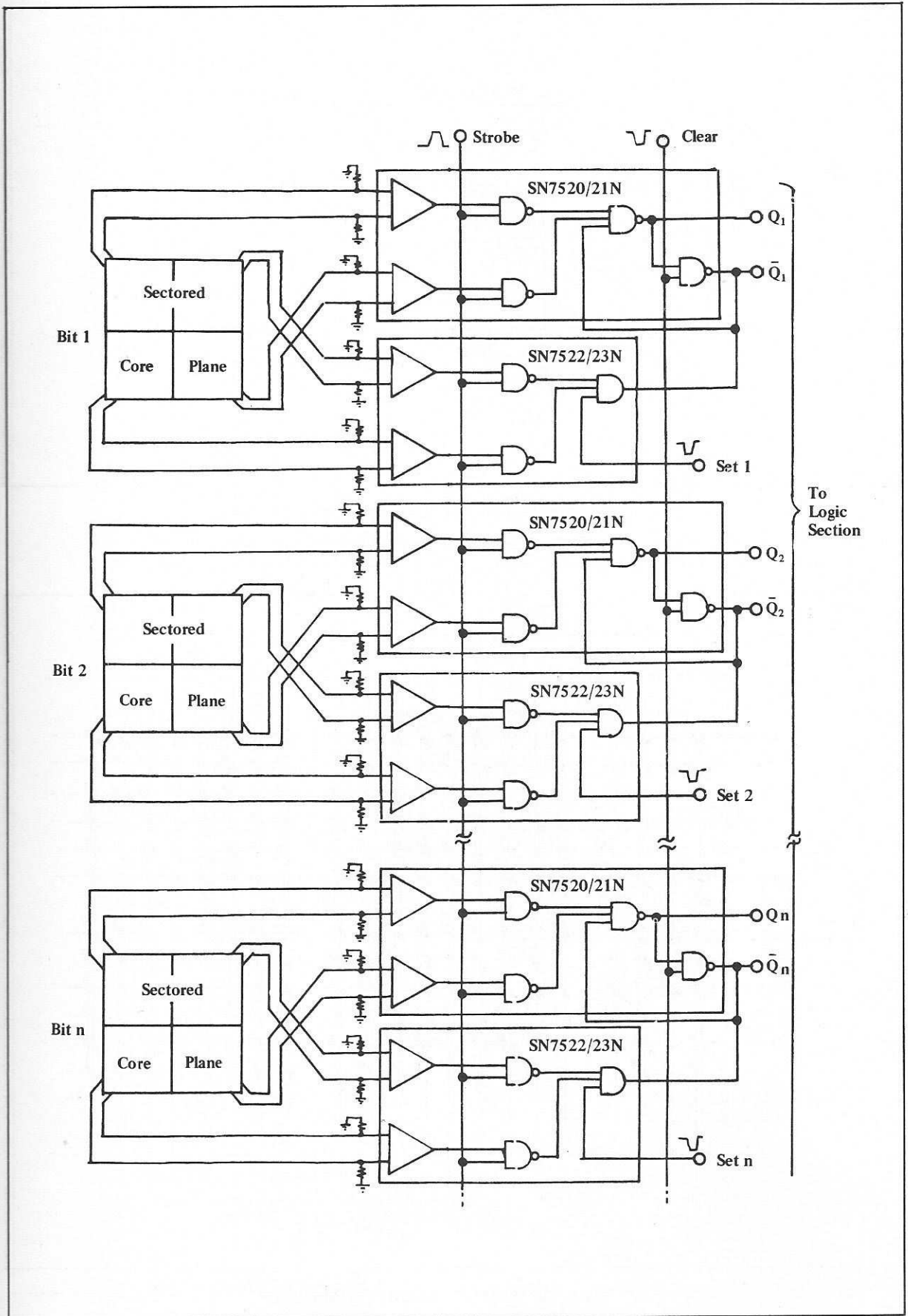


Figure 12. USE OF SN7520/21N AND SN7522/23N WITH 16K WORD 3D MEMORIES

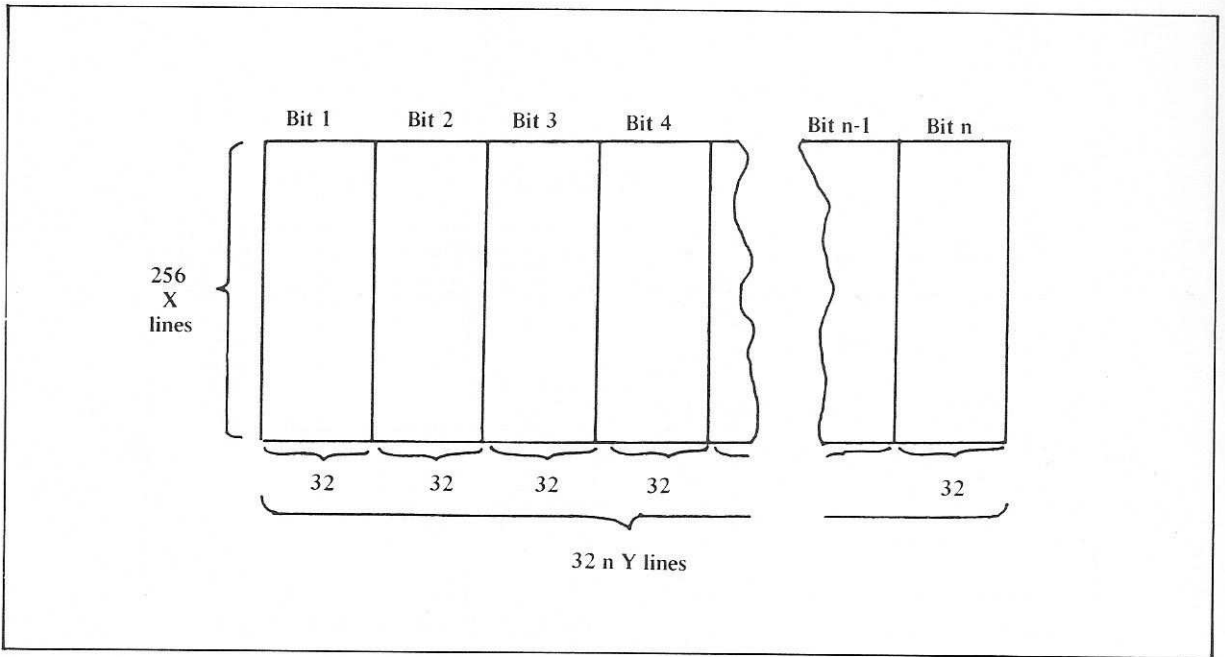


Figure 13a. TYPICAL LOGICAL MEMORY ORGANIZATION

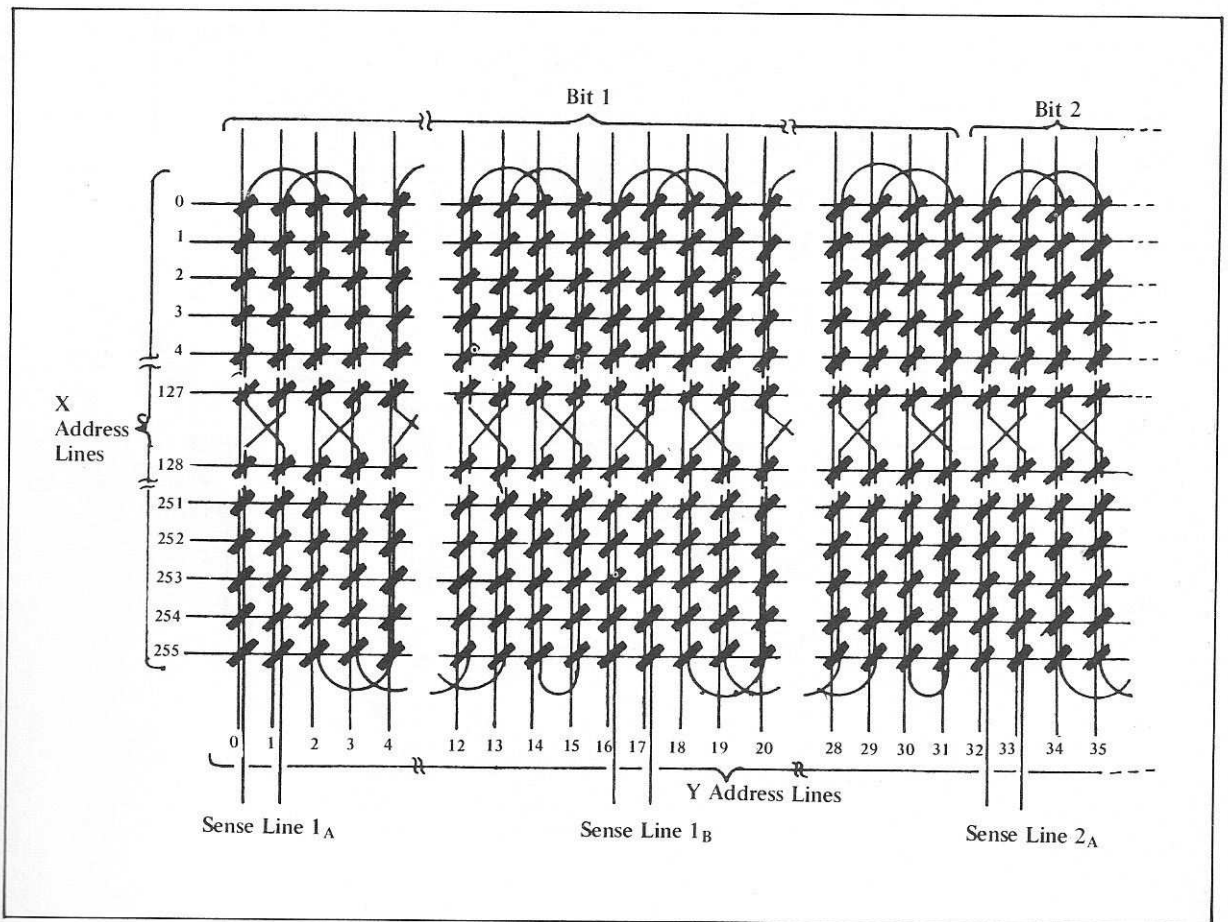


Figure 13b. DETAILED MEMORY WIRING

Figure 13. TYPICAL 2 1/2D MEMORY APPLICATION (8K N-BIT WORDS)

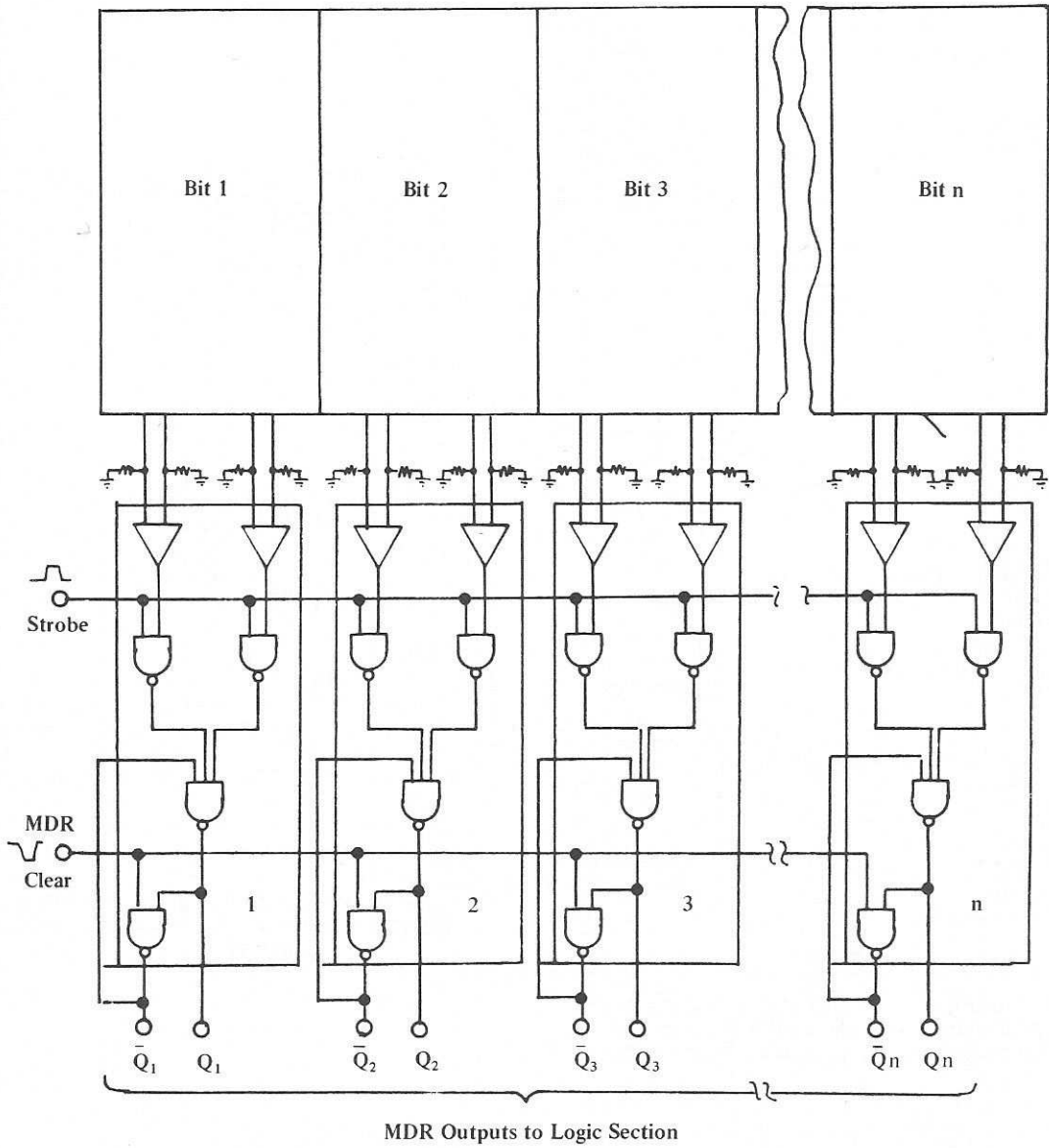


Figure 14. USE OF SN7520/21N WITH 8K WORD 2 1/2D MEMORY (SN 7520/21N CONNECTED IN MDR LATCH CONFIGURATION)

Applications of the SN75324 Monolithic Memory Driver

This section briefly describes the SN75324 monolithic integrated-circuit memory driver and illustrates how to use it to address and drive a magnetic memory. Detailed specifications of this circuit are found in the appropriate data sheet.

Description of SN75324

A functional diagram of the SN75324 appears in Figure 1. This unit is designed specifically to replace

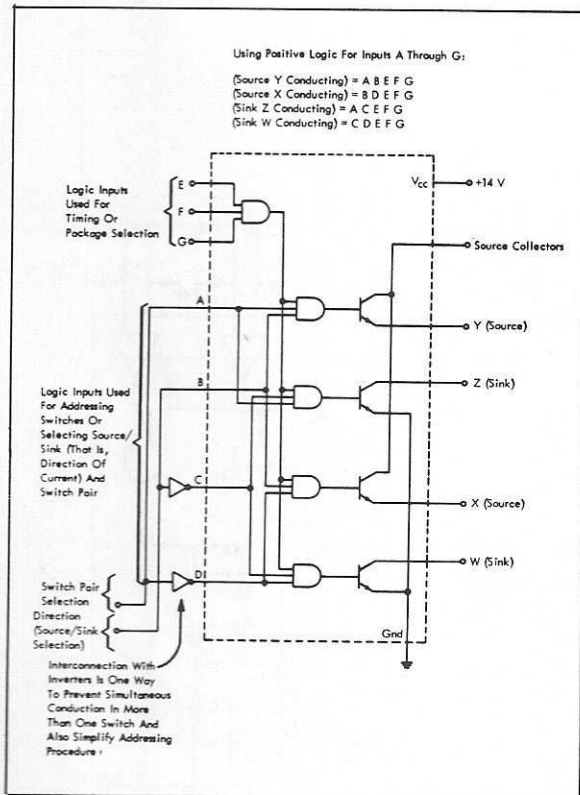


Figure 1. SIMPLIFIED FUNCTIONAL DIAGRAM AND LOGIC TABLE FOR SN75324 WITH TYPICAL INTER-CONNECTION OF ADDRESS INPUTS

traditional discrete transistor-transformer circuits in magnetic memory systems. However, it can also be used as a lamp driver, relay driver, or high-fan-out logic gate. It consists of four fast, high-current switches controlled by seven logic inputs (denoted A through G) that are compatible with 74 TTL and other standard logic systems with precautions mentioned under "Logic Input" below. One pole of each switch leads outside the unit (outputs W, X, Y, and Z). On their opposite poles, two of the switches connect to the memory current source, and the other two connect to ground. Thus two outputs are sources and two are sinks for memory drive current.

The decoding circuitry is arranged so that any or all of the switches in a package may be conducting at any given time. However, the unit will overheat if more than one switch at a time carries memory current. Therefore the system must be designed to prevent this occurrence by such means as the external logic inverters shown in Figure 1.

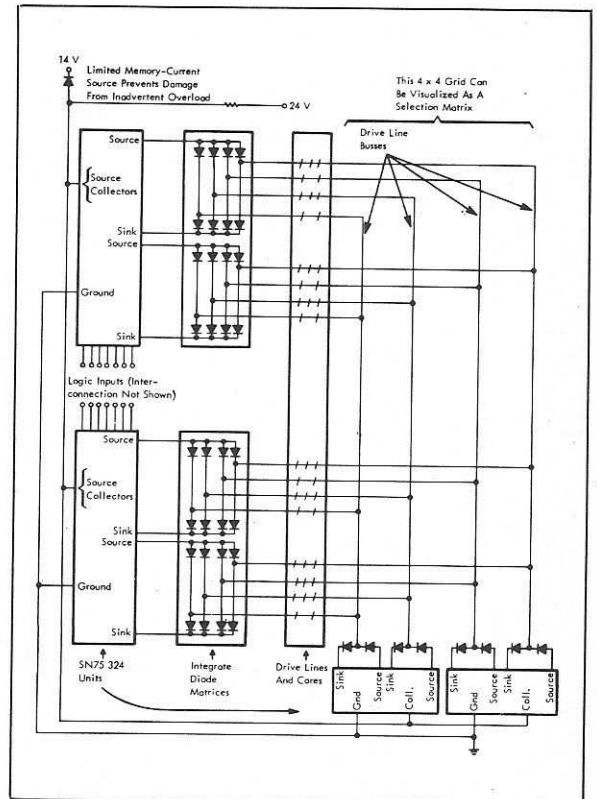


Figure 2. TYPICAL APPLICATION OF SN75324 IN MEMORY-DRIVE: A SELECTION SCHEME FOR 16 DRIVE LINES

Memory-Drive Applications

In memory-drive applications, the SN75324 can be connected in any of several fashions. Typically, however, sources and sinks are arranged in pairs from which many drive lines branch off, as shown in Figure 2. Here each drive line is served by a unique combination of two source/sink pairs, so that a selection matrix is formed. The size of such a matrix is limited only by the number of drive lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive line of the particular system imposes on the driver.

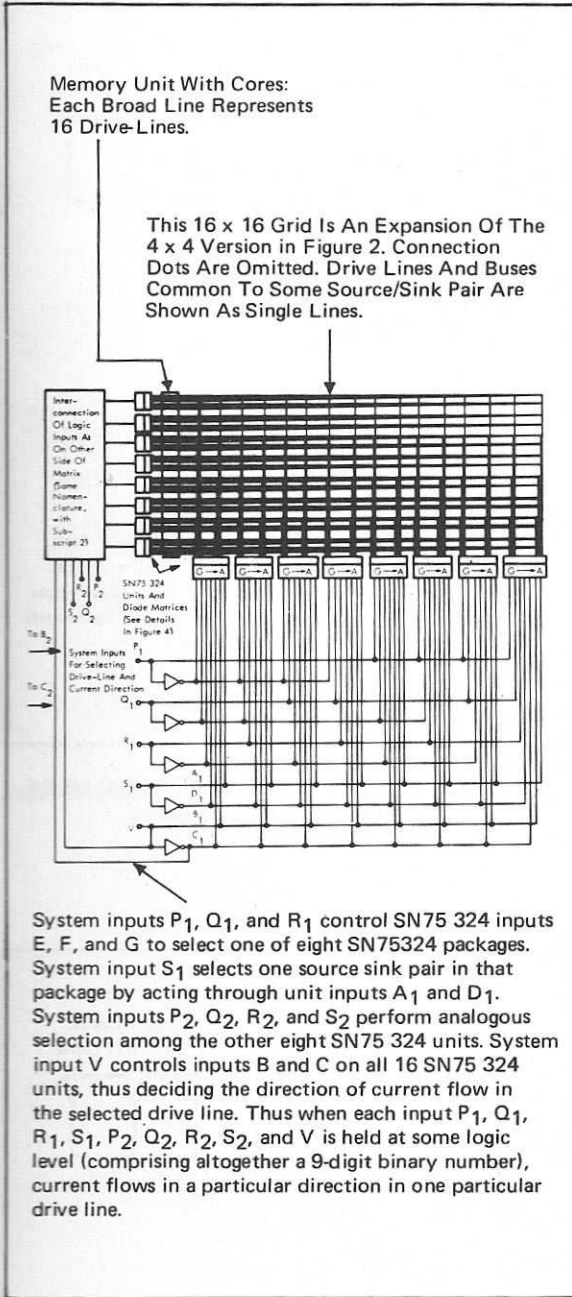


Figure 3. SN75324 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY, WITH HYPOTHETICAL LOGIC INTERCONNECTIONS TO SHOW INPUT FLEXIBILITY

A larger selection matrix is shown in Figures 3 and 4. The hypothetical interconnection of logic inputs demonstrates one way to take advantage of the multiple logic inputs of the SN75324.

Regardless of the particular line-selection and logic scheme, the SN75324 can be densely mounted on printed-wiring boards along with monolithic diode arrays and IC logic packages. The result normally is a system that is cheaper, faster, smaller, more reliable, and simpler to connect than a conventional discrete transistor-transformer version.

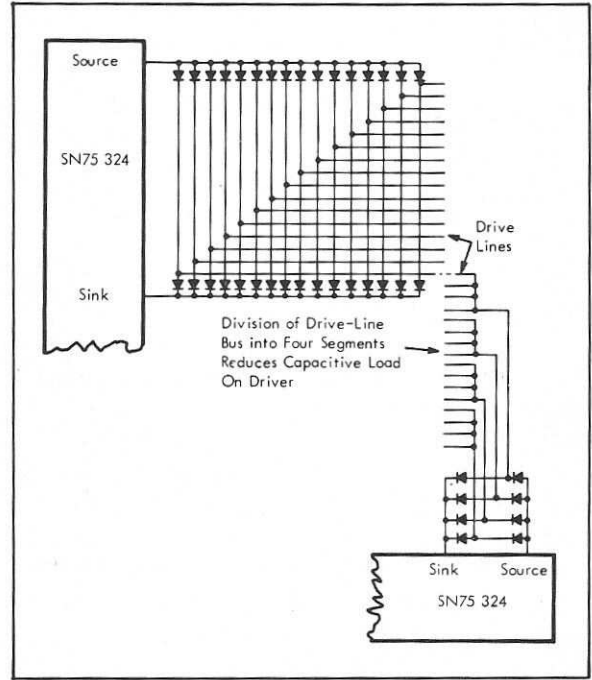


Figure 4. DETAILS OF CONNECTION OF DRIVE-LINES TO DRIVERS IN Figure 3.

Logic Input from 74 TTL

Because of the high-noise environment in which the SN75324 is intended to operate, the input logic levels have been purposely designed to be somewhat higher than standard 74 TTL logic levels, as compared below:

	54/74 TTL	SN75 324
$V_{out(0)}$	0.4 V max.	---
$V_{out(1)}$	2.4 V min.	---
$V_{in(0)}$	0.8 V max.	1.0 V max.
$V_{in(1)}$	2.0 V min.	3.5 V min.
$V_{threshold}$	1.4 V typ.	2.3 V typ.

The higher logical 0 input level, $V_{in(0)}$ of the SN75324 guarantees a d-c noise margin of 600 mV when driven from 74 TTL. However, the higher $V_{in(1)}$ of the SN75324 (3.5 V) leads to some minor difficulties when using 54/74 TTL. The minimum guaranteed logical 1 level of 2.4 V at a 54/74 TTL output falls short of the 3.5-V minimum level required at the SN75324 input. However, this problem can be readily solved by the proper selection of a pull-up resistor at the gate output as shown in Figure 5.

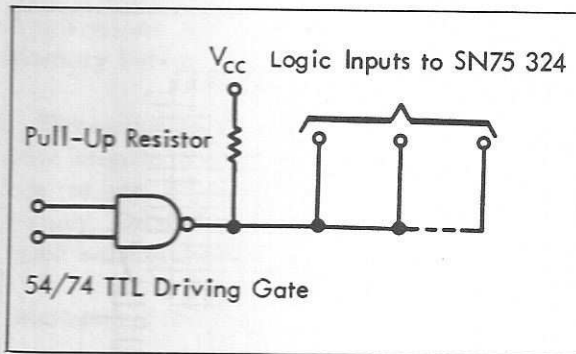


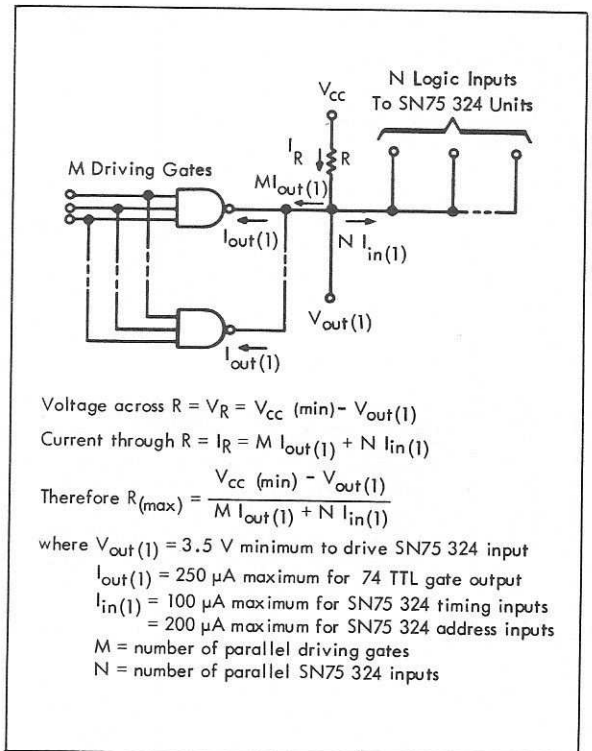
Figure 5. INPUT TO SN75324 FROM 74 TTL USING PULL-UP RESISTOR

Because of the high logical 0 input current of the SN75324 (12mA for the timing inputs, 6mA for the address inputs), it may be desirable to drive the inputs from 74 TTL buffer gates (SN7440 or SN74H40) to assure adequate sink current capability. Each SN7440 buffer gate output is specified at 0.4 V maximum $V_{out(0)}$ at a sink current of 48mA. The $V_{out(0)}$ for the SN74H40 buffer gate is 0.4 V at a sink current of 60mA. If additional sink current is required, the inputs and outputs of both gates in the SN7440 or SN74H40 package may be paralleled for 96 and 120mA capability, respectively. (This parallel connection requires no significant sacrifice, if any, in switching characteristics, but the outputs of these gates should not be paralleled without also paralleling inputs. Otherwise one or both of the gates can be damaged because of the active pull-up or "totem-pole" output configuration.)

A large number of SN75324 inputs may also be driven from the output of any of several 74 TTL decode/drivers. For example, the output of the SN7445 BCD-to-Decimal Decode/Driver can sink 80mA at $V_{out(0)}$ of 0.9 V or sink 20mA at $V_{out(0)}$ of 0.4 V. Since the maximum $V_{in(0)}$ of the SN75324 is 1.0 V, the SN7445 can drive the SN75324 with a pull-up resistor.

When a pull-up resistor is used at the driving gate output, its value must be determined to ensure proper logic levels. The worst-case resistor values may be readily calculated using available driving gate data sheet information, as exemplified below.

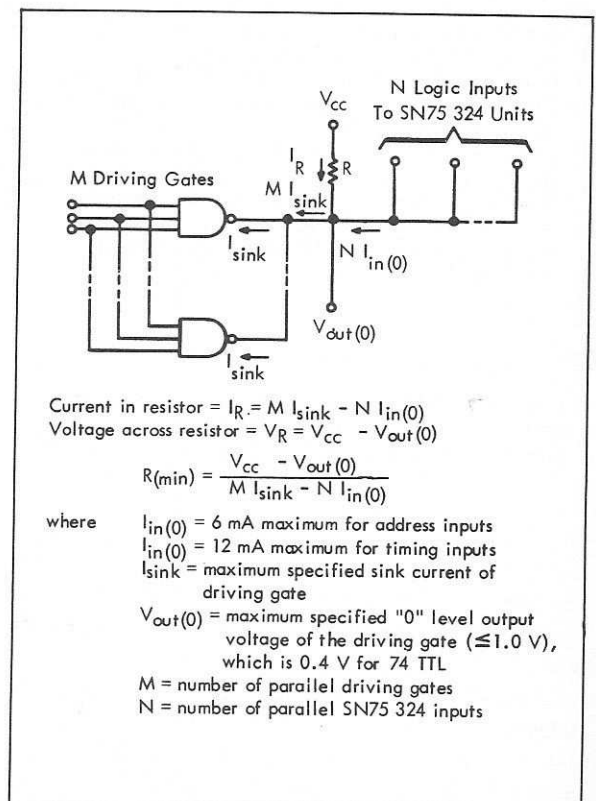
The maximum resistor value is calculated to ensure that sufficient current is available when the driving gate output is high (off). This current must supply the SN75324 input as well as the driving gate output. For a logical 1, it is necessary to maintain 3.5 V minimum at the SN75324 input. A suggested method of calculating the maximum resistor value is shown in Figure 6. The minimum value of the resistor is calculated to ensure that its current plus that from the SN75324 inputs will not cause the output voltage $V_{out(0)}$ of the driving gate to exceed the maximum of 1.0 V. (See Figure 7).



$$\begin{aligned} \text{Voltage across } R &= V_R = V_{CC} (\text{min}) - V_{out(1)} \\ \text{Current through } R &= I_R = M I_{out(1)} + N I_{in(1)} \\ \text{Therefore } R_{(\text{max})} &= \frac{V_{CC} (\text{min}) - V_{out(1)}}{M I_{out(1)} + N I_{in(1)}} \end{aligned}$$

where $V_{out(1)} = 3.5 \text{ V}$ minimum to drive SN75324 input
 $I_{out(1)} = 250 \mu\text{A}$ maximum for 74 TTL gate output
 $I_{in(1)} = 100 \mu\text{A}$ maximum for SN75324 timing inputs
 $= 200 \mu\text{A}$ maximum for SN75324 address inputs
 $M =$ number of parallel driving gates
 $N =$ number of parallel SN75324 inputs

Figure 6. CALCULATION OF MAXIMUM VALUE OF PULL-UP RESISTOR IN Figure 5.



$$\begin{aligned} \text{Current in resistor} &= I_R = M I_{\text{sink}} - N I_{in(0)} \\ \text{Voltage across resistor} &= V_R = V_{CC} - V_{out(0)} \\ R_{(\text{min})} &= \frac{V_{CC} - V_{out(0)}}{M I_{\text{sink}} - N I_{in(0)}} \end{aligned}$$

where $I_{in(0)} = 6 \text{ mA}$ maximum for address inputs
 $I_{in(0)} = 12 \text{ mA}$ maximum for timing inputs
 $I_{\text{sink}} =$ maximum specified sink current of driving gate
 $V_{out(0)} =$ maximum specified "0" level output voltage of the driving gate ($\leq 1.0 \text{ V}$), which is 0.4 V for 74 TTL
 $M =$ number of parallel driving gates
 $N =$ number of parallel SN75324 inputs

Figure 7. CALCULATION OF MINIMUM VALUE OF PULL-UP RESISTOR IN Figure 5.

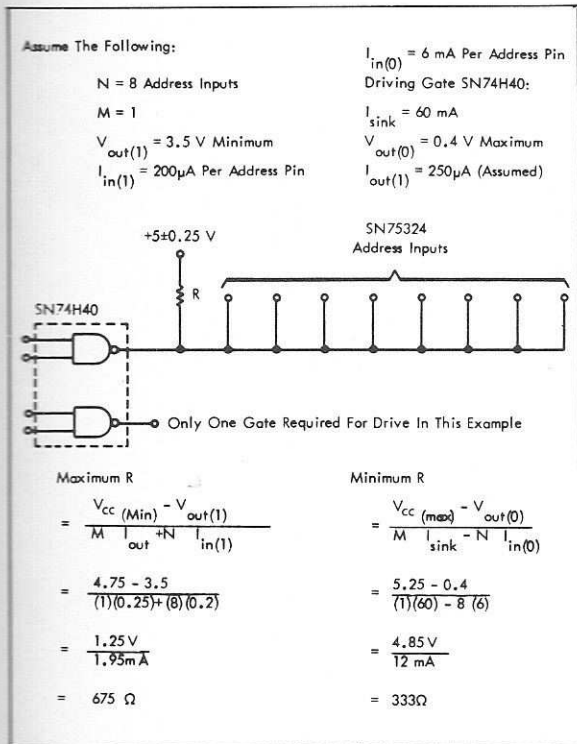


Figure 8. SAMPLE CALCULATION OF PULL-UP RESISTOR VALUE FOR SN74H40.

After determining the worst-case minimum and maximum pull-up resistor values, any value between the limits may be selected. (Obviously, the calculated minimum value must be below the calculated maximum value to be practical). Selecting a resistor value near the minimum limit will raise the logical 1 voltage and thereby improve the logical 1 noise margin.

An example of an SN74H40 buffer gate driving eight SN75324 address inputs is shown along with sample calculations in Figure 8. If, in this example, a value of 400Ω is selected for the pull-up resistor, the guaranteed logic levels at the SN75324 inputs are 0.4 V maximum for $V_{in(0)}$ and 4.0 V minimum for $V_{in(1)}$. This resistor results in guaranteed d-c noise margins of 600 mV at the logical 0 level and 500 mV at the logical 1 level at worst-case conditions.

Applications of the SN75325 Memory Driver

This device has the same use as the SN75324 but does not incorporate the decode facility, however, it is capable of sinking (sourcing more current, viz 600 mA .) An SN74154 can be used to provide the required decode function. Apart from this, the applications of the SN75325 are similar to those of the SN75324.