

Interfacing the DP8422A to the 68000-16 (Zero Wait State Burst Mode Access)

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Lawson H.C. Chang
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INTRODUCTION

This application note describes interfacing the DP8422A DRAM controller (also applicable to DP8420A/21A) to the 68000 (16 MHz) with slower memories. This design is based upon burst mode access by holding \overline{RAS} low and toggling \overline{CAS} . It is assumed that the user is familiar with the DP8422A and 68000 mode operations.

DESIGN DESCRIPTION

This design consists of the DP8422A DRAM controller, a PAL (20R4D), and a page detector (ALS6311). This design accommodates four banks of DRAM, each bank being 16 bits in width, giving maximum memory capacity of either 2 Mbytes (using 256k x 4 light load DRAMs) or 8 Mbytes (using 1M x 1 DRAMs). The schematic diagram of interfacing DP8422A to the 68000 is shown in *Figure 1*. The DP8422A is operated in Mode 1. An access cycle begins when the 68000 places a valid address on the address bus and asserts the Address Strobe (\overline{AS}) if a refresh or Port B access (DP8422A only) is not in progress. The proper \overline{RAS} and \overline{CAS} will be asserted respectively, depending upon programming bits C6, C5, and C4 for \overline{RAS} and \overline{CAS} configuration after guaranteeing the programmed value of row address hold time and the column address setup time.

The High Speed Access (\overline{HSA}) output signal of page detector indicates whether the current access is in the same page as previous access or not. \overline{ADS} (\overline{AREQ}) is kept low if the current access is in the page, otherwise \overline{ADS} (\overline{AREQ}) will be forced to go high to terminate the burst access. Internal refresh logic automatically generates refresh request every 15 μ s. Since the 256k x 4 DRAM data input and output signals can be controlled by the Output Enable (\overline{OE}). Transceivers (F245) could be eliminated from this design if 256k x 4 DRAM light load DRAM were used. The timing diagrams are shown in *Figure 2* and *Figure 3*.

DP8422A PROGRAMMING BITS

u = user defined

Programming Bits	Description
R0,R1 = 0,1	\overline{RAS} high and low times
R2,R3 = u,u	\overline{DTACK} generation mode for nonburst access
R4,R5 = u,u	\overline{DTACK} generation mode for burst access
R6 = 0	Add wait states if \overline{WAITIN} is low
R7 = 1	\overline{DTACK} mode select
R8 = 1	Noninterleave mode
R9 = u	All \overline{RAS} 's or staggered refresh select
C0,C1,C2 = 0,1,0	Refresh clock divisor select
C3 = 0	Refresh clock divider select
C4,C5,C6 = u,u,u	\overline{RAS} and \overline{CAS} configuration mode
C7 = 1	tASC mode select
C8 = 1	tRAH mode select
C9 = u	Delay \overline{CAS} during write access mode select

Programming

Bits	Description
B0 = 1	Fall through mode
B1 = 1	Mode 1 access
$\overline{ECAS0}$ = 1	Extend \overline{CAS} and refresh request

DESIGN TIMING PARAMETERS

Timing parameters are referenced to the numbers shown in the DP8422A data sheet timing parameters. Numbered times starting with a "\$" refer to DP8422A timing parameters. Numbered times starting with a "#" refer to 68000 timing parameters.

16 MHz T_{cp} = 62.5 ns	
\$400b: \overline{ADS} asserted setup to CLK	
T_{cp} - PAL tCLK max.	
= 62.5 ns - 8 ns	
= 54.5 ns	
\$401: \overline{CS} setup to \overline{ADS} asserted	
2 T_{cp} - #6 \overline{CLK} to Address valid - PAL tp max.	
= 125 ns - 55 ns - 10 ns	
= 60 ns	
#47: \overline{DTACK} (68000) low setup to CLK low	
T_{cp} - \$18 CLK to \overline{DTACK} (DP8422A) asserted - PAL tp max.	
= 62.5 ns - 28 ns - 10 ns	
= 24.5 ns	(DP8422A-25)
= 62.5 ns - 33 ns - 10 ns	
= 19.5 ns	(DP8422A-20)

I. LIGHT LOAD TIMING

tRAC (nonburst access):	
3 T_{cp} - PAL tCLK max. - \$402 \overline{ADS} low to \overline{RAS} low - #27 data setup - F245 Transceiver tp max.	
= 187.5 ns - 8 ns - 25 ns - 7 ns - 6 ns	
= 141.5 ns	(DP8422A-25)
= 187.5 ns - 8 ns - 30 ns - 7 ns - 6 ns	
= 136.5 ns	(DP8422A-20)
tCAC (nonburst access):	
3 T_{cp} - PAL tCLK max. - \$403a \overline{ADS} low to \overline{CAS} low - #27 data setup - F245 Transceiver tp max.	
= 187.5 ns - 8 ns - 75 ns - 7 ns - 6 ns	
= 91.5 ns	(DP8422A-25)
= 187.5 ns - 8 ns - 86 ns - 7 ns - 6 ns	
= 80.5 ns	(DP8422A-20)
tAA (nonburst access):	
3 T_{cp} - PAL tCLK max. - \$417 \overline{ADS} low to Column Address valid - #27 data setup - F245 Transceiver tp max.	
= 187.5 ns - 8 ns - 69 ns - 7 ns - 6 ns	
= 97.5 ns	(DP8422A-25)
= 187.5 ns - 8 ns - 83 ns - 7 ns - 6 ns	
= 83.5 ns	(DP8422A-20)

tCAC (burst access):

2.5 T_{cp} - #9 $\overline{\text{CLK}}$ high to $\overline{\text{DS}}$ low max. - PAL tp max. - \$14 $\overline{\text{ECAS}}$ low to $\overline{\text{CAS}}$ low max. - #27 data setup - F245 Transceiver tp max.

= 156 ns - 40 ns - 10 ns - 20 ns - 7 - 6 ns
= 73 ns (DP8422A-25)
= 156 ns - 40 ns - 10 ns - 23 ns - 7 ns - 6 ns
= 70 ns (DP8422A-20)

tAA (burst access):

3 T_{cp} - #6 $\overline{\text{CLK}}$ low to Address valid max. - \$26 Address valid to Q max. - #27 data setup - F245 Transceiver tp max.

= 187.5 ns - 5 ns - 26 ns - 7 ns - 6 ns
= 98.5 ns (DP8422A-25)
= 187.5 ns - 5 ns - 29 ns - 7 ns - 6 ns
= 95.5 ns (DP8422A-20)

II. HEAVY LOAD TIMING

tRAC (nonburst access):

3 T_{cp} - PAL tCLK max. - \$402 $\overline{\text{ADS}}$ low to $\overline{\text{RAS}}$ low - #27 data setup - F245 Transceiver tp max.

= 187.5 ns - 8 ns - 29 ns - 7 ns - 6 ns
= 137.5 ns (DP8422A-25)
= 187.5 ns - 8 ns - 35 ns - 7 ns - 6 ns
= 131.5 ns (DP8422A-20)

tCAC (nonburst access):

3 T_{cp} - PAL tCLK max. - \$403a $\overline{\text{ADS}}$ low to $\overline{\text{CAS}}$ low - #27 data setup - F245 Transceiver tp max.

= 187.5 ns - 8 ns - 82 ns - 7 ns - 6 ns
= 84.5 ns (DP8422A-25)
= 187.5 ns - 8 ns - 94 ns - 7 ns - 6 ns
= 72.5 ns (DP8422A-20)

tAA (nonburst access):

3 T_{cp} - PAL tCLK max. - \$417 $\overline{\text{ADS}}$ low to Column Address valid - #27 data setup - F245 Transceiver tp max.

= 187.5 ns - 8 ns - 78 ns - 7 ns - 6 ns
= 88.5 ns (DP8422A-25)
= 187.5 ns - 8 ns - 92 ns - 7 ns - 6 ns
= 74.5 ns (DP8422A-20)

tCAC (burst access):

2.5 T_{cp} - #9 $\overline{\text{CLK}}$ high to $\overline{\text{DS}}$ low max. - PAL tp max. - \$14 $\overline{\text{ECAS}}$ low to $\overline{\text{CAS}}$ low max. - #27 data setup - F245 Transceiver tp max.

= 156 ns - 40 ns - 10 ns - 27 ns - 7 ns - 6 ns
= 66 ns (DP8422A-25)
= 156 ns - 40 ns - 10 ns - 31 ns - 7 ns - 6 ns
= 62 ns (DP8422A-20)

tAA (burst access):

3 T_{cp} - #6 $\overline{\text{CLK}}$ low to Address valid max. - \$26 Address valid to Q max. - #27 data setup - F245 Transceiver tp max.

= 187.5 ns - 5 ns - 35 ns - 7 ns - 6 ns
= 89.5 ns (DP8422A-25)
= 187.5 ns - 5 ns - 38 ns - 7 ns - 6 ns
= 86.5 ns (DP8422A-20)

68KPAL (PAL20R4D) EQUATIONS

The Boolean entry operators are listed as:

“:=” Replaced by (after clock)
“=” Equality
“*” AND
“+” OR
“/” Complement
“~” Active low

The brief explanation of PAL output signals

CS~ This combinational output signal is Chip Select.
CSD~ This sequential output signal is Chip Select Delayed by one clock.
ADS~ This sequential output signal is Address Strobe (also used as an Access Request, $\overline{\text{AREQ}}$, to DP8422A).
READY~ This combinational output signal is Data Ready.
ECASU~ This combinational output signal is to select upper byte.
ECASL~ This combinational output signal is to select lower byte.

Inputs: CLK, A21, A22, FC2, FC1, FC0, UDS~, LSD~, RFRQ~, AS~, DTACK~, HSA~

Outputs: /CS~ = /A21*/A22*/FC2*/FC1*FC0 + /A21*/A22*/FC2*FC1*/FC0 + /A21*/A22*FC2*/FC1*FC0 + /A21*/A22*FC2*FC1*/FC0

/CSD~ := /CS~

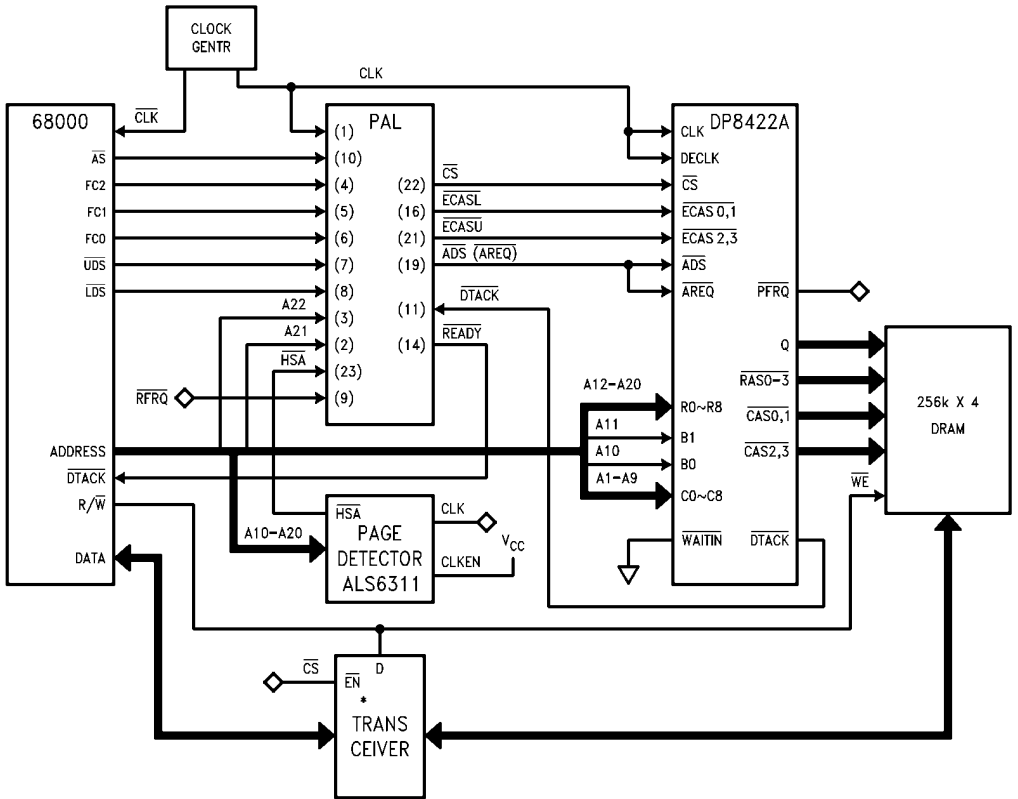
/ADS~ := /HSA~*/CSD~*RFRQ~ + /AS~*/RFRQ~

/READY~ = /DTACK~*/AS~

/ECASU~ = /ADS~*/UDS~*/CSD~*/HSA~

/ECASL~ = /ADS~*/LDS~*/CSD~*/HSA~

Note: Address inputs such as A21 and A22, are system dependent.



*Transceivers could be eliminated from this design.

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FIGURE 1.1 Schematic Diagram of Interfacing DP8422A/68000 Burst Access to 256k x 4 DRAM

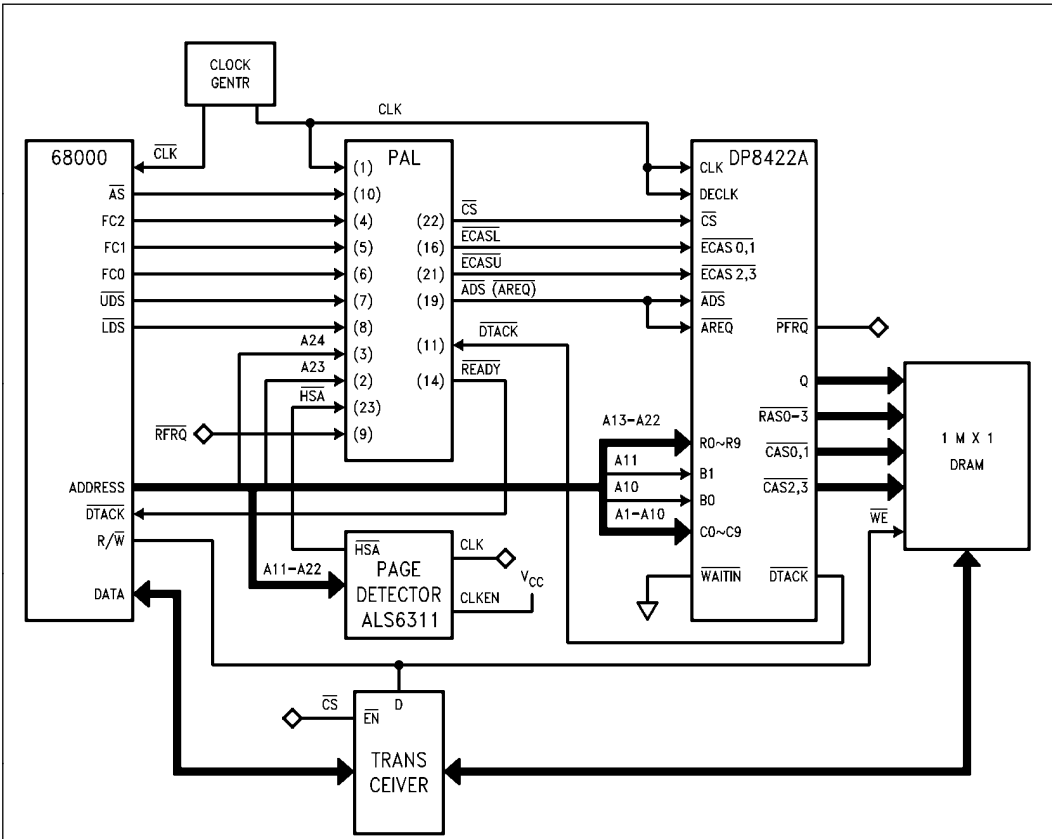
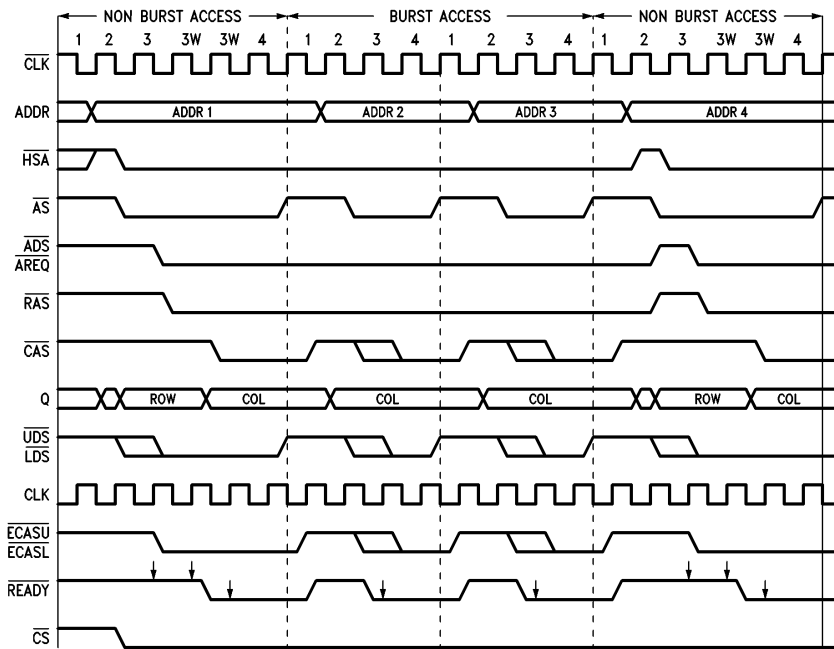


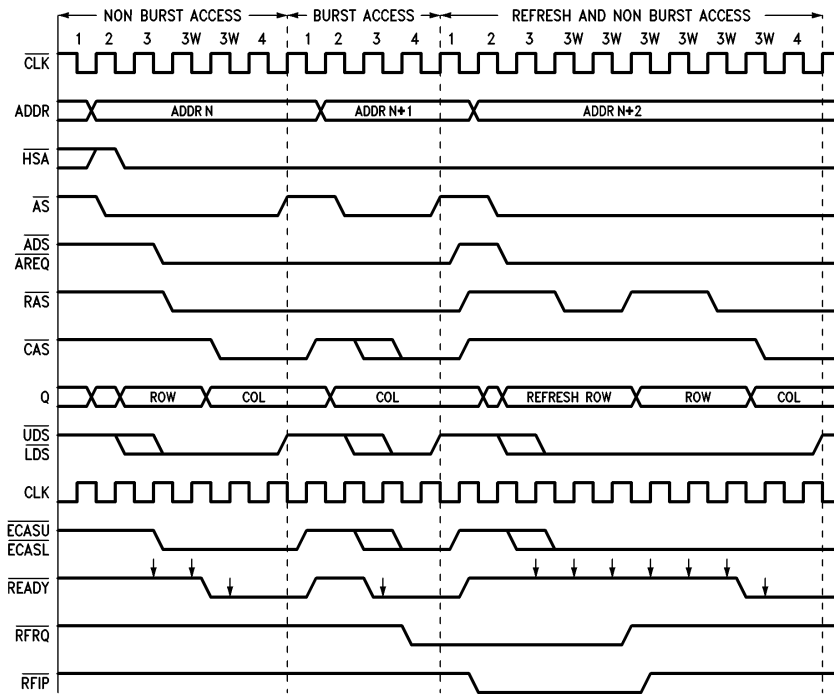
FIGURE 1.2 Schematic Diagram of Interfacing DP8422A/68000 Burst Access to 1M x 1 DRAM

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FIGURE 2. Timing Diagram of Burst and Nonburst Access



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FIGURE 3. Timing Diagram of Refresh, Burst and Nonburst Access

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National Semiconductor Corporation
 2900 Semiconductor Drive
 P.O. Box 58090
 Santa Clara, CA 95052-8090
 Tel: 1(800) 272-9959
 TWX: (910) 339-9240

National Semiconductor GmbH
 Livny-Gargan-Str. 10
 D-82256 Fürstenfeldbruck
 Germany
 Tel: (81-41) 35-0
 Telex: 527849
 Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
 Sumitomo Chemical
 Engineering Center
 Bldg. 7F
 1-7-1, Nakase, Mihama-Ku
 Chiba-City,
 Ciba Prefecture 261
 Tel: (043) 299-2300
 Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
 Rue Deputado Lacorda Franco
 120-3A
 Sao Paulo-SP
 Brazil 05418-000
 Tel: (55-11) 212-5066
 Telex: 391-1131931 NSBR BR
 Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
 Building 16
 Business Park Drive
 Monash Business Park
 Nottingham, Melbourne
 Victoria 3168 Australia
 Tel: (3) 558-9999
 Fax: (3) 558-9998

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