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TECHNICAL DATA

Addendum to
MC68HC000
Low Power HCMOS
16-/32-Bit Microprocessor

This addendum applies to the *MC68HC000 Low Power HCMOS 16-/32-Bit Microprocessor Technical Summary* (BR275/D). The following preliminary tables correspond to the AC Electrical Characteristics of the new 16 MHz version of the MC68HC000 microprocessor available from Motorola. These tables are provided as additions to the current MC68HC000 AC Electrical Specifications.

PRELIMINARY AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING

Num.	Characteristic	Symbol	16 MHz		Unit
			Min	Max	
	Frequency of Operation	f	8	16.67	MHz
1	Clock Period	t_{cyc}	60	125	ns
2,3	Clock Pulse Width Measured From 1.5 V to 1.5 V	t_{CL}, t_{CH}	27	62.5	ns
4,5	Clock Rise and Fall Times	t_{Cr}, t_{Cf}	—	5	ns

PRELIMINARY AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

Num.	Characteristic	Symbol	16 MHz		Unit
			Min	Max	
6	Clock Low to Address Valid	t_{CLAV}	—	30	ns
6A	Clock High to FC Valid	t_{CHFCV}	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	50	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	t_{CHSL}	3	30	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	t_{AVSL}	15	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	t_{FCVSL}	45	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	t_{CLSH}	3	30	ns
13[2]	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	t_{SHAFI}	15	—	ns
14[2]	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SL}	120	—	ns
14A[2]	$\overline{DS}$ Width Asserted, Write	t_{DSL}	60	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	t_{SH}	60	—	ns

— Continued —

PRELIMINARY AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Continued)

Num.	Characteristic	Symbol	16 MHz		Unit
			Min	Max	
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	50	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	t_{SHRH}	15	—	ns
18[1]	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	30	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	30	ns
20A[2,6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	t_{ASRV}	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	t_{AVRL}	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	t_{FCVRL}	30	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RLSL}	30	—	ns
23	Clock Low to Data-Out Valid	t_{CLDO}	—	30	ns
25[2]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid (Write)	t_{SHDOI}	15	—	ns
26[2]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DOSL}	15	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time on Read)	t_{DICL}	5	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	t_{SHDAH}	0	110	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	ns
29A	$\overline{AS}$, $\overline{DS}$ Negated to Data-In High Impedance	t_{SHDZ}	—	90	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	t_{SHBEH}	0	—	ns
31[2,5]	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time)	t_{DALDI}	—	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr,f}$	—	150	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	0	30	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	0	30	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	t_{BRLGL}	1.5	3.5	Clks
36[7]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	t_{BRHGH}	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	1.5	3.5	Clks
37A[8]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	t_{GALBRH}	10	1.5	ns/Clks
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	50	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	Clks
40	Clock Low to VMA Asserted	t_{CLVML}	—	50	ns
41	Clock Low to E Transition	t_{CLET}	—	35	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	ns
43	VMA Asserted to E High	t_{VMLEH}	80	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to VPA Negated	t_{SHVPH}	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	10	—	ns
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	Clks
47[5]	Asynchronous Input Setup Time	t_{ASI}	5	—	ns
48[2,3]	$\overline{BERR}$ Asserted to $\overline{DTACK}$ Asserted	t_{BELDAL}	10	—	ns
49[9]	$\overline{AS}$, $\overline{DS}$ Negated to E Low	t_{SHEL}	−35	35	ns
50	E Width High	t_{EH}	220	—	ns
51	E Width Low	t_{EL}	340	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	10	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RLDBD}	0	—	ns

— Continued —

PRELIMINARY AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Concluded)

Num.	Characteristic	Symbol	16 MHz		Unit
			Min	Max	
56[4]	$\overline{HALT}/\overline{RESET}$ Pulse Width	t_{HRPW}	10	—	Clks
57	BGACK Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{GASD}	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, VMA Driven	t_{GAFD}	1	—	Clks
58[7]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{RHSD}	1.5	—	Clks
58A[7]	$\overline{BR}$ Negated to FC, VMA Driven	t_{RHFD}	1	—	Clks

NOTES:

1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For powerup, the MC68HC000 must be held in the reset state for 100 milliseconds to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$-asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 nanoseconds from the values given in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and x$\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

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