National Semiconductor

PRELIMINARY

DP84422 Dynamic RAM Controller Interface Circuit for the 68000/008/010 CPU(s)

General Description

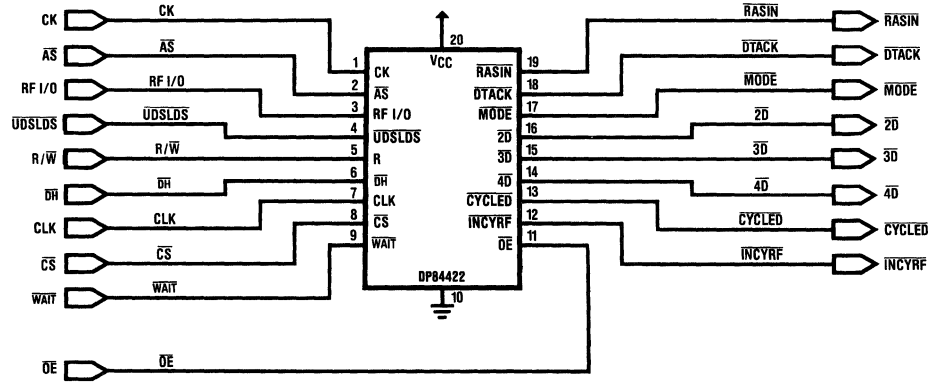
The DP84422 is a new Programmable Array Logic (PAL®) device, that replaces the DP84322, designed to allow an easy interface between the Motorola 68000 family of processors and the National Semiconductor DP8409A, DP8429, or DP8419 DRAM controller.

The new DP84422 supplies all the control signals needed to perform memory read, write, read modify write (as in the Test and Set, "TAS", instruction), and refresh and work with the 68000 family of processors up to 12.5 MHz. Logic is also included to insert WAIT states, if wanted, into the microprocessor READ or WRITE cycles when using fast CPUs.

Features

- Provides a 3-chip solution for the 68000 family, dynamic RAM interface (DP8409A or DP8419, DP84422, and clock divider).
- Works with all 68000 family speed versions up to 12.5 MHz.—(68008; 68000; and 68010).
- Operation of 68000 processor at 10 MHz with no WAIT states.
- Controls DP8409A or DP8419 Mode 5 accesses, hidden refreshes and Mode 1 Forced Refreshes automatically.
- Inserts WAIT states in READ or WRITE cycles automatically depending on when $\overline{WAIT}$ is low, or if chip select becomes active during a forced Refresh cycle.
- Uses a standard National Semiconductor PAL part (DMPAL16R4A).
- The PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new very high speed PALs ("B" PAL parts).

Connection Diagram



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Order Number DP84422J or DP84422N
See NS Package J20A or N20A

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Operating	Programming
Supply Voltage, V_{CC}	7V	12V
Input Voltage	5.5V	12V

	Operating	Programming
Off-State Output Voltage	5.5V	12V
Storage Temperature Range	−65°C to +150°C	

Recommended Operating Conditions

Symbol	Parameter		Commercial			Units
			Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
t_w	Width of Clock	Low	15	10		ns
		High	15	10		
t_{su}	Setup Time from Input or Feedback to Clock		25	16		ns
t_h	Hold Time		0	−10		ns
T_A	Operating Free-Air Temperature		0	25	75	°C
T_C	Operating Case Temperature					°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −3.2 mA COM	2.4	2.8		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 24 mA COM		0.3	0.5	V
I_{OZH}	Off-State Output Current	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.4V			−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.02	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max			120	180	mA

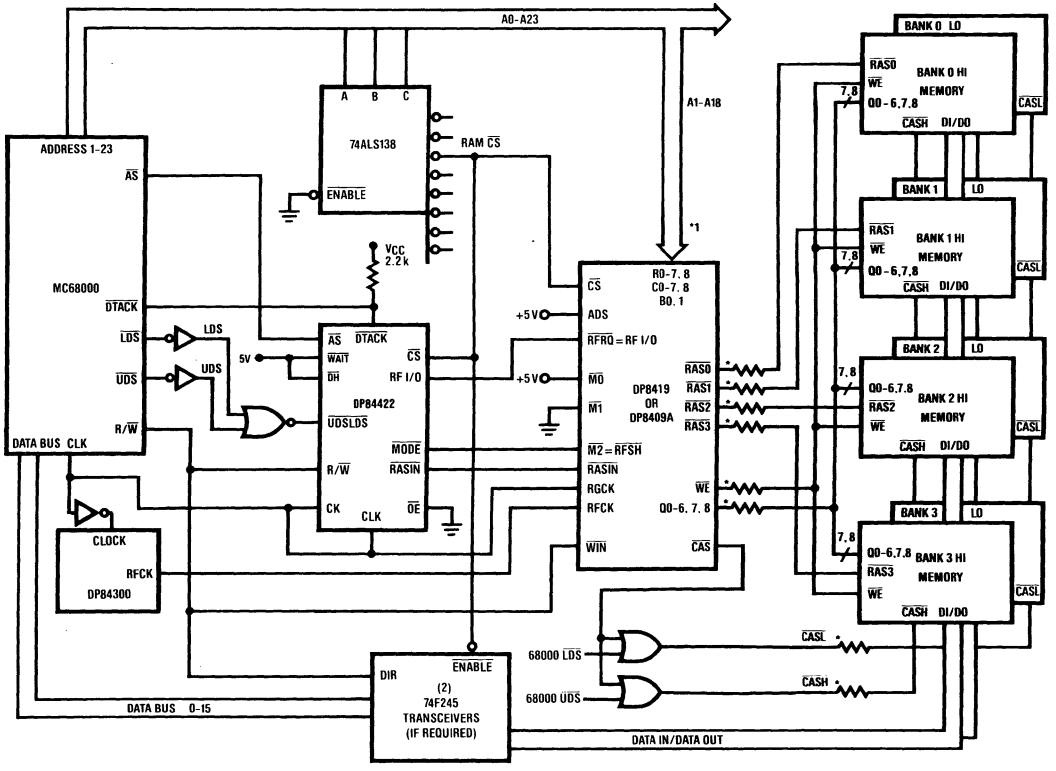
Switching Characteristics Over Recommended Ranges of Temperature and V_{CC}

V_{CC} = 5V ± 10% Commercial: T_A = 0 to 75°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions R1, R2	Commercial			Units
			Min	Typ	Max	
t_{PD}	Input or Feedback to Output	CL = 50 pF		15	25	ns
t_{CLK}	Clock to Output of Feedback			10	15	ns
t_{PZX}	Pin 11 to Output Enable			10	20	ns
t_{PXZ}	Pin 11 to Output Disable	C_L = 5 pF		11	20	ns
t_{PZX}	Input to Output Enable	C_L = 50 pF		10	25	ns
t_{PXZ}	Input to Output Disable	C_L = 5 pF		13	25	ns
f_{MAX}	Maximum Frequency		25	30		ns

V_{CC} = Max. at minimum temperature

ALL IC'S DECOUPLED
* SERIES DAMPING RESISTERS
*1 TIE UNUSED ADDRESS LINES TO V_{CC}
This circuit provides direct support of the 68000 Test and Set Instruction using PAGE MODE DRAMs.



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Mnemonic Description

INPUT SIGNALS

1) "CLK", "CK" This is the 68000 CPU clock.
2) "$\overline{AS}$" This is the 68000 address strobe pin. This signal also tells when the 68000 is in a cycle.
3) "$\overline{CS}$" This is the chip select signal for the DP8409A.
4) "R" This is the READ/$\overline{WRITE}$ pin from the 68000.
5) "RFIO" This is the RFIO, used as refresh request, from the DP8409A.
6) "$\overline{WAIT}$" This pin allows the insertion of 1 WAIT state in a $\overline{CS}$ Access cycle if low. As an example; if the user wants 1 WAIT state in READ accesses but 0 WAIT states in WRITE accesses he can invert the "R/$\overline{W}$" input to this input.
7) "$\overline{UDSLDS}$" This input was produced by inverting the two terms $\overline{UDS}$ and $\overline{LDS}$ and then logically "NOR"ing them together. This input is low whenever one or both $\overline{UDS}$ or $\overline{LDS}$ are low. This pin is used in order to support the 68000 "TAS" instruction. This signal is used in the "$\overline{DTACK}$" PAL output.
8) "$\overline{DH}$" This input allows the user to disable the DP8409A/19 hidden refresh, when low, provided he also ties "$\overline{CS}$" low on the DP8409A/19. When this input is low "$\overline{RASIN}$" is only brought low when a "$\overline{CS}$" access ("$\overline{CS}$" input to PAL low) is in progress
9) "$\overline{OE}$" Must be tied low to enable DP84422 outputs.

OUTPUT SIGNALS

1) "$\overline{CYCLED}$" This signal goes low once a hidden refresh or an access has been done as indicated by $\overline{2DLY}$ and $\overline{3DLY}$ being low. This signal goes high once the cycle is over as indicated by $\overline{AS}$ going high. See also "$\overline{DH}$ input
2) "$\overline{RASIN}$" This signal goes low following $\overline{AS}$ during an access or hidden refresh. See also "$\overline{DH}$" input.
3) "$\overline{DTACK}$" This signal causes WAIT states to be inserted into the 68000 processor cycles if it is not low a setup time before S4 falling clock edge.
4) "$\overline{INCYRF}$" This signal indicates that an access has been requested during a forced refresh cycle. This signal is used to insert WAIT states during the forementioned condition or to prevent a "non-$\overline{CS}$" access cycle from automatically starting.
5) "$\overline{MODE}$" This signal is used to pull the DP8409A pin M2 low in order to go to mode 1 to do a forced refresh.
6) "$\overline{2DLY}$" This signal is an internal delay.
7) "$\overline{3DLY}$" This signal is an internal delay.
8) "$\overline{4DLY}$" This signal is an internal delay.

Functional Description

The following description applies to both the DP8409A, DP8429, and the DP8419 dynamic RAM controllers.

A memory cycle starts when chip select ($\overline{CS}$) and address strobe ($\overline{AS}$) are true. $\overline{RASIN}$ is supplied from the DP84422 to the DP8409A dynamic RAM controller, which then supplies a $\overline{RAS}$ signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8409A switches the address outputs to the column address. The DP8409A then supplies the required $\overline{CAS}$ signal to the DRAM. In order to do byte operations it is suggested that the user provide external logic, as shown in the system block diagram, to produce a HIGH CAS and a LOW CAS. To differentiate between a READ and a WRITE, the R/$\overline{W}$ signal from the CPU is used.

A refresh cycle is started by one of two conditions. The refresh cycle caused by the first condition is called a hidden refresh. This occurs when refresh clock (RFCK) is high, $\overline{CS}$ is not true, and $\overline{RASIN}$ goes low. Here the CPU is accessing something else in the system and the DRAM can be refreshed at that time, thereby being transparent to the CPU. The second type of refresh is called forced refresh. This occurs if no hidden refresh was performed while RFCK was high. When RFCK transitions low a refresh request (RFRQ) is generated. If there is not a DRAM access in progress the DP84422 will force a refresh by putting the DP8409A into mode 1 (automatic forced refresh mode). If the CPU tries to access the DRAM during a forced refresh cycle WAIT states will be inserted into its cycles until the forced refresh is over and the DRAM $\overline{RAS}$ precharge time has been met. Then the pending DRAM access will be allowed to take place.

The DP84422 also allows forced refreshes to take place during long accesses of other devices. For instance, if EEPROM takes several microseconds to write to, the DRAM will still be refreshed while that access is in progress.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories or allow time to generate parity. This is accomplished by inserting a WAIT state into the processor access cycle. The DP84422 can insert WAIT states into either READ cycles, WRITE cycles, READ MODIFY WRITE cycles, or both READ and WRITE cycles or the READ and WRITE portion of a READ MODIFY WRITE cycle. The extra WAIT state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

During a Test and Set instruction $\overline{CAS}$ is generated twice while $\overline{RAS}$ is low. In order for this instruction to execute properly Page Mode DRAMs must be used.

System Interface Description

All members of the Motorola 68000 family of processors are able to use the DP84422.

$\overline{RASIN}$ during a READ cycle will always start at the beginning of the "S3" processor cycle. The user must guarantee that $\overline{CS}$ is valid a minimum of 34 ns before $\overline{RASIN}$ becomes valid, unless the PAL "$\overline{DH}$" input is low and the DP8409A/19 "$\overline{CS}$" input is tied low (hidden refresh disabled).

System Interface Description (Continued)

Several critical parameters in this application involve the input system CLOCK and the ADDRESS STROBE, $\overline{AS}$. These parameters become most critical at higher frequencies (10 MHz and above) where it is suggested that they are directly connected to the corresponding pins of the Motorola 68000 family ICs.

This section of the data sheet goes through the calculation of the "t_{RAC}" ($\overline{RAS}$ access time) and "t_{CAC}" ($\overline{CAS}$ access time) required by the DRAM for the 68000 family CPUs to operate at a particular clock frequency without introducing wait states into the processor access cycles. Both "t_{RAC}" and "t_{CAC}" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "t_{RAC}" and "t_{CAC}" parameters calculated. In order to determine the "t_{RAC}" and "t_{CAC}" needed the DP8419 and fast PALs ("B" type PALs) timing parameters were used. If the user is using the DP8408A/09A or a slower PAL device he should substitute their respective delays into the equation below.

Most all of the calculations contained in this note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from RAH exceeded 200 ns. This is because DRAMs can be found with row access times up to 150 ns that require only 15 ns row address hold times.

The calculated "t_{RAC}" and "t_{CAC}" may differ from the actual system values depending upon the external circuitry used to produce "$\overline{CASH}$" and "$\overline{CASL}$". The DP8409A/19 "$\overline{RASIN}$–$\overline{CAS}$" low will be approximately 10–15 ns less than the value given in the data sheet because of the small loading on the DP8409A/19 "$\overline{CAS}$" output. The external circuitry needed to produce "$\overline{CASH, L}$" should be loaded such that the column address (from DP8409A/19 is valid when "$\overline{CASH, L}$" goes low. For this reason "$\overline{RASIN}$–$\overline{CASH, L}$" may be longer than the value used in the "t_{RAC}, t_{CAC}" calculations, and therefore may give a smaller "t_{RAC}, t_{CAC}" then was calculated.

EXAMPLE DRAM TIMING CALCULATIONS

A) 8 MHz 68000, No WAIT States

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 125 + 60 + 15 = 220 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ – $\overline{CAS}$ low) – 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 15 ns minimum

"t_{RAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (min) – #1 – #2 – #4 – #5
= 125 + 125 + 125 + 55 – 200 – 20 – 7 – 15
= 188 ns

"t_{CAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (min) – #1 – #3 – #4 – #5
= 125 + 125 + 125 + 55 – 200 – 77 – 7 – 15
= 131 ns

Therefore the DRAM chosen should have a "t_{RAC}" less than or equal to 188 ns and a "t_{CAC}" less than or equal to 131 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one and one half clock periods = 125 + 55 = 180 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 125 + 55 + 35 = 215 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods – 5 ns (maximum $t_{RPDL} - t_{RPDH}$ for the DP8409-2) = 250 – 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods – 70 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 250 – 70 = 180 ns.

The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times, the $\overline{CAS}$ pulse width, and the $\overline{RAS}$ pulse width would be increased by one clock period (125 ns in this case). A WAIT state in WRITE cycles would just increase the $\overline{RAS}$ and $\overline{CAS}$ precharge by one clock period.

B) 10 MHz 68000, No WAIT states

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 100 + 55 + 15 = 170 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ – $\overline{CAS}$ low) – 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"t_{RAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (min) – #1 – #2 – #4 – #5
= 100 + 100 + 100 + 45 – 170 – 20 – 7 – 10
= 138 ns

"t_{CAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) – S6 (min) – #1 – #3 – #4 – #5
= 100 + 100 + 100 + 45 – 170 – 77 – 7 – 10
= 81 ns

Therefore the DRAM chosen should have a "t_{RAC}" less than or equal to 138 ns and a "t_{CAC}" less than or equal to 81 ns. Standard 120 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one and one half clock periods = 100 + 45 = 145 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8419) = 100 + 45 + 35 = 180 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods – 5 ns (maximum $t_{RPDL} - t_{RPDH}$ for the DP8419) = 200 – 5 = 195 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods – 50 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8419) = 200 – 50 = 150 ns.

The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times, the $\overline{CAS}$ pulse width, and the $\overline{RAS}$ pulse width would be increased by one clock period (100 ns in this case). A WAIT state in WRITE cycles would just increase the $\overline{RAS}$ and $\overline{CAS}$ precharge by one clock period.

Interpreting the DP84422 PAL Equations

The boolean equations for the DP84422 were written using the standard PALASM™ format. In other words the equation: "IF (VCC) RASIN = INCY *$\overline{\text{MODE}}$*4D*$\overline{\text{R}}$" will mean;

The output "$\overline{\text{RASIN}}$" (see pin list for DP84422) will be active low (inverted $\overline{\text{RASIN}}$) when the output "$\overline{\text{INCY}}$" is low (making INCY high) AND the output "$\overline{\text{MODE}}$" is high AND the output "$\overline{\text{4D}}$" is low (making 4D high) and the input R/$\overline{\text{W}}$ is low (making $\overline{\text{R}}$ high).

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PAL16R4A ; FAST PAL
NEW PAL FOR THE MOTOROLA 68000 PROCESSOR
(WORKS UP TO 12.5MHZ)

CK /AS RFIO /UDSLDS R /DH CLK /CS /WAIT GND
/OE /INCYRF /CYCLED /4DLY /3DLY /2DLY /MODE /DTACK /RASIN VCC

IF (VCC) RASIN =
 CS*/INCYRF*AS*/MODE*4DLY*/CYCLED*/CLK+          ;Start RASIN
 /CS*/INCYRF*AS*/MODE*2DLY*/CYCLED*/DH+          ;RASIN for Hidden RFSH
 CS*INCYRF*AS*/MODE*4DLY*/CYCLED*/CLK+           ;Start RASIN after RFSH
 CS*RASIN*/MODE*AS+                              ;Hold RASIN valid
 RASIN*/MODE*2DLY                                ;Hold RASIN valid

IF (VCC) CYCLED =/MODE*2DLY*3DLY*/4DLY+          ;Start "CYCLED", does not allow
                 CYCLED*AS+                      ;  glitch after refresh
                 /MODE*CYCLED*/CLK+              ;End on rising edge of CLK
                 /CS*AS*/MODE*/2DLY*/3DLY*/4DLY  ;Start during long accesses of other
                                                 ; devices

IF (VCC) INCYRF =MODE*AS+                        ;Set Access during Refresh
                 INCYRF*4DLY*AS                  ;Hold it while 4DLY is low

IF (CS) DTACK = AS*/WAIT*/R*/MODE*/CLK+          ;0 WAIT's for WRITE
        AS*WAIT*/R*/MODE*2DLY*/CLK+              ;1 WAIT for WRITE
        UDSLDS*/WAIT*R*/MODE*/CLK+               ;0 WAIT's for READ
        UDSLDS*WAIT*R*/MODE*2DLY*/CLK+           ;1 WAIT for READ
        DTACK*2DLY*/MODE+                        ;Continue DTACK
        DTACK*AS*RASIN*/MODE*/CYCLED+            ;Continue DTACK
        DTACK*AS*/R*/MODE                        ;Continue DTACK in RMW
                                                 ;  cycle
MODE : = /RFIO*/AS*/CYCLED*/RASIN+               ;For IDLE states or beginning
                                                 ;  states of 68000 cycle
        /CS*/RFIO*AS*CYCLED*/2DLY*/3DLY*/RASIN+  ;For RFSH during long cycles
                                                 ;  of other devices
        MODE*/3DLY+
        MODE*/4DLY
2DLY : = MODE*/4DLY+
        /INCYRF*AS*/CYCLED*/MODE*/3DLY*4DLY+     ;Start 2DLY
        CS*INCYRF*AS*/CYCLED*/MODE*/3DLY*4DLY+   ;Start 2DLY after RFSH
        /MODE*2DLY*/3DLY+
        CS*WAIT*AS*/MODE*2DLY*3DLY*/4DLY+        ;Make 2DLY longer
        CS*AS*/R*CYCLED*/MODE*/2DLY*/3DLY*/4DLY  ;Start second 2DLY for
                                                 ;the TAS instruction
3DLY : = 2DLY*/4DLY
4DLY : = 3DLY+
         /AS*/MODE+
         /CS*/RFIO*AS*CYCLED*/2DLY*/3DLY*/RASIN*/MODE ;Need for beginning of forced refresh to
                                                      ; inhibit "2DLY"
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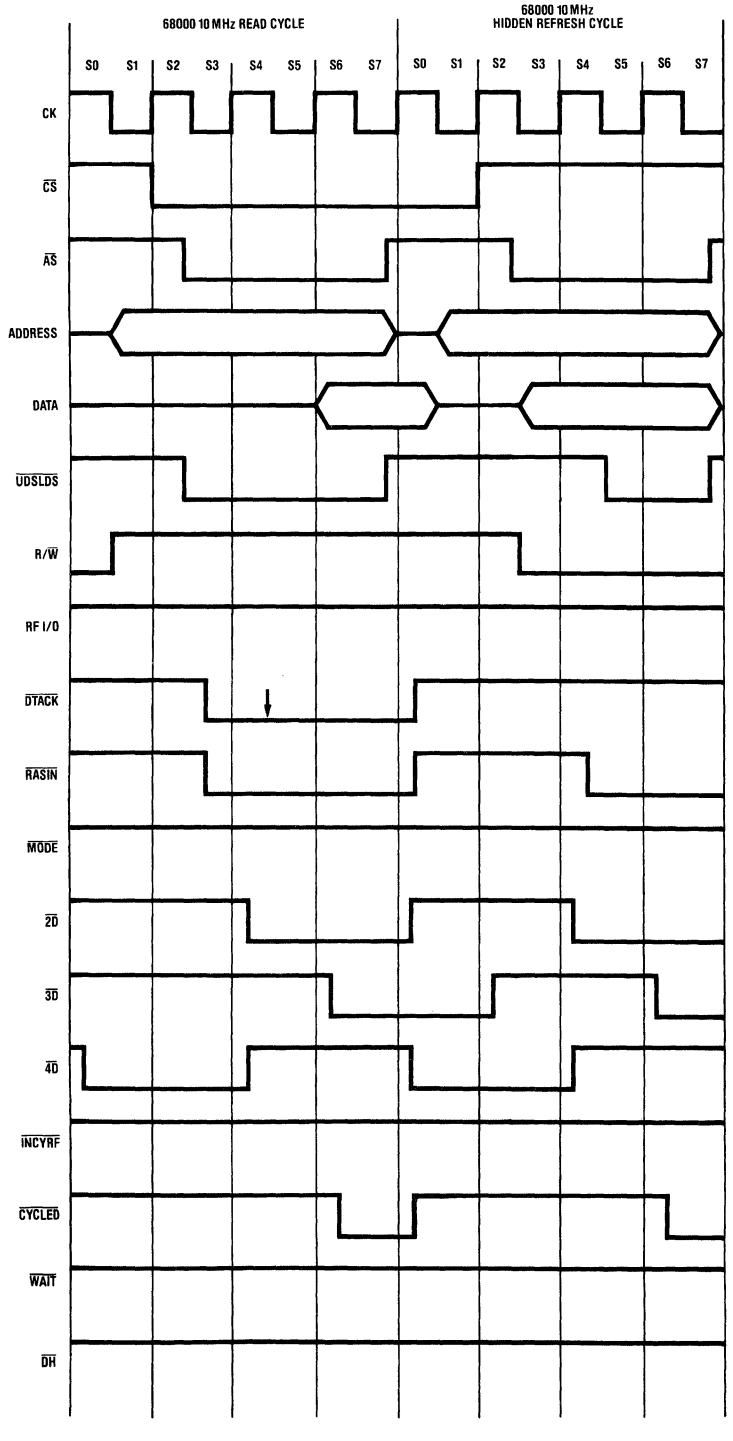
FIGURE 1. Equations for New 68000 PAL That Supports the 68000 "TAS" Instruction

System Timing Diagrams



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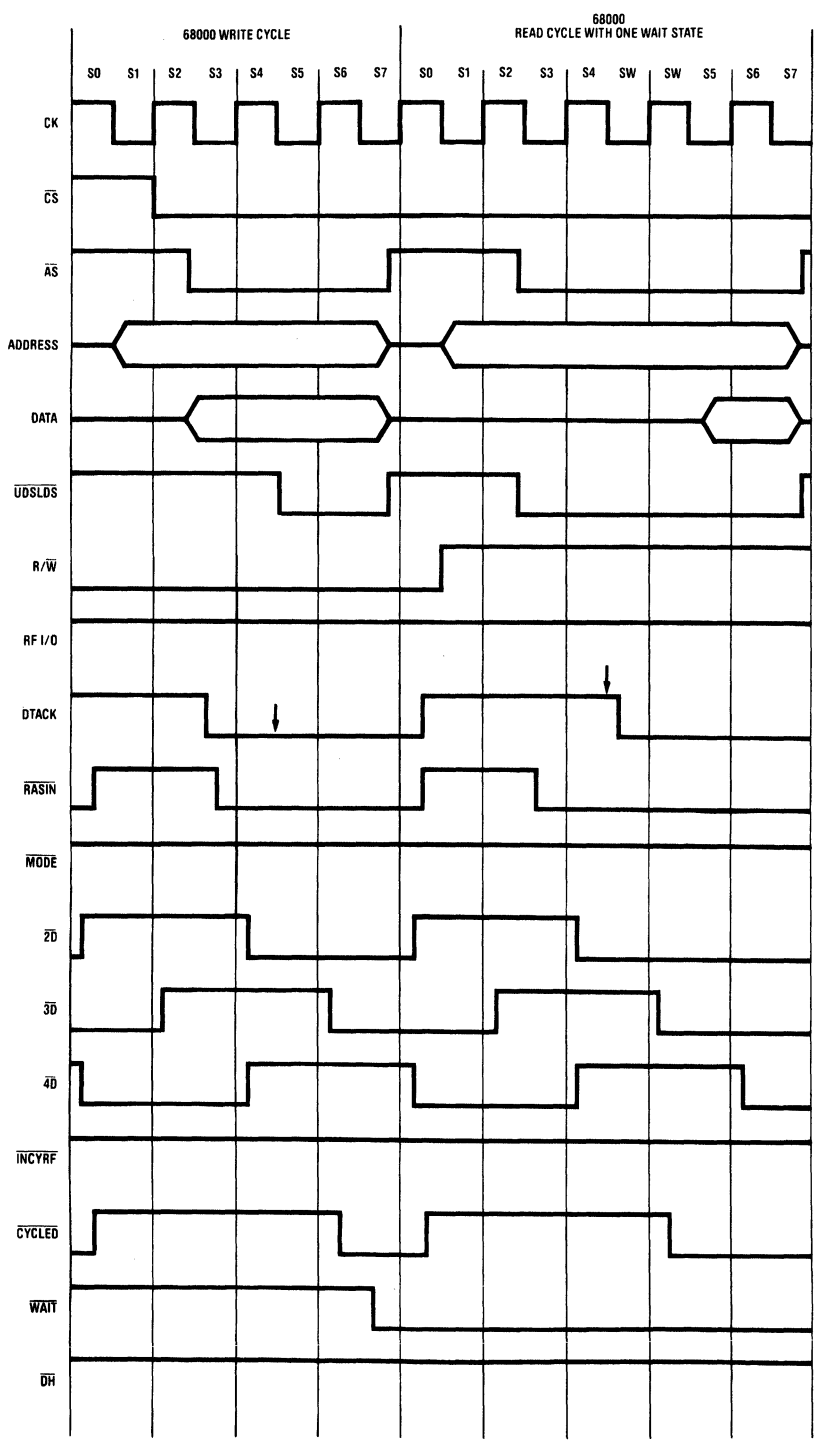
System Timing Diagrams (Continued)



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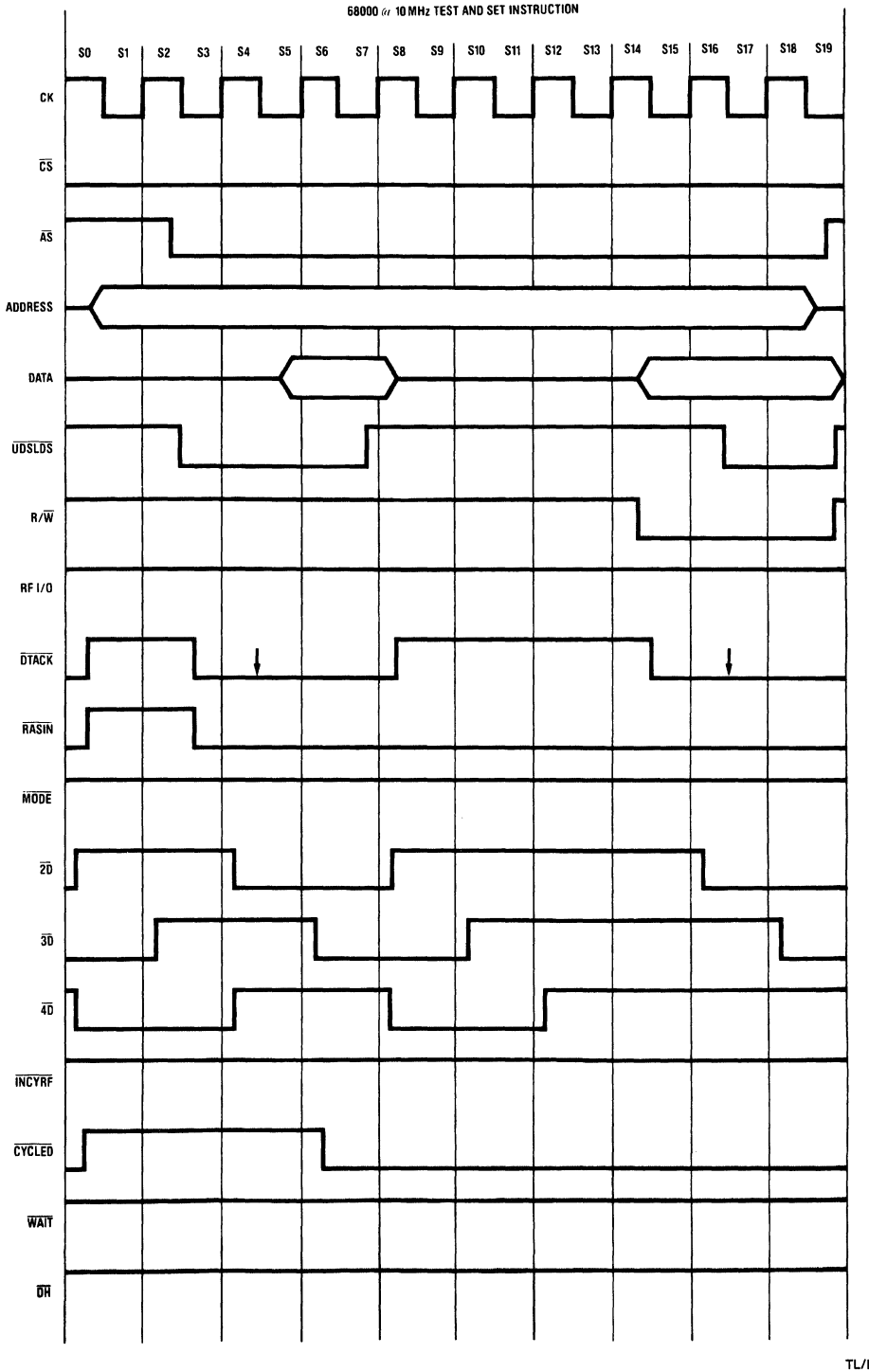
System Timing Diagrams (Continued)



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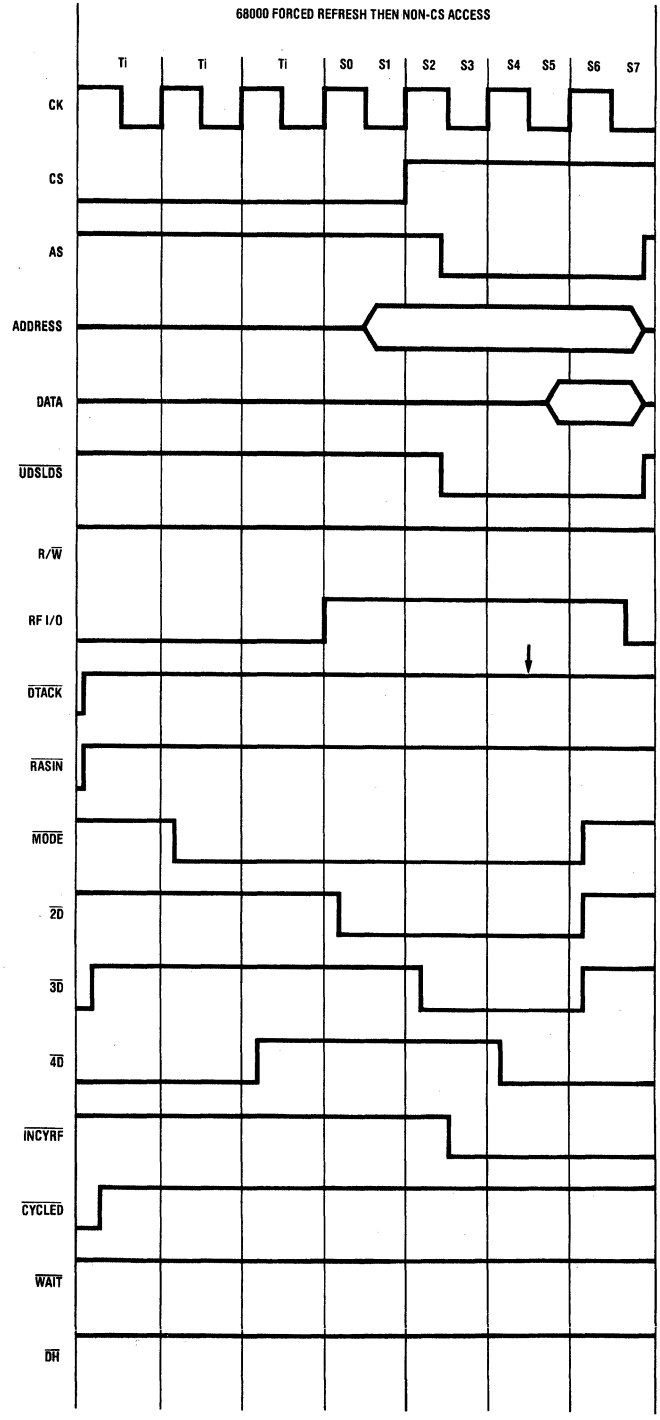
System Timing Diagrams (Continued)



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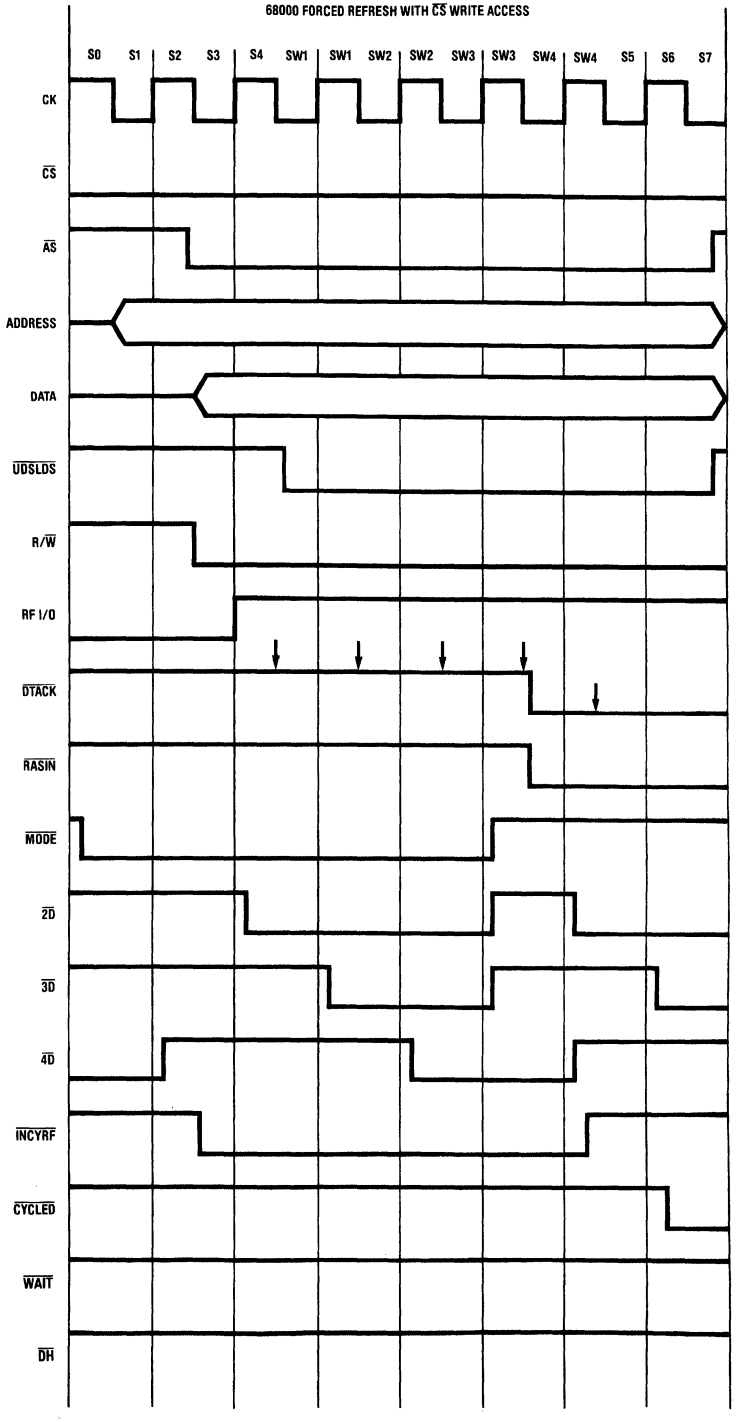
System Timing Diagrams (Continued)



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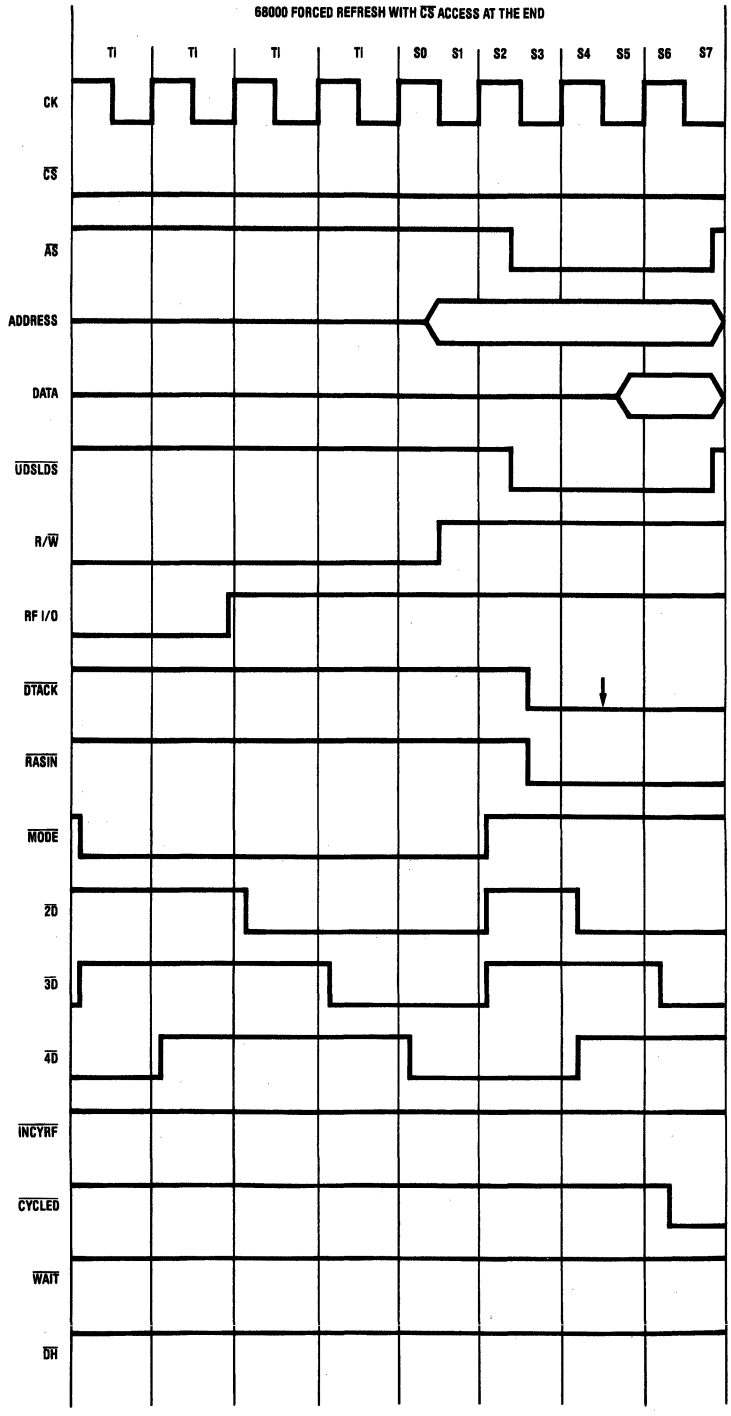
System Timing Diagrams (Continued)



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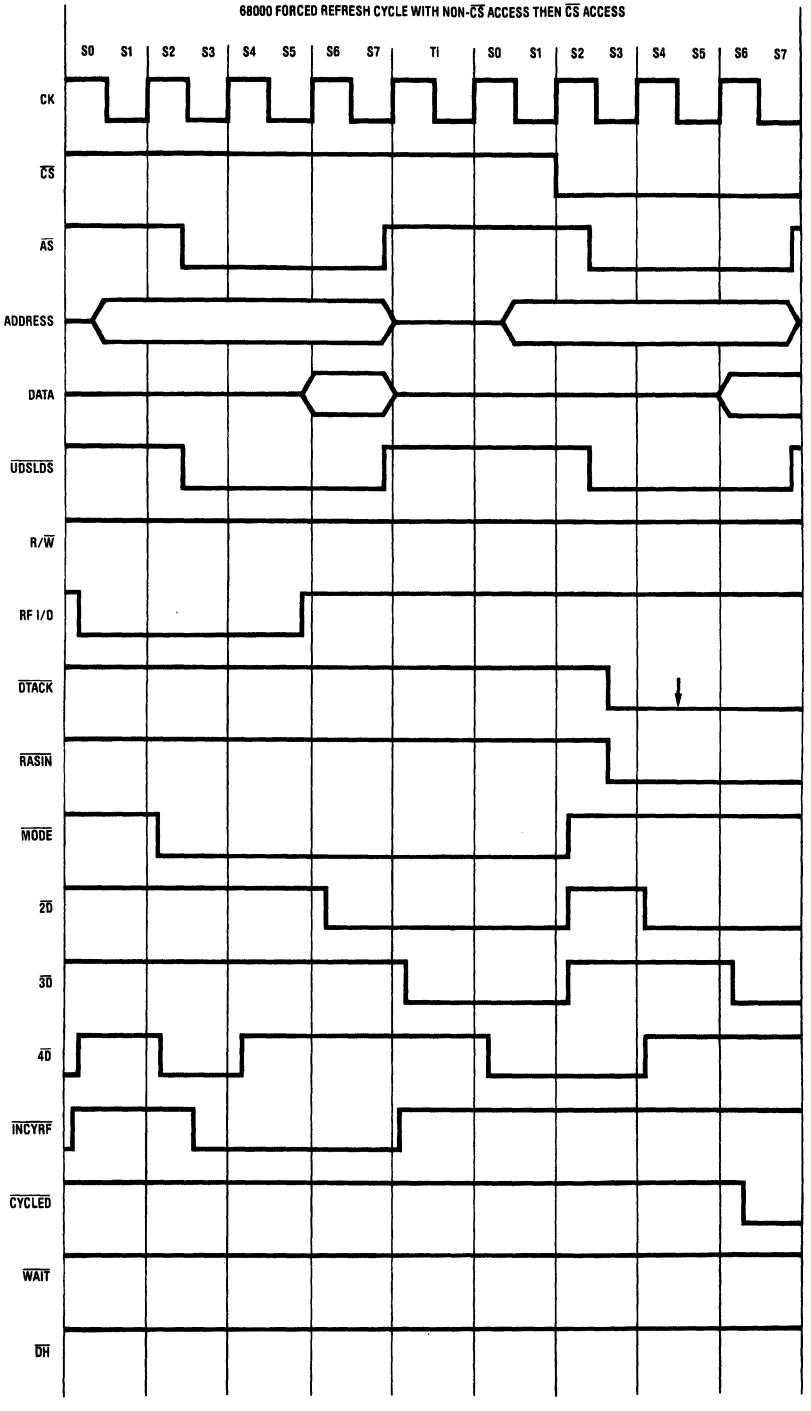
System Timing Diagrams (Continued)



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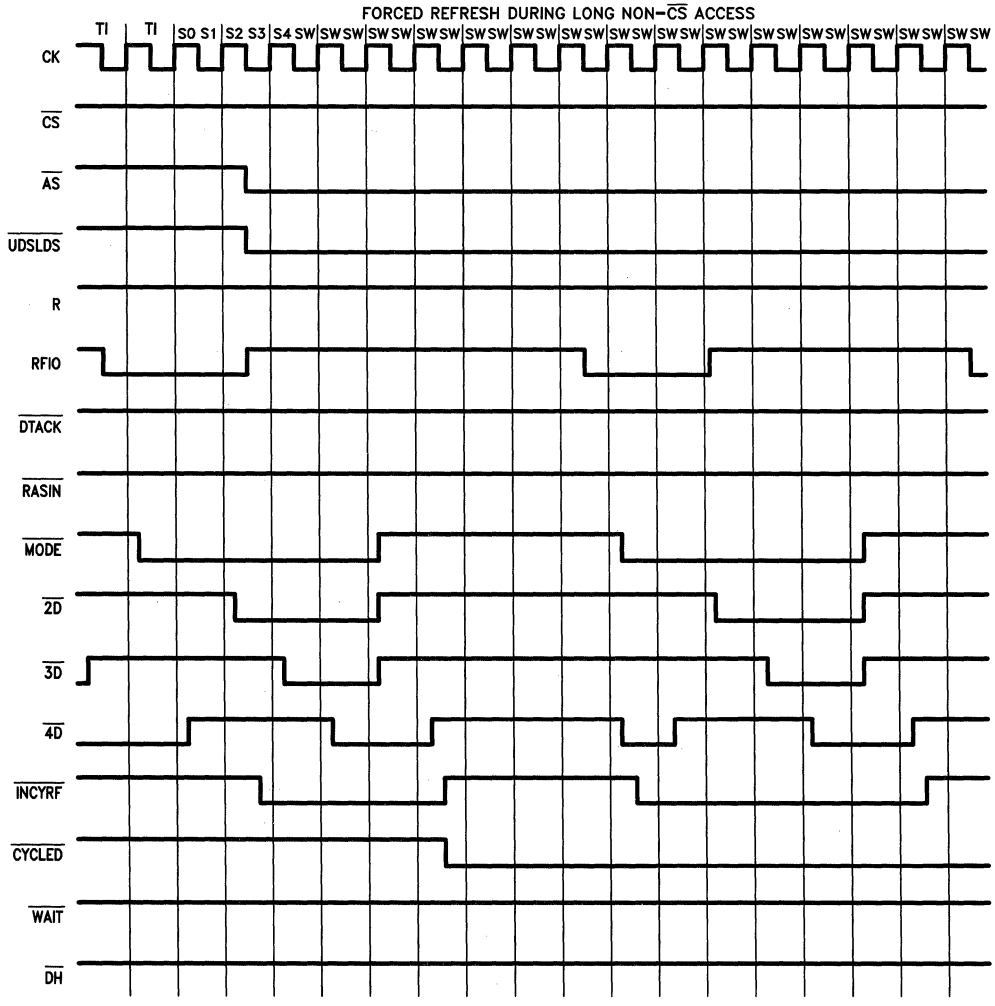
System Timing Diagrams (Continued)



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