

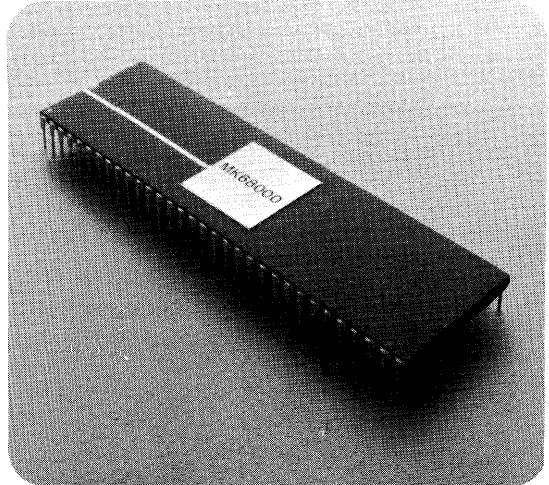


**16-BIT MICROPROCESSOR
MK68000**

Advances in semiconductor technology have provided the capability to place on a single silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The MK68000 is the first of a family of such VLSI microprocessors from Mostek. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

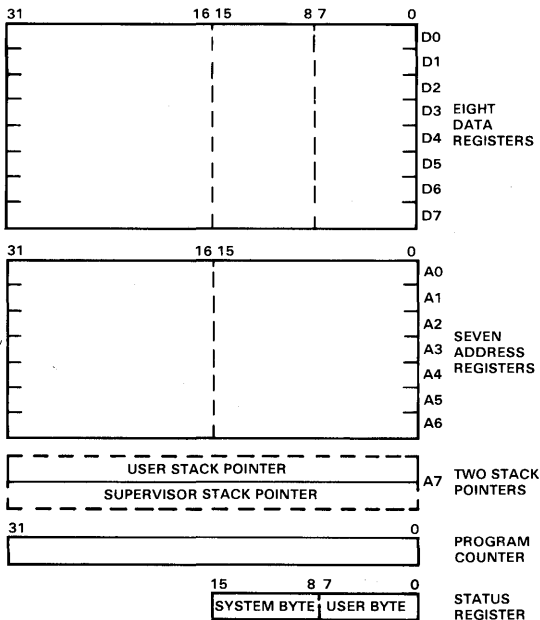
The resources available to the MK68000 user consist of the following:

- 17 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes

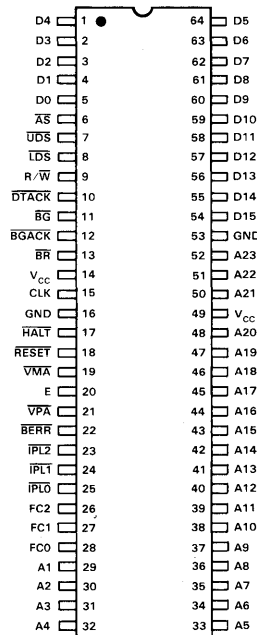


VI

PROGRAMMING MODEL



PIN ASSIGNMENT



As shown in the programming model, the MK68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

A 23-bit address bus provides a memory addressing range of greater than 16 megabytes. This large range of addressing capability, coupled with a memory management unit, allows large, modular programs to be developed and operated without resorting to cumbersome and time consuming software bookkeeping and paging techniques.

The status register contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Word (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 1, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

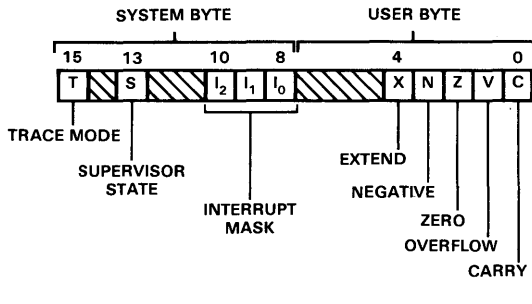
The MK68000 instruction set is shown in Table 2. Some additional instructions are variations, or subsets, of these and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic and expanded operations (through traps).

DATA ADDRESSING MODES

Table 1

Mode	Generation
Register Direct Addressing Data Register Direct Address Register Direct	EA = D _n EA = A _n
Absolute Data Addressing Absolute Short Absolute Long	EA = (Next Word) EA = (Next Two Words)
Program Counter Relative Addressing Relative with Offset Relative with Index and Offset	EA = (PC) + d ₁₆ EA = (PC) + (X _n) + d ₈
Register Indirect Addressing Register Indirect Postincrement Register Indirect Predecrement Register Indirect Register Indirect with Offset Indexed Register Indirect with Offset	EA = (A _n) EA = (A _n), A _n ← A _n + N A _n ← A _n - N, EA = (A _n) EA = (A _n) + d ₁₆ EA = (A _n) + (X _n) + d ₈
Immediate Data Addressing Immediate Quick Immediate	DATA = Next Word(s) Inherent Data
Implied Addressing Implied Register	EA = SR, USP, SP, PC

STATUS REGISTER



NOTES:

EA = Effective Address
 A_n = Address Register
 D_n = Data Register
 X_n = Address or Data Register used as Index Register
 SR = Status Register
 PC = Program Counter
 () = Contents of
 d₈ = Eight-bit Offset (displacement)

d₁₆ = Sixteen-bit Offset (displacement)
 N = 1 for Byte, 2 for Word, and 4 for Long Word. If A_n is the Stack Pointer and the operand size is byte, N = 2 to keep the Stack Pointer on a word boundary.
 ← = Replaces

INSTRUCTION SET

Table 2

Mnemonic	Description	Mnemonic	Description	Mnemonic	Description
ABCD	Add Decimal with Extend	EOR	Exclusive Or	PEA	Push Effective Address
ADD	Add	EXG	Exchange Registers	RESET	Reset External Devices
AND	Logical And	EXT	Sign Extend	ROL	Rotate Left without Extend
ASL	Arithmetic Shift Left	JMP	Jump	ROR	Rotate Right without Extend
ASR	Arithmetic Shift Right	JSR	Jump to Subroutine	ROXL	Rotate Left with Extend
B _{CC}	Branch Conditionally	LEA	Load Effective Address	ROXR	Rotate Right with Extend
BCHG	Bit Test and Change	LINK	Link Stack	RTE	Return from Exception
BCLR	Bit Test and Clear	LSL	Logical Shift Left	RTR	Return and Restore
BRA	Branch Always	LSR	Logical Shift Right	RTS	Return from Subroutine
BSET	Bit Test and Set	MOVE	Move	SBCD	Subtract Decimal with Extend
BSR	Branch to Subroutine	MOVEM	Move Multiple Registers	S _{CC}	Set Conditional
BTST	Bit Test	MOVEP	Move Peripheral Data	STOP	Stop
CHK	Check Register Against Bounds	MULS	Signed Multiply	SUB	Subtract
CLR	Clear Operand	MULU	Unsigned Multiply	SWAP	Swap Data Register Halves
CMP	Compare	NBCD	Negate Decimal with Extend	TAS	Test and Set Operand
DB _{CC}	Test Condition, Decrement and Branch	NEG	Negate	TRAP	Trap
DIVS	Signed Divide	NOP	No Operation	TRAPV	Trap on Overflow
DIVU	Unsigned Divide	NOT	One's Complement	TST	Test
		OR	Logical Or	UNLK	Unlink

VI

VARIATIONS OF INSTRUCTION TYPES

Table 3

Instruction Type	Variation	Description	Instruction Type	Variation	Description
ADD	ADD	Add	MOVE	MOVE	MOVE
	ADDA	Add Address		MOVEA	Move Address
AND	ADDQ	Add Quick	MOVEQ	Move Quick	
	ADDI	Add Immediate	MOVE from SR	Move from Status Register	
	ADDX	Add with Extend	MOVE to SR	Move to Status Register	
	AND	Logical And	MOVE to CCR	Move to Condition Codes	
	ANDI	And Immediate	MOVE USP	Move User Stack Pointer	
	ANDI to CCR	AND Immediate to Condition Codes			
	ANDI to SR	AND Immediate to Status Register			
CMP	CMP	Compare	NEG	NEG	Negate
	CMPA	Compare Address	NEGX	Negate with Extend	
	CMPM	Compare Memory	OR	OR	Logical Or
CMPI	Compare Immediate	ORI		Or Immediate	
			ORI to CCR	Or Immediate to Condition Codes	
			ORI to SR	OR Immediate to Status Register	
EOR	EOR	Exclusive Or	SUB	SUB	Subtract
	EORI	Exclusive Or Immediate		SUBA	Subtract Address
	EORI to CCR	Exclusive OR Immediate to Condition Codes		SUBI	Subtract Immediate
	EORI to SR	Exclusive OR Immediate to Status Register		SUBQ	Subtract Quick
			SUBX	Subtract with Extend	

DATA ORGANIZATION AND ADDRESSING CAPABILITIES

The following paragraphs describe the data organization and addressing capabilities of the MK68000.

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. All explicit instructions support byte, word or long word operands. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31.

When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high-order portion is neither used nor changed.

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32 bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte

having an even address the same as the word, as shown in Figure 1. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address $n + 2$.

The data types supported by the MK68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 2.

ADDRESSING

Instructions for the MK68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

Register Specification - the number of the register is given in the register field of the instruction.

Effective Address - use of the different effective address modes.

Implicit Reference - the definition of certain instructions implies the use of specific registers.

INSTRUCTION FORMAT

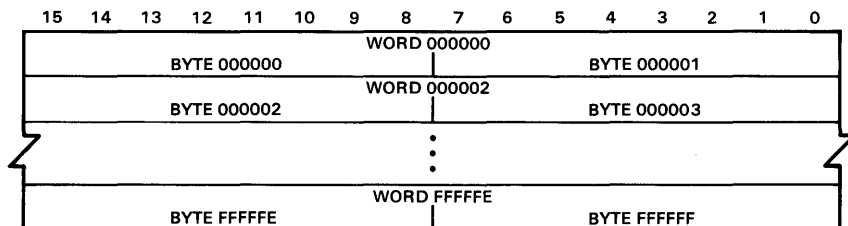
Instructions are from one to five words in length, as shown in Figure 3. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

PROGRAM/DATA REFERENCES

The MK68000 separates memory references into two classes: program references, and data references. Program references, as the name implies, are references to that section of memory that contains the program being

WORD ORGANIZATION IN MEMORY

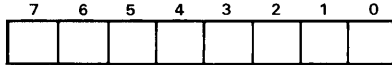
Figure 1



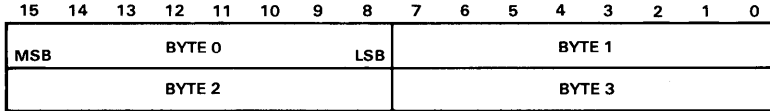
DATA ORGANIZATION IN MEMORY

Figure 2

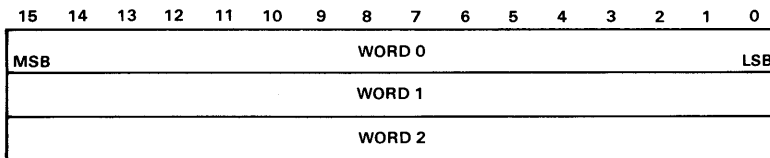
BIT DATA
1 BYTE = 8 BITS



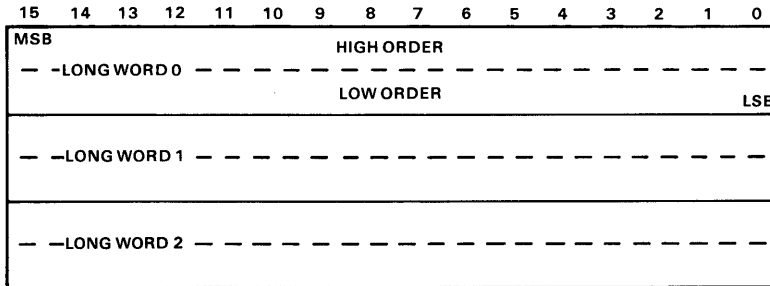
INTEGER DATA
1 BYTE = 8 BITS



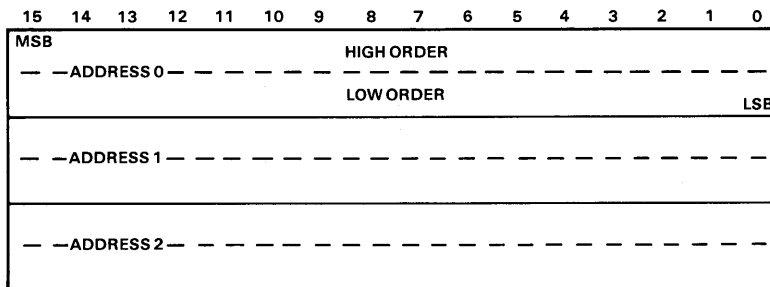
1 WORD = 16 BITS



1 LONG WORD = 32 BITS

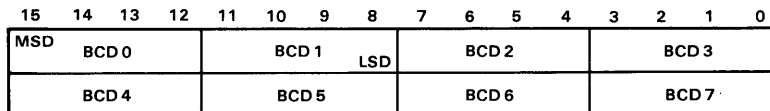


ADDRESSES
1 ADDRESS = 32 BITS



MSB = Most Significant Bit
LSB = Least Significant Bit

DECIMAL DATA
2 BINARY CODED DECIMAL DIGITS = 1 BYTE



MSD = Most Significant Digit
LSD = Least Significant Digit



executed. Data references refer to that section of memory that contains data. Generally, operand reads are from the data space. All operand writes are to the data space.

REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 4 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 3. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES

These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register

specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES

These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

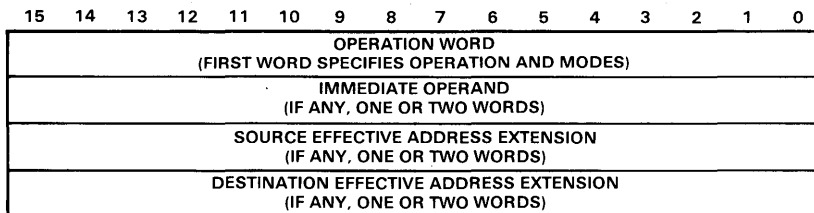
Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two, or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

INSTRUCTION OPERATION WORD

GENERAL FORMAT

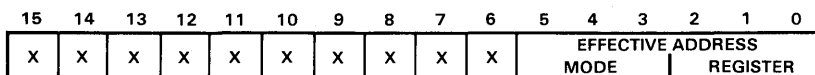
Figure 3



SINGLE-EFFECTIVE-ADDRESS INSTRUCTION

OPERATION WORD

Figure 4



Address Register Indirect With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

SPECIAL ADDRESS MODES

The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference

with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate or Status Register	111	100

IMPLICIT INSTRUCTION REFERENCE SUMMARY

Table 5

Instruction	Implied Register(s)
Branch Conditional (B _{CC}), Branch Always (BRA)	PC
Branch to Subroutine (BSR)	PC, SP
Check Register against Bounds (CHK)	SSP, SR
Test Condition, Decrement and Branch (DB _{CC})	PC
Signed Divide (DIVS)	SSP, SR
Unsigned Divide (DIVU)	SSP, SR
Jump (JMP)	PC
Jump to Subroutine (JSR)	PC, SP
Link and Allocate (LINK)	SP
Move Condition Codes (MOVE CCR)	SR
Move Status Register (MOVE SR)	SR
Move User Stack Pointer (MOVE USP)	USP
Push Effective Address (PEA)	SP
Return from Exception (RTE)	PC, SP, SR
Return and Restore Condition Codes (RTR)	PC, SP, SR
Return from Subroutine (RTS)	PC, SP
Trap (TRAP)	SSP, SR
Trap on Overflow (TRAPV)	SSP, SR
Unlink (UNLK)	SP

Program Counter With Index. This address mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference is classified as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

Byte operation - operand is low order byte of extension word

Word operation - operand is extension word

Long word operation - operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

Condition Codes or Status Register. A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR

ANDI to SR

EORI to CCR

EORI to SR

ORI to CCR

ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4 is a summary of the effective addressing modes discussed in the previous paragraphs.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR). Table 5 provides a list of these instructions and the registers implied.

SYSTEM STACK

The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state, SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state, the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

INSTRUCTION SET SUMMARY

The following paragraphs contain an overview of the form and structure of the MK68000 instruction set. The

instructions form a set of tools that include all the machine functions to perform the following operations:

- Data Movement
- Integer Arithmetic
- Logical
- Shift and Rotate
- Bit Manipulation
- Binary Coded Decimal
- Program Control
- System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

DATA MOVEMENT OPERATIONS

The basic method of data acquisition (transfer and storage) is provided by the move (MOVE) instruction. The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 6 is a summary of the data movement operations.

INTEGER ARITHMETIC OPERATIONS

The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A test operand (TST) instruction that will set the condition codes as a result of a compare of the operand with zero is also available. Test and set (TAS) is a synchronization

instruction useful in multiprocessor systems. Table 7 is a summary of the integer arithmetic operations.

DATA MOVEMENT OPERATIONS

Table 6

Instruction	Size	Operation
EXG	32	$R_x \leftrightarrow R_y$
LEA	32	$EA \rightarrow An$
LINK	—	$An \rightarrow -(SP)$ $SP \rightarrow An$ $SP + displacement \rightarrow SP$
MOVE	8, 16, 32	$(EA)_s \rightarrow EAd$
MOVEM	16, 32	$(EA) \rightarrow An, Dn$ $An, Dn \rightarrow EA$
MOVEP	16, 32	$(EA) \rightarrow Dn$ $Dn \rightarrow EA$
MOVEQ	8	$\#xxx \rightarrow Dn$
PEA	32	$EA \rightarrow -(SP)$
SWAP	32	$Dn[31:16] \leftrightarrow Dn[15:0]$
UNLK	—	$An \rightarrow Sp$ $(SP)^+ \rightarrow An$

NOTES:

s = source
d = destination
[] = bit numbers
-() = indirect with predecrement
()+ = indirect with postincrement
= immediate data

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provides these logical operations with all sizes of immediate data. Table 8 is a summary of the logical operations.

SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by the arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in the instruction of one to eight bits, or 0 to 63 specified in a data register.

INTEGER ARITHMETIC OPERATIONS

Table 7

Instruction	Operand Size	Operation
ADD	8, 16, 32	$Dn + (EA) \rightarrow Dn$ $(EA) + Dn \rightarrow EA$
	16, 32	$(EA) + \#xxx \rightarrow EA$ $An + (EA) \rightarrow An$
ADDX	8, 16, 32	$Dx + Dy + X \rightarrow Dx$
	16, 32	$-(Ax) + -(Ay) + X \rightarrow (Ax)$
CLR	8, 16, 32	$0 \rightarrow EA$
CMP	8, 16, 32	$Dn - (EA)$ $(EA) - \#xxx$
	16, 32	$-(Ax) - (Ay)^+$ $An - (EA)$
DIVS	32 – 16	$Dn / (EA) \rightarrow Dn$
DIVU	32 – 16	$Dn / (EA) \rightarrow Dn$
EXT	8 – 16	$(Dn)_8 \rightarrow Dn_{16}$
	16 – 32	$(Dn)_{16} \rightarrow Dn_{32}$
MULS	$16 * 16 \rightarrow 32$	$Dn * (EA) \rightarrow Dn$
MULU	$16 * 16 \rightarrow 32$	$Dn * (EA) \rightarrow Dn$
NEG	8, 16, 32	$0 - (EA) \rightarrow EA$
NEGX	8, 16, 32	$0 - (EA) - X \rightarrow EA$
SUB	8, 16, 32	$Dn - (EA) \rightarrow Dn$ $(EA) - Dn \rightarrow EA$
	16, 32	$(EA) - \#xxx \rightarrow EA$ $An - (EA) \rightarrow An$
SUBX	8, 16, 32	$Dx - Dy - X \rightarrow Dx$
		$-(Ax) - -(Ay) - X \rightarrow (Ax)$
TAS	8	$(EA) - 0, 1 \rightarrow EA[7]$
TST	8, 16, 32	$(EA) - 0$

NOTE: [] = bit number

x = extend bit

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 9 is a summary of the shift and rotate operations.

BIT MANIPULATION OPERATIONS

Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 10 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

LOGICAL OPERATIONS

Table 8

Instruction	Operand Size	Operation
AND	8, 16, 32	$D_n \Delta (EA) \rightarrow D_n$ $(EA) \Delta D_n \rightarrow EA$ $(EA) \Delta \#xxx \rightarrow EA$
OR	8, 16, 32	$D_n \vee (EA) \rightarrow D_n$ $(EA) \vee D_n \rightarrow EA$ $(EA) \vee \#xxx \rightarrow EA$
EOR	8, 16, 32	$(EA) \oplus D_y \rightarrow EA$ $(EA) \oplus \#xxx \rightarrow EA$
NOT	8, 16, 32	$\sim (EA) \rightarrow EA$

NOTE: \sim = invert

BINARY CODED DECIMAL OPERATIONS

Multiprecision arithmetic operations on binary coded decimal numbers are accomplished using the following instructions: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 11 is a summary of the binary coded decimal operations.

SHIFT AND ROTATE OPERATIONS

Table 9

Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

BIT MANIPULATION OPERATIONS

Table 10

Instruction	Operand Size	Operation
BTST	8, 32	\sim bit of (EA) \rightarrow Z
BSET	8, 32	\sim bit of (EA) \rightarrow Z 1 \rightarrow bit of EA
BCLR	8, 32	\sim bit of (EA) \rightarrow Z 0 \rightarrow bit of EA
BCHG	8, 32	\sim bit of (EA) \rightarrow Z \sim bit of (EA) \rightarrow bit of EA

BINARY CODED DECIMAL OPERATIONS

Table 11

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10} + Dy_{10} + X \rightarrow Dx$ $-(Ax)_{10} + -(Ay)_{10} + X \rightarrow (Ax)$
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ $-(Ax)_{10} - -(Ay)_{10} - X \rightarrow (Ax)$
NBCD	8	$0 - (EA)_{10} - X \rightarrow EA$

PROGRAM CONTROL OPERATIONS

Program control operations are accomplished using a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 12.

The conditional instructions provide setting and branching for the following conditions:

CC - carry clear	LS - low or same
CS - carry set	LT - less than
EQ - equal	MI - minus
F - never true	NE - not equal
GE - greater or equal	PL - plus
GT - greater than	T - always true
HI - high	VC - no overflow
LE - less or equal	VS - overflow

PROGRAM CONTROL OPERATIONS

Table 12

Instruction	Operation
Conditional	
B_{CC}	Branch conditionally (14 conditions) 8- and 16-bit displacement
DB_{CC}	Test condition, decrement, and branch 16-bit displacement
S_{CC}	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 13.

SIGNAL AND BUS OPERATION DESCRIPTION

The following paragraphs contain a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also given.

SIGNAL DESCRIPTION

The input and output signals can be functionally organized into the groups shown in Figure 5. The following paragraphs provide a brief description of the signals and also a reference (if applicable) to other paragraphs that contain more detail about the function being performed.

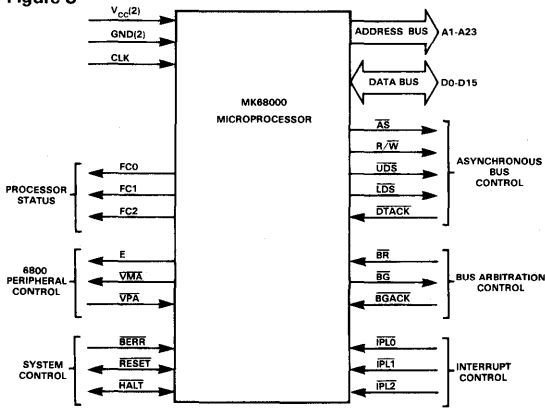
ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

DATA BUS (D0 THROUGH D15). This 16-bit bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

INPUT AND OUTPUT SIGNALS

Figure 5



SYSTEM CONTROL OPERATIONS

Table 13

Instruction	Operation
Privileged	
RESET	Reset external devices
RTE	Return from exception
STOP	Stop program execution
ORI to SR	Logical OR to status register
MOVE USP	Move user stack pointer
ANDI to SR	Logical AND to status register
EORI to SR	Logical EOR to status register
MOVE EA to SR	Load new status register
Trap Generating	
TRAP	Trap
TRAPV	Trap on overflow
CHK	Check data register against upper bounds
Status Register	
ANDI to CCR	Logical AND to condition codes
EORI to CCR	Logical EOR to condition codes
MOVE EA to CCR	Load new condition codes
ORI to CCR	Logical OR to condition codes
MOVE SR to EA	Store status register

VI

Address Strobe (\overline{AS}). This signal indicates that there is a valid address on the address bus.

Read/Write (R/\overline{W}). This signal defines the data bus transfer as a read or write cycle. The R/\overline{W} signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper And Lower Data Strobes (\overline{UDS} , \overline{LDS}). These signals control the data on the data bus, as shown in Table 14. When the R/\overline{W} line is high, the processor will read from the data bus as indicated. When the R/\overline{W} line is low, the processor will write to the data bus as shown.

Data Transfer Acknowledge (\overline{DTACK}). This input indicates that the data transfer is completed. When the processor recognizes \overline{DTACK} during a read cycle, data is latched and the bus cycle terminated. When \overline{DTACK} is recognized during a write cycle, the bus cycle is terminated.

An active transition of data transfer acknowledge, \overline{DTACK} , indicates the termination of a data transfer on the bus.

If the system must run at a maximum rate determined by RAM access times, the relationship between the times at which \overline{DTACK} and DATA are sampled are important.

All control and data lines are sampled during the MK68000's clock high time. The clock is internally buffered, which results in some slight differences in the sampling and recognition of various signals. The \overline{DTACK} signal, like other

DATA STROBE CONTROL OF DATA BUS

Table 14

\overline{UDS}	\overline{LDS}	R/\overline{W}	D8-D15	D0-D7
High	High	-	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

control signals, is internally synchronized to allow for valid operation in an asynchronous system. If the required setup time (#47) is met during S4, \overline{DTACK} will be recognized during S5 and S6, and data will be captured during S6. The data must meet the required setup time (#27).

If an asynchronous control signal does not meet the required setup time, it is possible that it may not be recognized during that cycle. Because of this, asynchronous systems must not allow \overline{DTACK} to precede data by more than parameter #31.

Asserting \overline{DTACK} (or \overline{BERR}) on the rising edge of a clock (such as S4) after the assertion of address strobe will allow an MK68000 system to run at its maximum bus rate. If setup times #27 and #47 are guaranteed, #31 may be ignored. If \overline{DTACK} and \overline{BERR} are asserted at the same time, the MK68000 will recognize the \overline{BERR} and abort the cycle.

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request (\overline{BR}). This input is write ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus Grant (\overline{BG}). This output indicates to all other potential bus master devices that the processor will release bus

control at the end of the current bus cycle.

Bus Grant Acknowledge (\overline{BGACK}). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant has been received
2. address strobe is inactive which indicates that the microprocessor is not using the bus
3. data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is given in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

SYSTEM CONTROL. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error (\overline{BERR}). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices
2. interrupt vector number acquisition failure
3. illegal access request as determined by a memory management unit
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction of the bus error and halt signals.

Reset (\overline{RESET}). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time. Refer to RESET OPERATION paragraph for additional information about reset operation.

Halt (\overline{HALT}). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor

FUNCTION CODE OUTPUTS

Table 15

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state. Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction between the halt and bus error signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

6800 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous 6800 peripheral devices with the asynchronous MK68000. These signals are explained in the following paragraphs.

SIGNAL SUMMARY

Table 16

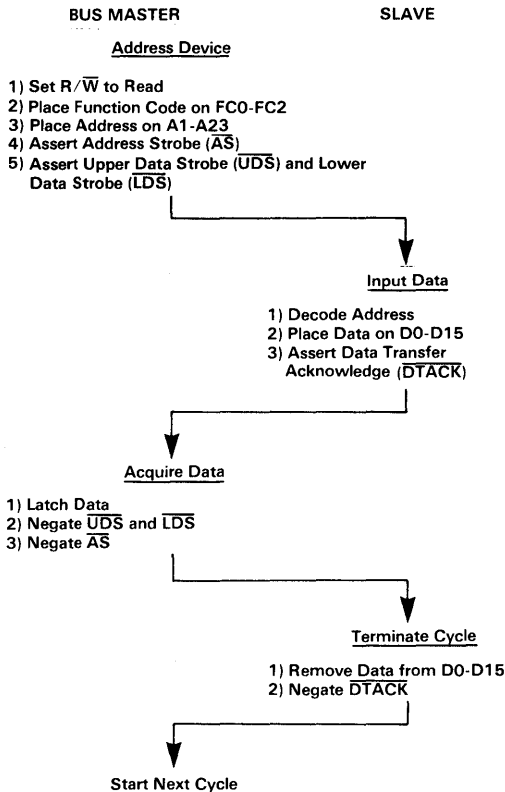
Signal Name	Mnemonic	Input/Output	Active State	Three State	
				On HALT	On BGACK
Address Bus	A1-A23	output	high	yes	yes
Data Bus	D0-D15	input/output	high	yes	yes
Address Strobe	\overline{AS}	output	low	no	yes
Read/Write	R/ \overline{W}	output	read-high write-low	no	yes
Upper and Lower Data Strobes	\overline{UDS} , \overline{LDS}	output	low	no	yes
Data Transfer Acknowledge	\overline{DTACK}	input	low	no	no
Bus Request	\overline{BR}	input	low	no	no
Bus Grant	\overline{BG}	output	low	no	no
Bus Grant Acknowledge	\overline{BGACK}	input	low	no	no
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	no	no
Bus Error	\overline{BERR}	input	low	no	no
Reset	\overline{RESET}	input/output	low	no*	no*
Halt	\overline{HALT}	input/output	low	no*	no*
Enable	E	output	high	no	no
Valid Memory Address	\overline{VMA}	output	low	no	yes
Valid Peripheral Address	\overline{VPA}	input	low	no	no
Function Code Output	FC0, FC1, FC2	output	high	no	yes
Clock	CLK	input	high	no	no
Power Input	V _{CC}	input	—	—	—
Ground	GND	input	—	—	—

* open drain

VI

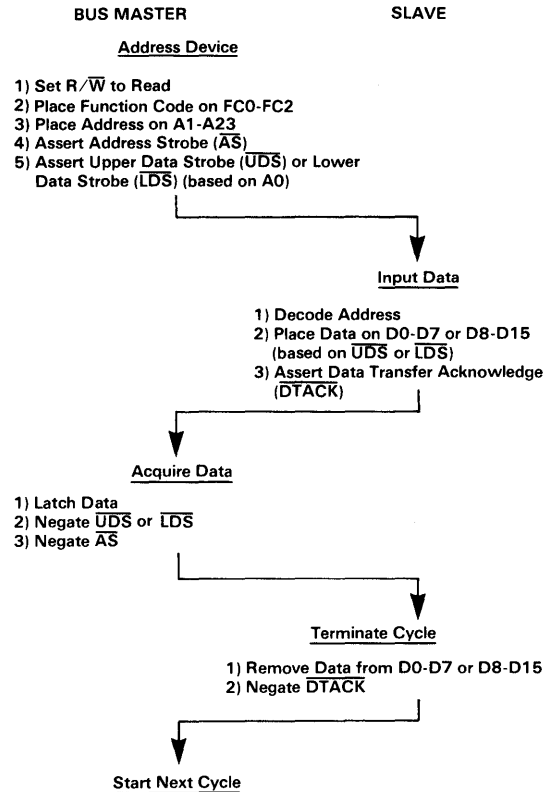
WORD READ CYCLE FLOW CHART

Figure 6



BYTE READ CYCLE FLOW CHART

Figure 7



Enable (E). This signal is the standard enable signal common to all 6800 type peripheral devices. The period for this output is ten MK68000 clock periods (six clocks low; four clocks high). Enable is generated by an internal ring counter which may come up in any state. (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address (VPA). This input indicates that the device or region addressed is a 6800 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH 6800 PERIPHERALS.

Valid Memory Address (VMA). This output is used to indicate to 6800 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the peripheral is a 6800 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 15.

The information indicated by the function code outputs is valid whenever address strobe (AS) is active.

CLOCK (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time, and the clock signal must conform to minimum and maximum pulse width times.

SIGNAL SUMMARY. Table 16 is a summary of all the signals discussed in the previous paragraphs.

BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

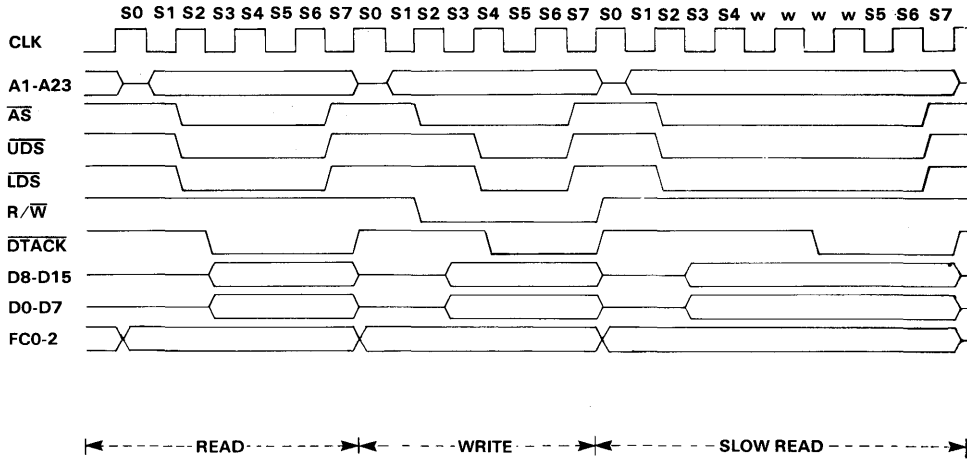
DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following leads:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses

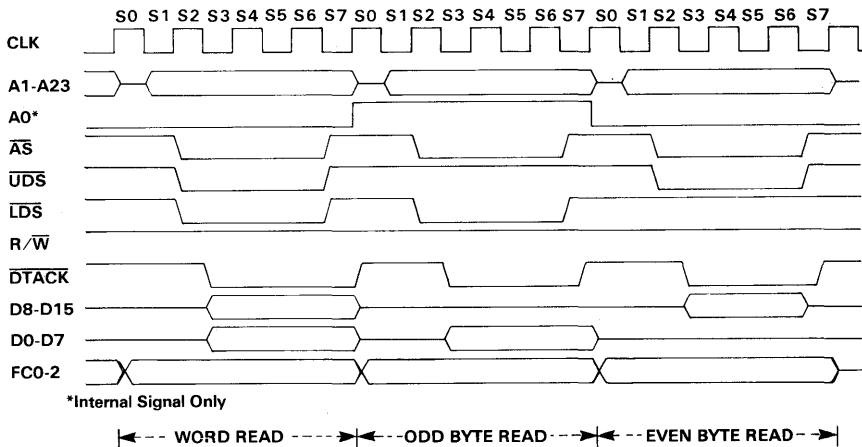
READ AND WRITE CYCLE TIMING DIAGRAM

Figure 8



WORD AND BYTE READ CYCLE TIMING DIAGRAM

Figure 9



*Internal Signal Only

used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the MK68000 for interlocked multiprocessor communications.

NOTE

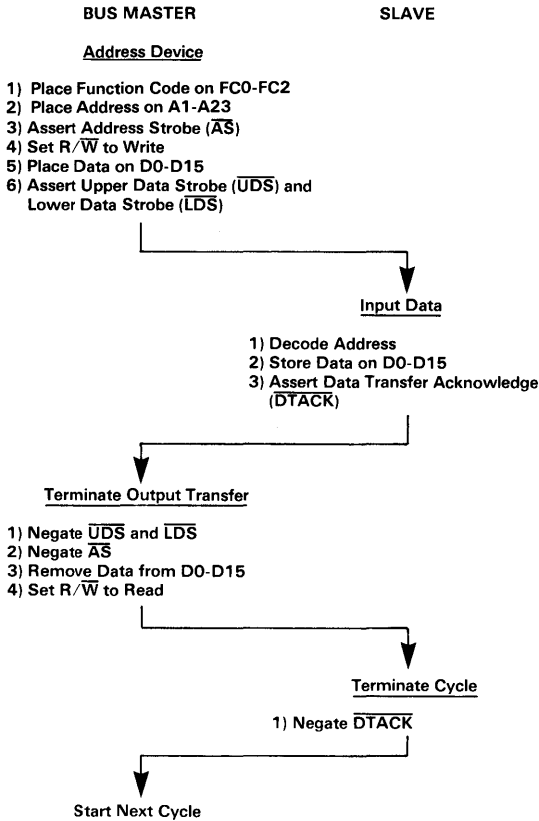
The terms assertion and negation will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert

or assertion is used to indicate that a signal is active or true independent of whether that voltage is low or high. The term negate or negation is used to indicate that a signal is inactive or false.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both bytes. When the instruction specifies byte operation, the processor uses an internal $A0$ bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the $A0$ bit equals zero, the upper data strobe is issued. When the $A0$ bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

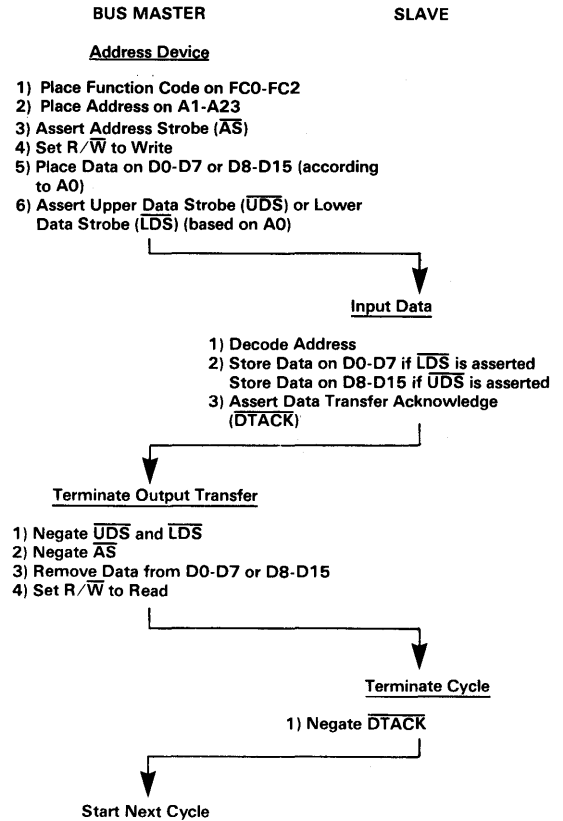
WORD WRITE CYCLE FLOW CHART

Figure 10



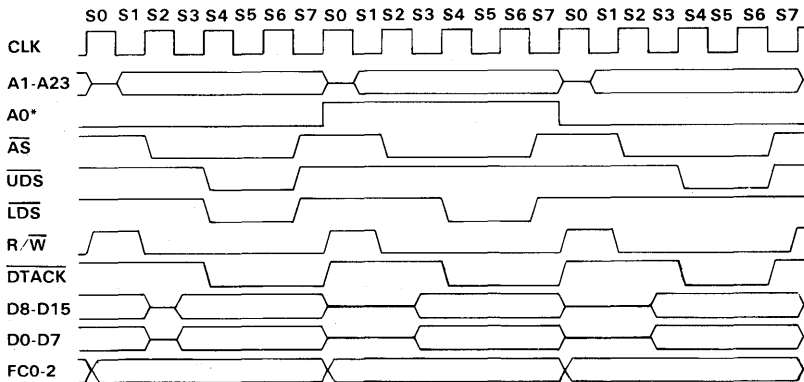
BYTE WRITE CYCLE FLOW CHART

Figure 11



WORD AND BYTE WRITE CYCLE TIMING DIAGRAM

Figure 12

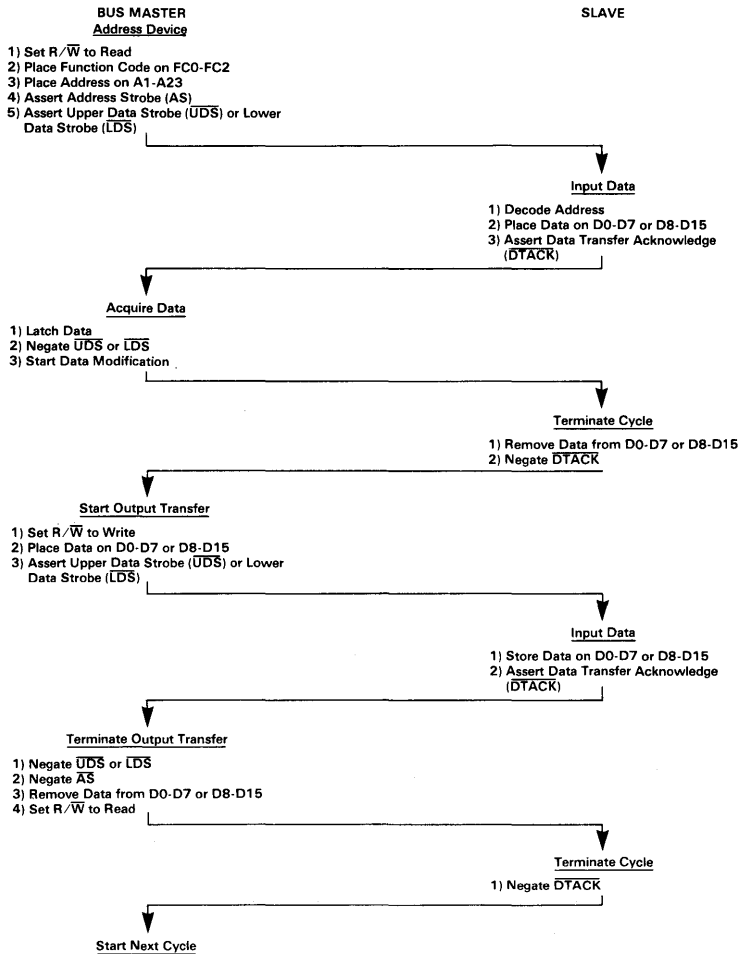


*Internal Signal Only



READ-MODIFY-WRITE CYCLE FLOW CHART

Figure 13



VI

A word read cycle flow chart is given in Figure 6. A byte read cycle flow chart is given in Figure 7. Read cycle timing is given in Figure 8 and Figure 9 details word and byte read cycle operation.

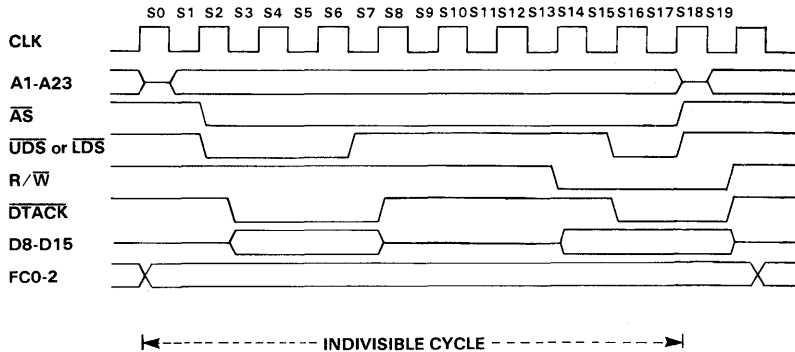
Write Cycle. During a write cycle, the processor sends data to memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal AO bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the AO bit equals zero, the upper data strobe is issued. When the AO bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 10. A byte write cycle flow chart is given in Figure 11. Write cycle timing is given in Figure 8 and Figure 12 details word and byte write cycle operation.

Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the MK68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 13 and a timing diagram is given in Figure 14.

BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of:

READ—MODIFY—WRITE CYCLE TIMING DIAGRAM

Figure 14



1. Asserting a bus mastership request.
2. Receiving a grant that the bus is available at the end of the current cycle.
3. Acknowledging that mastership has been assumed.

Figure 15 is a flow chart showing the detail involved in a request from a single device. Figure 16 is a timing diagram for the same operations. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This type of operation would be true for a system consisting of the processor and one device capable of bus mastership. In systems having a number of devices capable of bus mastership, the bus request line from each device is wire ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signal is negated a few clock cycles after the transition of the acknowledge (BGACK) signal.

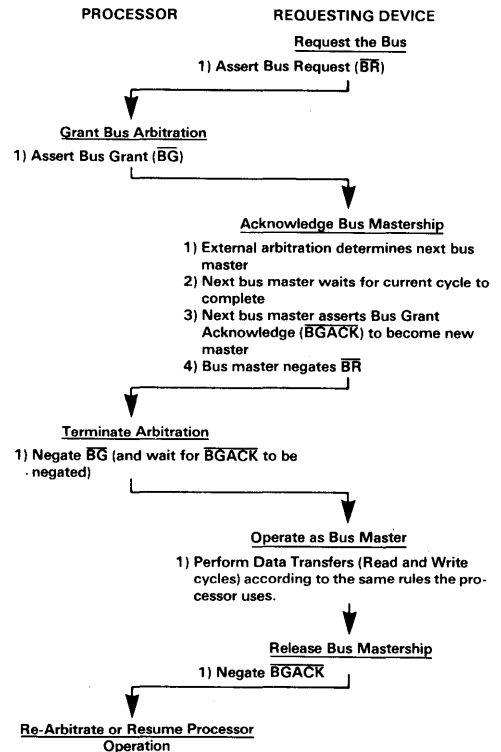
However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request (\overline{BR}) signal. This is a wire ORed signal (although it need not be constructed from open collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows

BUS ARBITRATION CYCLE FLOW-CHART

Figure 15

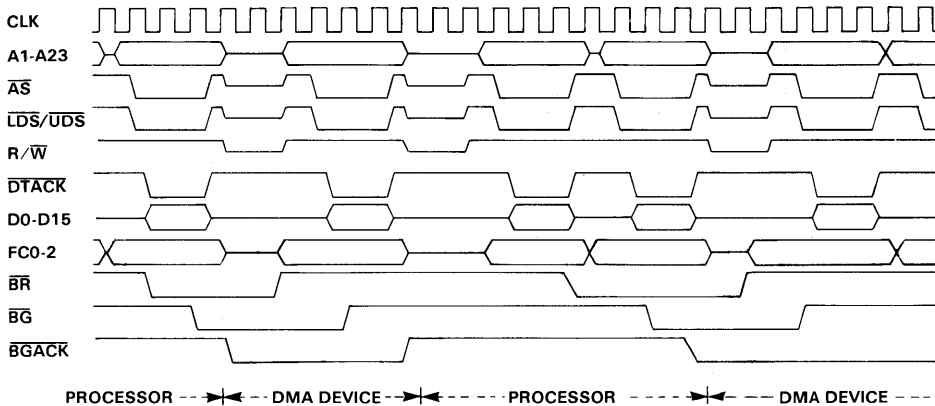


ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

Receiving the Bus Grant. The processor asserts bus grant (\overline{BG}) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe

BUS ARBITRATION CYCLE TIMING DIAGRAM

Figure 16



(\overline{AS}) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed. The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

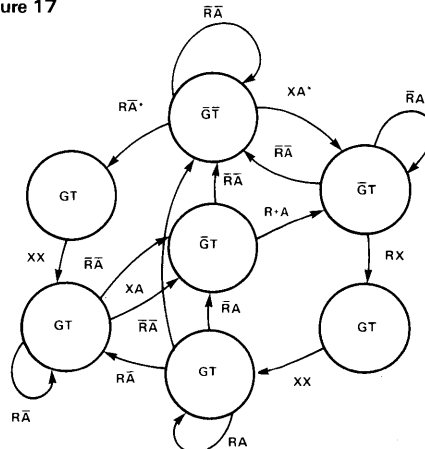
Acknowledgement of Mastership. Upon receiving a bus grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own \overline{BGACK} . The negation of the address strobe indicates that the previous master has completed its cycle, the negation of bus grant acknowledge indicates that the previous master has released the bus. (While address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued the device is bus master until it negates bus grant acknowledge. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be dropped when bus grant acknowledge is asserted. If bus request is still asserted after bus grant acknowledge is negated, the processor performs another arbitration sequence and issues another bus grant. Note that the processor does not perform any external bus cycles before it re-asserts bus grant.

BUS ARBITRATION CONTROL. The bus arbitration control unit in the MK68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 17. All asynchronous signals to the MK68000 are

STATE DIAGRAM OF MK68000 BUS ARBITRATION UNIT

Figure 17



- R = Bus Request Internal
- A = Bus Grant Acknowledge Internal
- G = Bus Grant
- T = Three-state Control to Bus Control Logic**
- X = Don't Care

*State machine will not change state if bus is in S0. Refer to BUS ARBITRATION CONTROL for additional information.

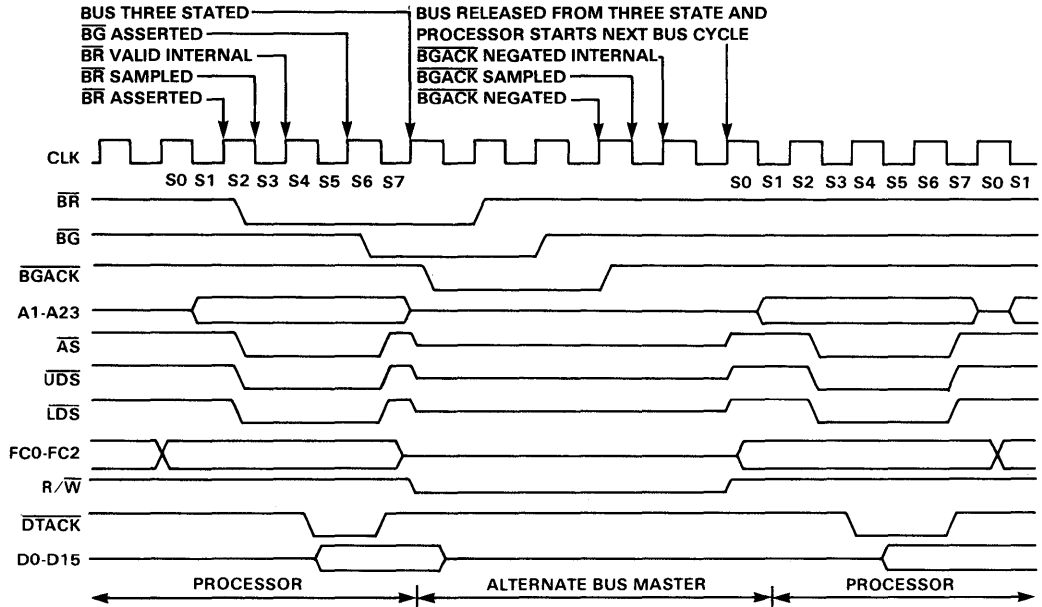
**The address bus will be placed in the high impedance state if T is asserted and \overline{AS} is negated.

synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met. The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge.

As shown in Figure 17, input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a

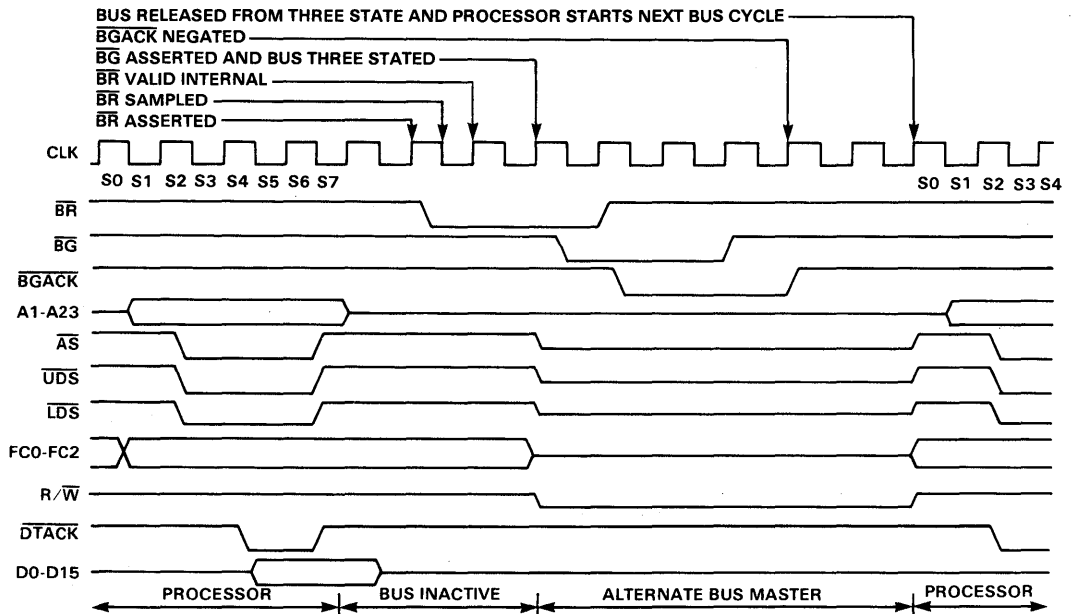
BUS ARBITRATION DURING PROCESSOR BUS CYCLE

Figure 18



BUS ARBITRATION WITH BUS INACTIVE

Figure 19



high-impedance state when \overline{AS} is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

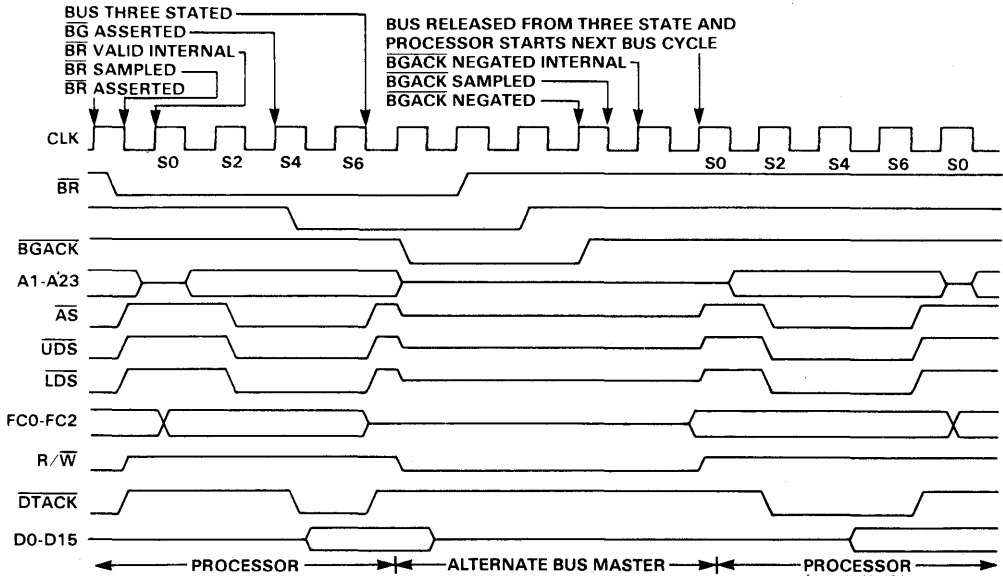
State changes (valid outputs) occur on the next rising edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 18. The bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 19.

If a bus request is made at a time when the MPU has already begun a bus cycle but \overline{AS} has not been asserted (bus state S0), \overline{BG} will not be asserted on the next rising edge. Instead, \overline{BG} will be delayed until the second rising edge following its internal assertion. This sequence is shown in Figure 20.

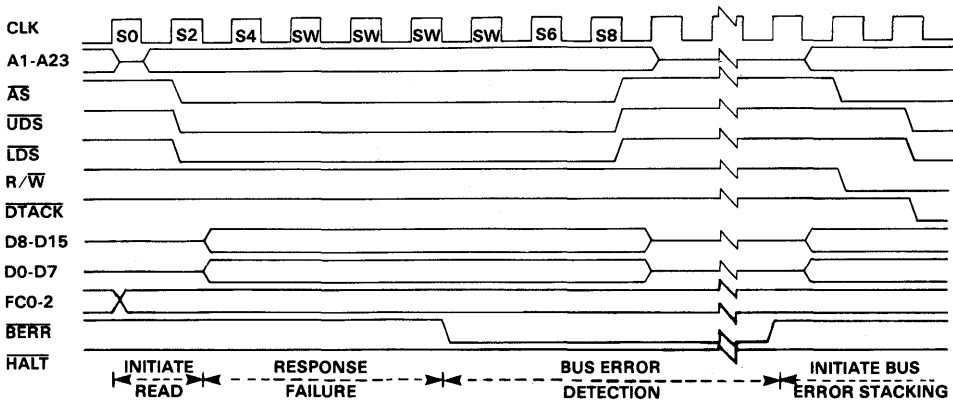
BUS ARBITRATION SPECIAL CASE

Figure 20



BUS ERROR TIMING DIAGRAM

Figure 21

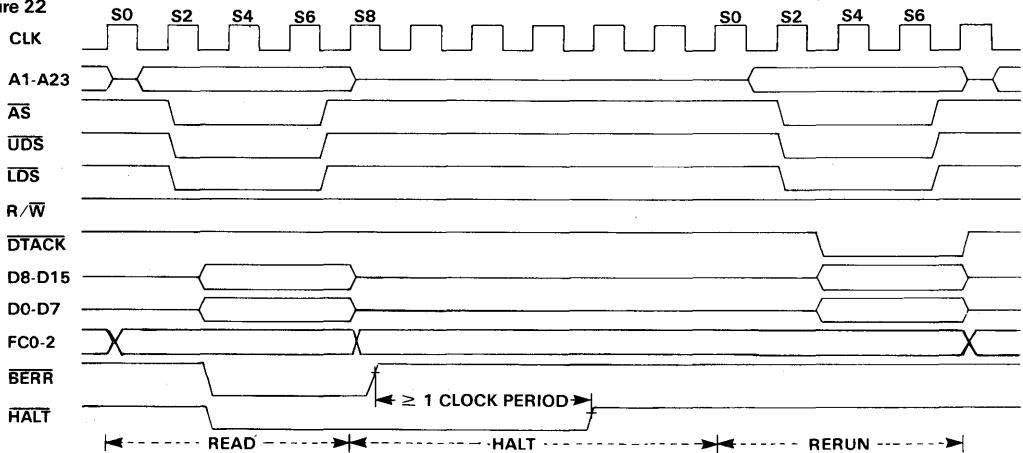


BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided. External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

Exception Sequence. When the bus error signal is asserted, the current bus cycle is terminated. If \overline{BERR} is asserted before the falling edge of S2, \overline{AS} will be negated in S7 in either a read or write cycle. As long as \overline{BERR} remains asserted, the data and address buses will be in the high-impedance state. When the \overline{BERR} is negated, the processor will begin stacking for exception processing. The bus error exception sequence is entered when the processor receives

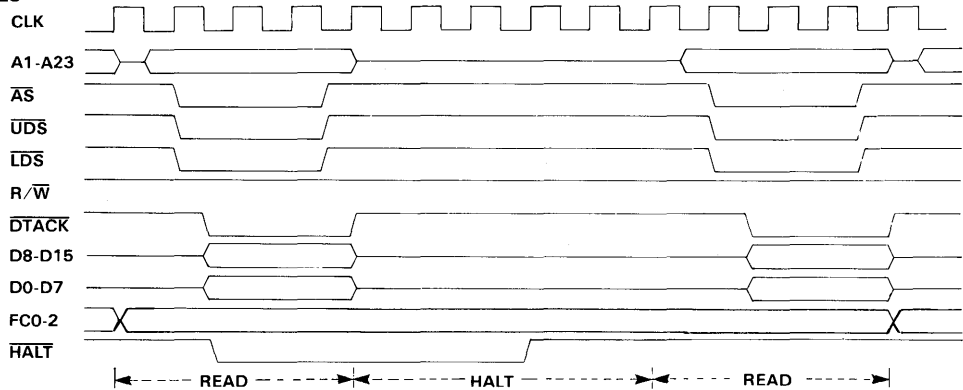
RE-RUN BUS CYCLE TIMING INFORMATION

Figure 22



HALT SIGNAL TIMING CHARACTERISTICS

Figure 23



a bus error signal and the halt pin is inactive. Figure 21 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. Stacking the program counter and status register
2. Stacking the error information
3. Reading the bus error vector table entry
4. Executing the bus error handler routine

The stacking of the program counter and the status register is the same as if an interrupt had occurred. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address \$000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to EXCEPTION PROCESSING for additional information.

Re-Running the Bus Cycle. When the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the re-run sequence. Figure 22 is a timing diagram for re-running the bus cycle.

The processor terminates the bus cycle, then puts the address and data lines in the high-impedance state. The processor remains "halted," and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. The bus error signal should be removed at least one clock cycle before the halt signal is removed.

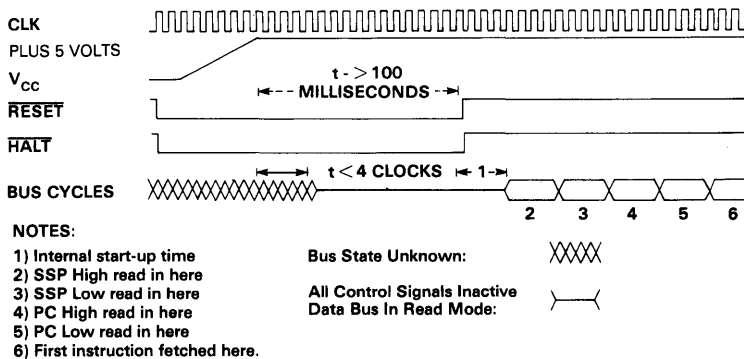
NOTE

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing \overline{AS} . If \overline{BERR} and \overline{HALT} are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation with No Bus Error. The halt input signal to the MK68000 performs a Halt/Run/Single-Step function. The halt and run modes are somewhat self explanatory in that when the halt signal is constantly active the processor

RESET OPERATION TIMING DIAGRAM

Figure 24



“halts” (does nothing) and when the halt signal is constantly inactive the processor “runs” (does something).

The single-step mode is derived from correctly timed transitions on the halt signal input. It forces the processor to execute a single bus cycle by entering the “run” mode until the processor starts a bus cycle then changing to the “halt” mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 23 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between the bus error signal and the halt pin when using the single cycle mode as a debugging tool. This is also true of interactions between the halt and reset lines, since these can reset the machine.

When the processor completes a bus cycle after recognizing that the halt signal is active, most three-state signals are put in the high-impedance state. These include:

1. address lines
2. data lines

This is required for correct performance of the re-run bus cycle operation.

While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration. It is the bus arbitration function that removes the control signals from the bus.

The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single instructions at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to

as a double bus fault. When a double bus fault occurs, the processor will halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 24 is a timing diagram for reset operations. Both the halt and the reset lines must be applied to ensure total reset of the processor.

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor. The processor responds by reading the reset vector table entry (vector number zero, address \$000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address \$000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven. No other registers are affected by the reset sequence.

When a RESET sequence is executed, the processor drives the reset pin for 124 clock periods. In this case, the processor is trying to reset the rest of the system. Therefore, there is no effect on the internal state of the processor. All of the processor’s internal registers and the status register are unaffected by the execution of a RESET instruction. All external devices connected to the reset line will be reset at

DTACK, BERR, HALT ASSERTION RESULTS

Table 17

Case No.	Control Signal	Asserted on Rising Edge of State		Result
		N	N+2	
1	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	S X X	Normal cycle terminate and continue.
2	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA A	S X S	Normal cycle terminate and halt. Continue when HALT removed.
3	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	A NA S	Normal cycle terminate and halt. Continue when HALT removed.
4	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A NA	X S NA	Terminate and take bus error trap.
5	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A A	X S S	Terminate and re-run.
6	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	X A S	Terminate and re-run when HALT removed.

Legend:

N — the number of the current even bus state (e.g., S4, S6, etc.)

A — signal is asserted in this bus state

NA — signal is not asserted in this state

X — don't care

S — signal was asserted in previous state and remains asserted in this state

BERR AND HALT NEGATION RESULTS

Table 18

Conditions of Termination in Table 17	Control Signal	Negated on Rising Edge of State		Results — Next Cycle
		N	N+2	
Bus Error	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• or • • or •	• •	Takes bus error trap.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• or • •	•	Illegal sequence, usually traps to vector number 0.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	•	•	Re-runs the bus cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• or •	•	May lengthen next cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• or •	• none	If next cycle is started it will be terminated as a bus error.

Legend:

• = signal is negated in this bus state

the completion of the RESET instruction.

Asserting the reset and halt pins for 10 clock cycles will cause a processor reset, except when V_{CC} is initially applied to the processor. In this case, an external reset must be applied to the reset pin for at least 100 milliseconds.

THE RELATIONSHIP OF \overline{DTACK} , \overline{BERR} , AND \overline{HALT}

In order to control termination of a bus cycle for a re-run or a bus error condition properly, \overline{DTACK} , \overline{BERR} , and \overline{HALT} should be asserted and negated on the rising edge of the MK68000 clock. This will assure that when two signals are asserted simultaneously, the required setup time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the MK68000. Parameter #48 is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 17):

Normal Termination: \overline{DTACK} occurs first (case 1).

Halt Termination: \overline{HALT} is asserted at same time, or precedes \overline{DTACK} (no \overline{BERR}) cases 2 and 3.

Bus Error Termination: \overline{BERR} is asserted in lieu of, at same time, or preceding \overline{DTACK} (case 4); \overline{BERR} negated at same time, or after \overline{DTACK} .

Re-Run Termination: \overline{HALT} and \overline{BERR} asserted at the same time, or before \overline{DTACK} (cases 5 and 6); \overline{HALT} must be negated at least 1 cycle after \overline{BERR} .

Table 17 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 18 (\overline{DTACK} is assumed to be negated normally in all cases; for best results, both \overline{DTACK} and \overline{BERR} should be negated when address strobe is negated.)

Example A: A system uses a watch-dog timer to terminate accesses to un-populated address space. The timer asserts \overline{DTACK} and \overline{BERR} simultaneously after time-out. (case 4)

Example B: A system uses error detection on RAM contents. Designer may (a) delay \overline{DTACK} until data verified, and return \overline{BERR} and \overline{HALT} simultaneously to re-run error cycle (case 5), or if valid, return \overline{DTACK} ; (b) delay \overline{DTACK} until data verified, and return \overline{BERR} at same time as \overline{DTACK} if data in error (case 4); (c) return \overline{DTACK} prior to data verification, as described in previous section. If data invalid, \overline{BERR} is asserted (case 1) in next cycle. Error-handling software must know how to recover error cycle.

PROCESSING STATES

The MK68000 is always in one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to

store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines which operations are legal, is used by the external memory management device to control and translate accesses, and is used to choose between the supervisor stack pointer and the user stack pointer in instruction references.

The privilege state is a mechanism for providing security in a computer system. Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by the S-bit of the status register; if the S-bit is asserted (high), the processor is in the supervisor state. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by the S-bit of the status register; if the S-bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole status register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicitly, or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made, using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 19 lists the classification of references.

EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made,

REFERENCE CLASSIFICATION

Table 19

Function Code Output			Reference Class
FC2	FC1	FC0	
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

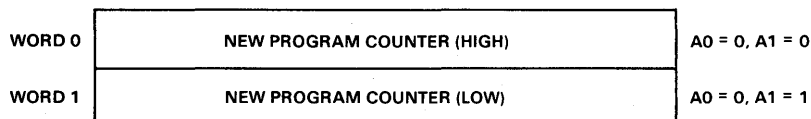
and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor context. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 25), except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 26) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 27. The memory layout for exception vectors is given in Table 20.

As shown in Table 20, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, these are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

EXCEPTION VECTOR FORMAT

Figure 25



EXCEPTION VECTOR ASSIGNMENT

Table 20

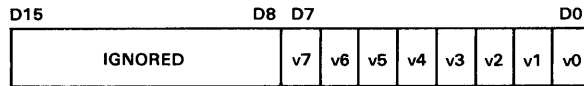
Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset Initial SSP
—	4	004	SP	Reset Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	040	SD	(Unassigned, reserved)
	92	05C		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	188	0BC		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	252	0FC		—
64-255	256	100	SD	User Interrupt Vectors
	1020	3FC		—

*Vector numbers 12, 13, 14, 16 through 23 and 48 through 63 are reserved for future enhancements by Mostek. No user peripheral devices should be assigned these numbers.

VI

PERIPHERAL VECTOR NUMBER FORMAT

Figure 26

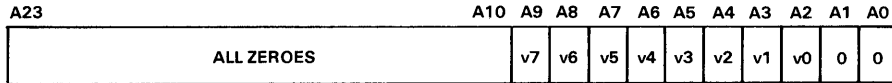


Where:

v7 is the MSB of the Vector Number
v0 is the LSB of the Vector Number

ADDRESS TRANSLATED FROM 8-BIT VECTOR NUMBER

Figure 27



KINDS OF EXCEPTIONS. Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts and the bus error and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset inputs are used for access control and processor restart. The internally generated exceptions come from instructions, or from address errors or tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status, except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer. The program counter value stacked usually points to the next unexecuted instruction, however for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence at the next minor cycle of the processor. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by bus error and then address error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction

EXCEPTION GROUPING AND PRIORITY

Table 21

Group	Exception	Processing
0	Reset Bus Error Address Error	Exception processing begins within two clock cycles
1	Trace Interrupt Illegal Privilege	Exception processing begins before the next instruction
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. A summary of exception grouping and priority is given in Table 21.

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state, and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power-up/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt

priority levels are numbered from one to seven, level seven being the highest priority. The status register contains a three-bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 28; a timing diagram is given in Figure 29, and the interrupt processing sequence is shown in Figure 30.

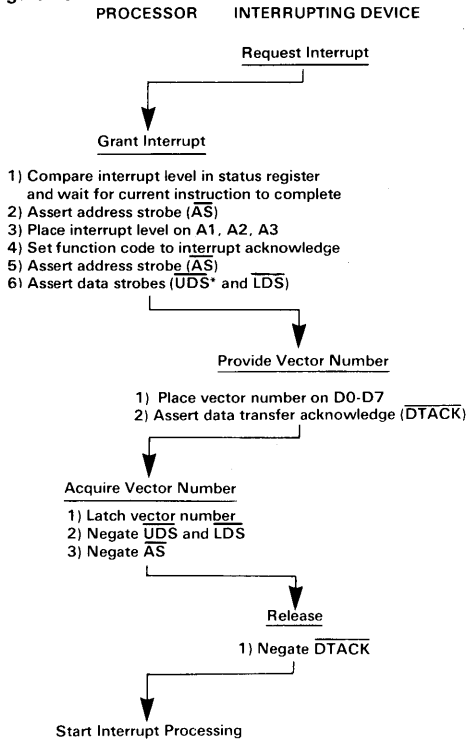
Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a “non-maskable interrupt” capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

UNINITIALIZED INTERRUPT. An interrupting device asserts VPA or provides an interrupt vector during an interrupt acknowledge cycle to the MK68000. If the vector register has not been initialized, the responding MK68000 Family peripheral will provide vector 15, the uninitialized



INTERRUPT ACKNOWLEDGE SEQUENCE FLOW CHART

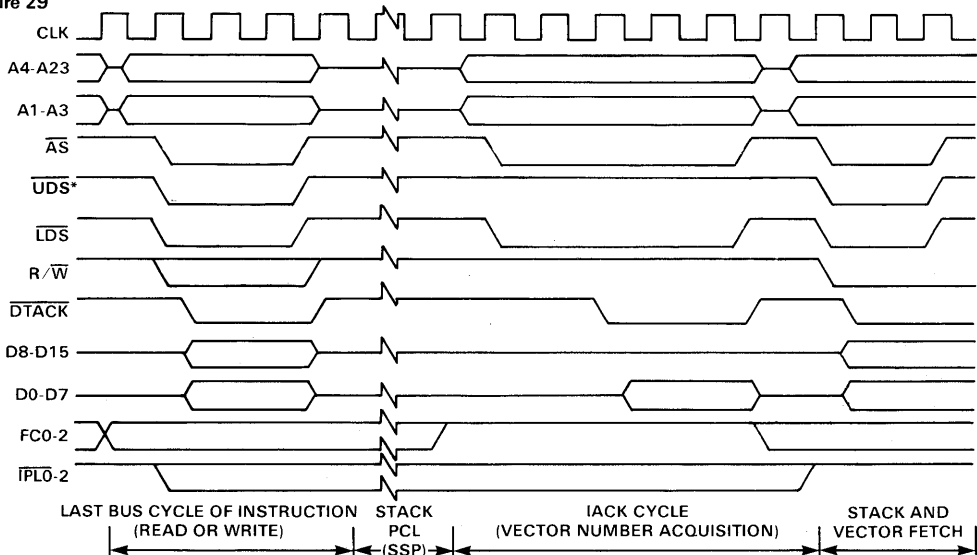
Figure 28



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

INTERRUPT ACKNOWLEDGE SEQUENCE TIMING DIAGRAM

Figure 29



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

interrupt vector. This provides a uniform way to recover from a programming error.

SPURIOUS INTERRUPT. If during the interrupt acknowledge cycle no device responds by asserting \overline{DTACK} or \overline{VPA} , the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

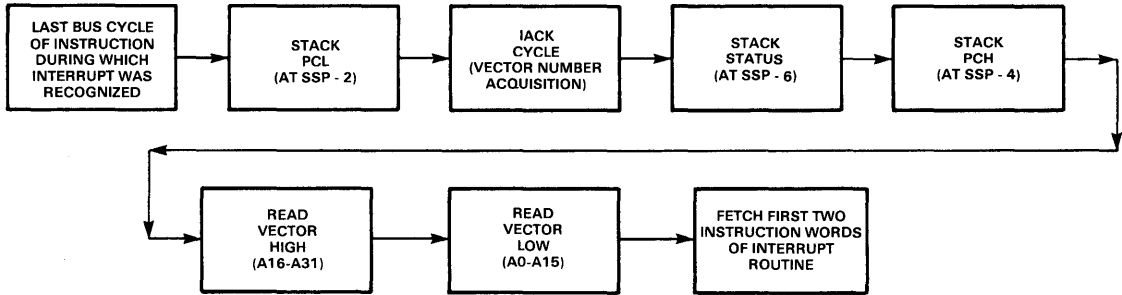
The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction is the term used to refer to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and

INTERRUPT PROCESSING SEQUENCE

Figure 30



NOTE:

SSP refers to the value of the supervisor stack pointer before the interrupt occurs.

separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND (word) Immediate to SR
RESET	EOR (word) Immediate to SR
RTE	OR (word) Immediate to SR
MOVE to SR	MOVE USP

TRACING. To aid in program development, the MK68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved whether it was a read or a write, whether the processor was processing an instruction or not, and the classification



displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if it is in the normal state or processing a Group 2 exception; the processor is not processing an instruction if it is processing a Group 0 or a Group 1 exception. Figure 31 illustrates how this information is organized on the supervisor stack. Although this information is not sufficient in general to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

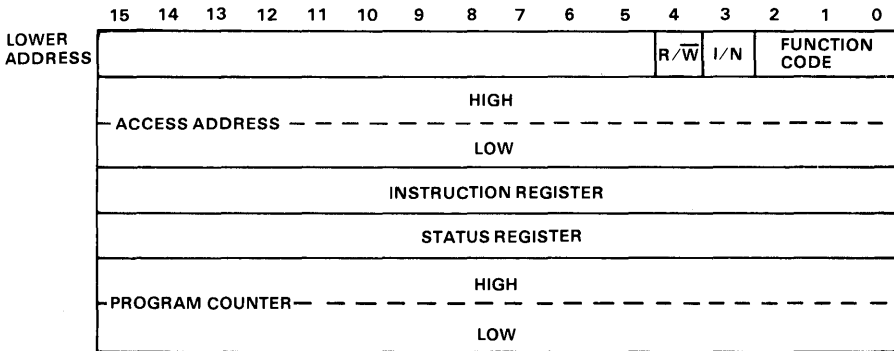
If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes

itself from the system rather than destroy all memory contents. Only the RESET pin can restart a halted processor.

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted. As shown in Figure 32, an address error will execute a short bus cycle followed by exception processing.

SUPERVISOR STACK ORDER

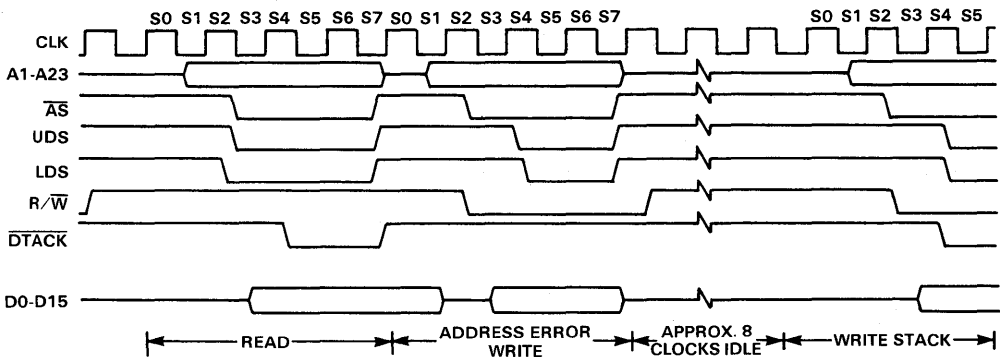
Figure 31



R/W (read/write): write = 0, read = 1. I/N (instruction/not): instruction = 0, not = 1

ADDRESS ERROR TIMING

Figure 32



INTERFACE WITH 6800 PERIPHERALS

To interface the synchronous 6800 peripherals with the asynchronous MK68000, the processor modifies its bus cycle to meet the 6800 cycle requirements whenever a 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 33 is a flow chart of the interface operation between the processor and 6800 devices.

DATA TRANSFER OPERATION

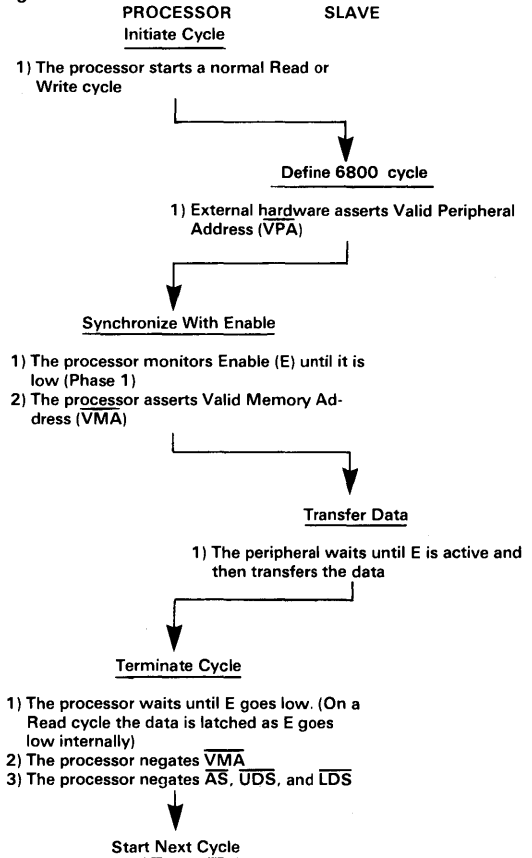
Three signals on the processor provide the 6800 interface. They are: enable (E), valid memory address (\overline{VMA}), and valid peripheral address (\overline{VPA}). Enable corresponds to the E or $\Phi 2$ signal in existing 6800 systems. It is the bus clock used by the frequency clock that is one tenth of the incoming MK68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz MK68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive \overline{VPA} accesses on successive E pulses.

6800 cycle timing is given in Figure 34. At state zero (S0) in the cycle, the address bus and function codes are in the high-impedance state. One half clock later, in state 1, the address bus and function code outputs are released from the high-impedance state.

During state 2, the address strobe (\overline{AS}) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/ \overline{W}) signal is switched to low (write) during state 2. One half clock later, in state 3, the write data

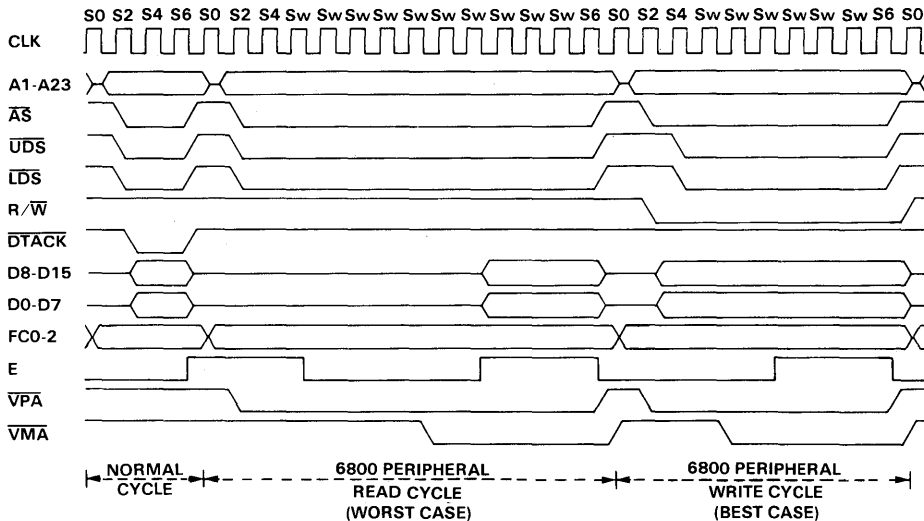
6800 INTERFACING FLOW CHART

Figure 33



6800 CYCLE OPERATION

Figure 34



is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus.

The processor now inserts wait states until it recognizes the assertion of \overline{VPA} . The \overline{VPA} input signals the processor that the address on the bus is the address of a 6800 device (or an area reserved for 6800 devices) and that the bus should conform to the $\Phi 2$ transfer characteristics of the 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by address strobe.

After the recognition of \overline{VPA} , the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts \overline{VMA} . Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the 6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal.

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7 and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high at this time. The peripheral logic must remove \overline{VPA} within one clock after address strobe is negated. \overline{DTACK} should not be asserted while \overline{VPA} is asserted.

Notice that the MK68000 \overline{VMA} is active low, contrasted with the active high 6800 \overline{VMA} . This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

INTERRUPT INTERFACE OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if \overline{VPA} is asserted, the MK68000 will assert \overline{VMA} and complete a normal 6800 read cycle as shown in Figure 35. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

This operates in the same fashion (but is not restricted to) the 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the 6800 and the MK68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since \overline{VMA} is asserted during autovectoring, the 6800

peripheral address decoding should prevent unintended accesses.

INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the MK68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instruction definitions.

Data	If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.
Memory	If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.
Alterable	If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.
Control	If an effective address mode may be used to refer to memory operands without an associated size, it is considered a control addressing effective address mode.

Table 22 shows the various categories to which each of the effective address modes belong. Table 23 is the instruction set summary.

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

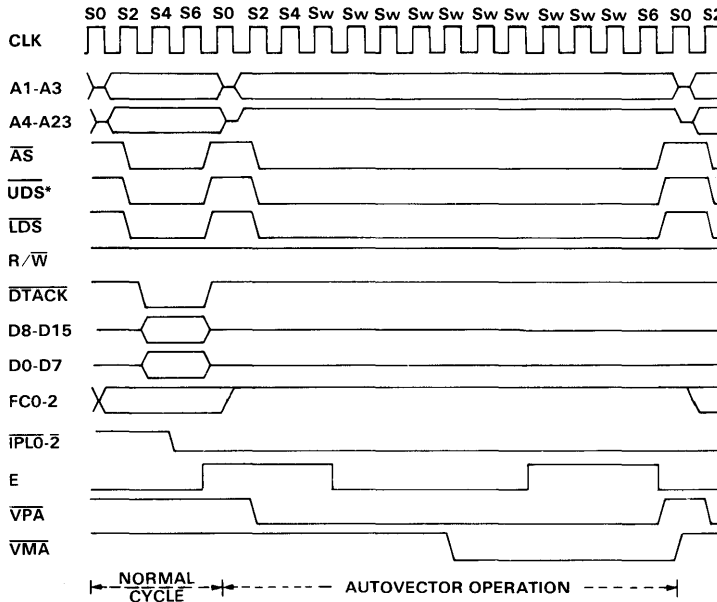
INSTRUCTION PRE-FETCH

The MK68000 uses a 2-word tightly-coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

- 1) When execution of an instruction begins, the operation word and the word following have already been

AUTOVECTOR OPERATION TIMING DIAGRAM

Figure 35



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

EFFECTIVE ADDRESSING MODE CATEGORIES

Table 22

Effective Address Modes	Mode	Register	Data	Addressing Categories		
				Memory	Control	Alterable
Dn	000	register number	X	-	-	X
An	001	register number	-	-	-	X
(An)	010	register number	X	X	X	X
(An)+	011	register number	X	X	-	X
-(An)	100	register number	X	X	-	X
d(An)	101	register number	X	X	X	X
d(An,ix)	110	register number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
d(PC)	111	010	X	X	X	-
d(PC,ix)	111	011	X	X	X	-
#xxx	111	100	X	X	-	-

INSTRUCTION SET

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	(Destination) ₁₀ +(Source) ₁₀ → Destination	*	U	*	U	*
ADD	Add Binary	(Destination)+(Source) → Destination	*	*	*	*	*

* affected 0 cleared U undefined - unaffected 1 set [] = bit number d = displacement

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ADDA	Add Address	(Destination)+(Source) → Destination	-	-	-	-	-
ADDI	Add Immediate	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination)+(Source)+ X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) \wedge (Source) → Destination	-	*	*	0	0
ANDI	AND Immediate	(Destination) \wedge Immediate Data → Destination	-	*	*	0	0
ANDI to CCR	AND Immediate to Condition Codes	(Source) \wedge CCR → CCR	*	*	*	*	*
ANDI to SR	AND Immediate to Status Register	(Source) \wedge SR → SR	*	*	*	*	*
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B _{CC}	Branch Conditionally	If _{CC} then PC+d → PC	-	-	-	-	-
BCHG	Test a Bit and Change	\sim (<bit number>) OF Destination → Z \sim (<bit number>) OF Destination → <bit number> OF Destination	-	-	*	-	-
BCLR	Test a Bit and Clear	\sim (<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	-	-	*	-	-
BRA	Branch Always	PC + d → PC	-	-	-	-	-
BSET	Test a Bit and Set	\sim (<bit number>) OF Destination → Z 1 → <bit number> OF Destination	-	-	*	-	-
BSR	Branch to Subroutine	PC → -(SP), PC+d → PC	-	-	-	-	-
BTST	Test a Bit	\sim (<bit number>) OF Destination → Z	-	-	*	-	-
CHK	Check Register against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	-	*	U	U	U
CLR	Clear an Operand	0 → Destination	-	0	1	0	0
CMP	Compare	(Destination) - (Source)	-	*	*	*	*
CMPA	Compare Address	(Destination) - (Source)	-	*	*	*	*
CMPI	Compare Immediate	(Destination) - Immediate Data	-	*	*	*	*
CMPM	Compare Memory	(Destination) - (Source)	-	*	*	*	*
DB _{CC}	Test Condition, Decrement and Branch	If _{CC} then Dn - 1 → Dn; if Dn \neq - 1 then PC + d → PC	-	-	-	-	-
DIVS	Signed Divide	(Destination)/(Source) → Destination	-	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	-	*	*	*	0
EOR	Exclusive OR Logical	(Destination) \oplus (Source) → Destination	-	*	*	0	0

* affected 0 cleared U undefined - unaffected 1 set [] = bit number d = displacement

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
EORI	Exclusive OR Immediate	(Destination) \oplus Immediate Data \rightarrow Destination	-	*	*	0	0
EORI to CCR	Exclusive OR Immediate to Condition Codes	(Source) \oplus CCR \rightarrow CCR	*	*	*	*	*
EORI to SR	Exclusive OR Immediate to Status Register	(Source) \oplus SR \rightarrow SR	*	*	*	*	*
EXG	Exchange Register	Rx \leftrightarrow Ry	-	-	-	-	-
EXT	Sign Extend	(Destination) Sign-extended \rightarrow Destination	-	*	*	0	0
JMP	Jump	Destination \rightarrow PC	-	-	-	-	-
JSR	Jump to Subroutine	PC \rightarrow -(SP); Destination \rightarrow PC	-	-	-	-	-
LEA	Load Effective Address	Destination \rightarrow An	-	-	-	-	-
LINK	Link and Allocate	An \rightarrow -(SP); SP \rightarrow An; SP + d \rightarrow SP	-	-	-	-	-
LSL, LSR	Logical Shift	(Destination) Shifted by <count> \rightarrow Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) \rightarrow Destination	-	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) \rightarrow CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) \rightarrow SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR \rightarrow Destination	-	-	-	-	-
MOVE USP	Move User Stack Pointer	USP \rightarrow An, An \rightarrow USP	-	-	-	-	-
MOVEA	Move Address	(Source) \rightarrow Destination	-	-	-	-	-
MOVEM	Move Multiple Registers	Registers \rightarrow Destination (Source) \rightarrow Registers	-	-	-	-	-
MOVEP	Move Peripheral Data	(Source) \rightarrow Destination	-	-	-	-	-
MOVEQ	Move Quick	Immediate Data \rightarrow Destination	-	*	*	0	0
MULS	Signed Multiply	(Destination)* (Source) \rightarrow Destination	-	*	*	0	0
MULU	Unsigned Multiply	(Destination)* (Source) \rightarrow Destination	-	*	*	0	0
NBCD	Negate Decimal with Extend	0 - (Destination) ₁₀ - X \rightarrow Destination	*	U	*	U	*
NEG	Negate	0 - (Destination) \rightarrow Destination	*	*	*	*	*
NEGX	Negate with Extend	0 - (Destination) - X \rightarrow Destination	*	*	*	*	*
NOP	No Operation	-	-	-	-	-	-
NOT	Logical Complement	\sim (Destination) \rightarrow Destination	-	*	*	0	0
OR	Inclusive OR Logical	(Destination) \vee (Source) \rightarrow Destination	-	*	*	0	0

* affected 0 cleared U undefined - unaffected 1 set [] = bit number d = displacement

VI

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ORI	Inclusive OR Immediate	(Destination) v Immediate Data → Destination	-	*	*	0	0
ORI to CCR	Inclusive OR Immediate to Condition Codes	(Source) V CCR → CCR	*	*	*	*	*
ORI to SR	Inclusive OR Immediate to Status Register	(Source) V SR → SR	*	*	*	*	*
PEA	Push Effective Address	Destination → -(SP)	-	-	-	-	-
RESET	Reset External Devices	-	-	-	-	-	-
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	-	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> → Destination	*	*	*	0	*
RTE	Return from Exception	(SP)+ → SR, (SP)+ → PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	(SP)+ → CC; (SP)+ → PC	*	*	*	*	*
RTS	Return from Subroutine	(SP)+ → PC	-	-	-	-	-
SBCD	Subtract Decimal with Extend	(Destination) ₁₀ - (Source) ₁₀ - X → Destination	*	U	*	U	*
S _{CC}	Set According to Condition	If CC then 1's → Destination else 0's → Destination	-	-	-	-	-
STOP	Load Status Register and Stop	Immediate Data → SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) - (Source) → Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) - (Source) → Destination	-	-	-	-	-
SUBI	Subtract Immediate	(Destination) - Immediate Data → Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) - Immediate Data → Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) - (Source) - X → Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16] ↔ Register [15:0]	-	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested → CC; 1 → [7] OF Destination	-	*	*	0	0
TRAP	Trap	PC → -(SSP); SR → -(SSP) -; (Vector) → PC	-	-	-	-	-
TRAPV	Trap on Overflow	If V then TRAP	-	-	-	-	-
TST	Test an Operand	(Destination) Tested → CC	-	*	*	0	0
UNLK	Unlink	An → SP; (SP)+ → An	-	-	-	-	-

* affected 0 cleared U undefined - unaffected 1 set [] = bit number d = displacement

- fetched. The operation word is in the instruction decoder.
- In the case of multi-word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
 - The last fetch from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
 - If the instruction is a single-word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch. In the case of

an interrupt or trace exception, both words are not used.

- 5) The program counter usually points to the last word fetched from the instruction stream.

cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is also included with the timing data. This data is enclosed in parenthesis following the execution periods and is shown as: (r/w) where r is the number of read cycles and w is the number of write cycles.

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that the memory cycle time is 4 clock periods. Any wait states caused by a longer memory

NOTE

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS CALCULATION TIMING

Table 24

	Addressing Mode	Byte, Word	Long
	Register		
Dn	Data Register Direct	0(0/0)	0(0/0)
An	Address Register Direct	0(0/0)	0(0/0)
	Memory		
(An)	Address Register Indirect	4(1/0)	8(2/0)
(An)+	Address Register Indirect with Postincrement	4(1/0)	8(2/0)
-(An)	Address Register Indirect with Predecrement	6(1/0)	10(2/0)
d(An)	Address Register Indirect with Displacement	8(2/0)	12(3/0)
d(An,ix)*	Address Register Indirect with Index	10(2/0)	14(3/0)
xxx.W	Absolute Short	8(2/0)	12(3/0)
xxx.L	Absolute Long	12(3/0)	16(4/0)
d(PC)	Program Counter with Displacement	8(2/0)	12(3/0)
d(PC,ix)*	Program Counter with Index	10(2/0)	14(3/0)
#xxx	Immediate	4(1/0)	8(2/0)

*The size of the index register (ix) does not affect execution time.

MOVE BYTE AND WORD INSTRUCTION CLOCK PERIODS

Table 25

Source	Destination								
	Dn	An	(An)	(An)+	-(An)	d(An)	d(An,ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
An	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
(An)	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
(An)+	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
-(An)	10(2/0)	10(2/0)	14(2/1)	14(2/1)	14(2/1)	18(3/1)	20(3/1)	18(3/1)	22(4/1)
d(An)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(An,ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
xxx.W	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
xxx.L	16(4/0)	16(4/0)	20(4/1)	20(4/1)	20(4/1)	24(5/1)	26(5/1)	24(5/1)	28(6/1)
d(PC)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(PC,ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
#xxx	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)

*The size of the index register (ix) does not affect execution time.



MOVE LONG INSTRUCTION CLOCK PERIODS

Table 26

Source	Destination								
	Dn	An	(An)	(An)+	-(An)	d(An)	d(An,ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	12(1/2)	12(1/2)	14(1/2)	16(2/2)	18(2/2)	18(2/2)	20(3/2)
An	4(1/0)	4(1/0)	12(1/2)	12(1/2)	14(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
(An)	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
(An)+	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
-(An)	14(3/0)	14(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
d(An)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
d(An,ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.W	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
xxx.L	20(5/0)	20(5/0)	28(5/2)	28(5/2)	28(5/2)	32(6/2)	34(6/2)	32(6/2)	36(7/2)
d(PC)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(5/2)
d(PC,ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
#xxx	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)

*The size of the index register (ix) does not affect execution time.

STANDARD INSTRUCTION CLOCK PERIODS

Table 27

Instruction	Size	op <ea>, An	op <ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) +**	6(1/0) +**	12(1/2) +
AND	Byte, Word	-	4(1/0) +	8(1/1)+
	Long	-	6(1/0) +**	12(1/2)+
CMP	Byte, Word	6(1/0)+	4(1/0) +	-
	Long	6(1/0) +	6(1/0) +	-
DIVS	-	-	158(1/0) +*	-
DIVU	-	-	140(1/0) +*	-
EOR	Byte, Word	-	4(1/0)***	8(1/1)+
	Long	-	8(1/0)***	12(1/2) +
MULS	-	-	70(1/0) +*	-
MULU	-	-	70(1/0) +*	-
OR	Byte, Word	-	4(1/0) +	8(1/1) +
	Long	-	6(1/0) +**	12(1/2) +
SUB	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) +**	6(1/0) +**	12(1/2) +

+ add effective address calculation time

* indicates maximum value

** total of 8 clock periods for instruction if the effective address is register direct

*** only available effective address mode is data register direct

DIVS, DIVU - The divide algorithm used by the MK68000 provides less than 10% difference between the best and worst case timings

MULS, MULU - The multiply algorithm requires $38 + 2n$ clocks, where n is defined as:

MULU: n = the number of ones in the <ea>

MULS: n = concatenate of the <ea> with a zero as the LSB; n is the resultant number of 10 or 01 patterns in the 17-bit source; i.e., worst case happens when the source is \$5555

IMMEDIATE INSTRUCTION CLOCK PERIODS

Table 28

Instruction	Size	op #, Dn	op #, M	op #, An
ADDI	Byte, Word	8(2/0)	12(2/1) +	-
	Long	16(3/0)	20(3/2) +	-
ADDQ	Byte, Word	4(1/0)	8(1/1) +	8(1/0)*
	Long	8(1/0)	12(1/2) +	8(1/0)
ANDI	Byte, Word	8(2/0)	12(2/1) +	-
	Long	16(3/0)	20(3/1) +	-
CMPI	Byte, Word	8(2/0)	8(2/0) +	8(2/0)**
	Long	14(3/0)	12(3/0) +	14(3/0)
EORI	Byte, Word	8(2/0)	12(2/1) +	-
	Long	16(3/0)	20(3/2) +	-
MOVEQ	Long	4(1/0)	-	-
ORI	Byte, Word	8(2/0)	12(2/1) +	-
	Long	16(3/0)	20(3/2) +	-
SUBI	Byte, Word	8(2/0)	12(2/1) +	-
	Long	16(3/0)	20(3/2) +	-
SUBQ	Byte, Word	4(1/0)	8(1/1) +	8(1/0)*
	Long	8(1/0)	12(1/2) +	8(1/0)

+ add effective address calculation time

*word only

** uses CMPA instruction and only supports word or long word immediate values

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 29

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NBCD	Byte	6(1/0)	8(1/1) +
NEG	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NEGX	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NOT	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
S _{CC}	Byte, False	4(1/0)	8(1/1) +
	Byte, True	6(1/0)	8(1/1) +
TAS	Byte	4(1/0)	10(1/1) +
TST	Byte, Word	4(1/0)	4(1/0)
	Long	4(1/0)	4(1/0) +

+ add effective address calculation time

VI

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 30

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	-
LSR, LSL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	-
ROR, ROL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	-
ROXR, ROXL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	-

+ add effective address calculation time
n is the shift or rotate count

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 31

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	-	$8(1/1)+$	-	$12(2/1)+$
	Long	$8(1/0)*$	-	$12(2/0)*$	-
BCLR	Byte	-	$8(1/1)+$	-	$12(2/1)+$
	Long	$10(1/0)*$	-	$14(2/0)*$	-
BSET	Byte	-	$8(1/1)+$	-	$12(2/1)+$
	Long	$8(1/0)*$	-	$12(2/0)*$	-
BTST	Byte	-	$4(1/0)+$	-	$8(2/0)+$
	Long	$6(1/0)$	-	$10(2/0)$	-

+ add effective address calculation time
* indicates maximum value

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 32

Instruction	Displacement	Trap or Branch Taken	Trap or Branch Not Taken
B _{CC}	Byte	$10(2/0)$	$8(1/0)$
	Word	$10(2/0)$	$12(2/0)$
BRA	Byte	$10(2/0)$	-
	Word	$10(2/0)$	-
BSR	Byte	$18(2/2)$	-
	Word	$18(2/2)$	-
DB _{CC}	CC true	-	$12(2/0)$
	CC false	$10(2/0)$	$14(3/0)$
CHK	-	$40(5/3)+ *$	$8(1/0)+$
TRAP	-	$34(4/3)$	-
TRAPV	-	$34(5/3)$	$4(1/0)$

+ add effective address calculation time
* indicates maximum value

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 33

Instr	Size	(An)	(An)+	-(An)	d(An)	d(An,ix)+	xxx.W	xxx.L	d(PC)	d(PC,ix)*
JMP	-	8(2/0)	-	-	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	-	16(2/2)	-	-	18(2/2)	22(2/2)	18(2/2)	20(3/2)	18(2/2)	22(2/2)
LEA	-	4(1/0)	-	-	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	-	12(1/2)	-	-	16(2/2)	20(2/2)	16(2/2)	20(3/2)	16(2/2)	20(2/2)
MOVEM	Word	12 + 4n (3 + n/0)	12 + 4n (3 + n/0)	-	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)	16 + 4n (4 + n/0)	20 + 4n (5 + n/0)	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)
	M→R Long	12 + 8n (3 + 2n/0)	12 + 8n (3 + 2n/0)	-	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)	16 + 8n (4 + 2n/0)	20 + 8n (5 + 2n/0)	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)
MOVEM	Word	8 + 5n (2/n)	-	8 + 5n (2/n)	12 + 5n (3/n)	14 + 5n (3/n)	12 + 5n (3/n)	16 + 5n (4/n)	-	-
	R→M Long	8 + 10n (2/2n)	-	8 + 10n (2/2n)	12 + 10n (3/2n)	14 + 10n (3/2n)	12 + 10n (3/2n)	16 + 10n (4/2n)	-	-

n is the number of registers to move

* is the size of the index register (ix) does not affect the instruction's execution time

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 24 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 25 and 26 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as: (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 27 indicates the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 27, the headings have the following meanings. An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 28 includes the

time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 28, the headings have the following meanings: # = immediate operand, Dn = data register operand, M = memory operand, and An = address register operand.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 29 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 34

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
CMPM	Byte, Word	-	12(3/0)
	Long	-	20(5/0)
SUBX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
ABCD	Byte	6(1/0)	18(3/1)
SBCD	Byte	6(1/0)	18(3/1)

be added to those of the effective address calculation where indicated.

be added to those of the effective address calculation where indicated.

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 31 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 35

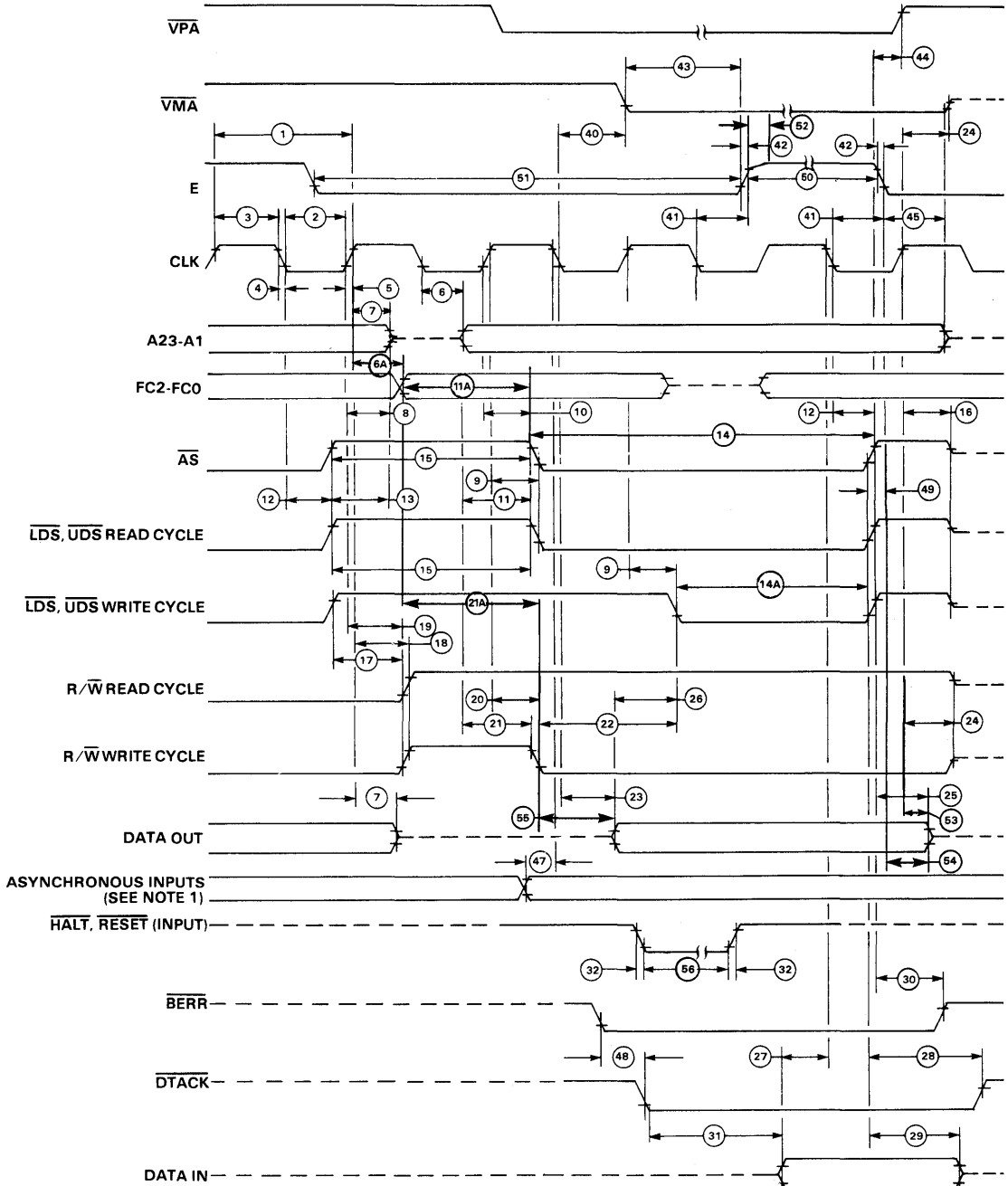
Instruction	Size	Register	Memory	Register → Memory	Memory → Register
ANDI to CCR	Byte	20(3/0)	-	-	-
ANDI to SR	Word	20(3/0)	-	-	-
EORI to CCR	Byte	20(3/0)	-	-	-
EORI to SR	Word	20(3/0)	-	-	-
ORI to CCR	Byte	20(3/0)	-	-	-
ORI to SR	Word	20(3/0)	-	-	-
MOVE from SR	-	6(1/0)	8(1/1)+	-	-
MOVE to CCR	-	12(2/0)	12(2/0)+	-	-
MOVE to SR	-	12(2/0)	12(2/0)+	-	-
MOVEP	Word	-	-	16(2/2)	16(4/0)
	Long	-	-	24(2/4)	24(6/0)
EXG	-	6(1/0)	-	-	-
EXT	Word	4(1/0)	-	-	-
	Long	4(1/0)	-	-	-
LINK	-	16(2/2)	-	-	-
MOVE from USP	-	4(1/0)	-	-	-
MOVE to USP	-	4(1/0)	-	-	-
NOP	-	4(1/0)	-	-	-
RESET	-	132(1/0)	-	-	-
RTE	-	20(5/0)	-	-	-
RTR	-	20(5/0)	-	-	-
RTS	-	16(4/0)	-	-	-
STOP	-	4(0/0)	-	-	-
SWAP	-	4(1/0)	-	-	-
UNLK	-	12(3/0)	-	-	-

+ add effective address calculation time

AC ELECTRICAL WAVEFORMS

Figure 36

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



VI

NOTE 1: Setup time for the asynchronous inputs \overline{BERR} , \overline{BGACK} , \overline{BR} , \overline{DTACK} , $\overline{IPL0}$ - $\overline{IPL2}$, and \overline{VPA} guarantees their recognition at the next falling edge of the clock.

NOTE 2: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

cycles must be added to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 33 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 34 indicates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 34, the headings have the following meanings: Dn = data register operand and M = memory operand.

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 35 indicates the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

EXCEPTION PROCESSING CLOCK PERIODS

Table 36 indicates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as: (r/w).

EXCEPTION PROCESSING CLOCK PERIODS

Table 36

Exception	Periods
Address Error	50(4/7)
Bus Error	50(4/7)
Interrupt	44(5/3)*
Illegal Instruction	34(4/3)
Privileged Instruction	34(4/3)
Trace	34(4/3)

*The interrupt acknowledge bus cycle is assumed to take four external clock periods

AC ELECTRICAL SPECIFICATIONS

($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$; $V_{SS} = 0 \text{ Vdc}$; $T_A = 0^\circ\text{C}$ to 70°C , Figure 34)

No.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		Unit
			MK68000-4		MK68000-6		MK68000-8		MK68000-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	250	500	167	500	125	500	100	500	ns
2	Clock Width Low	t_{CL}	115	250	75	250	55	250	45	250	ns
3	Clock Width High	t_{CH}	115	250	75	250	55	250	45	250	ns
4	Clock Fall Time	t_{Cf}	-	10	-	10	-	10	-	10	ns
5	Clock Rise Time	t_{Cr}	-	10	-	10	-	10	-	10	ns
6	Clock Low to Address	t_{CLAV}	-	90	-	80	-	70	-	55	ns
6A	Clock High to FC Valid	t_{CHFCV}	-	90	-	80	-	70	-	60	ns
7	Clock High to Address/Data High Impedance (maximum)	t_{CHAZx}	-	120	-	100	-	80	-	70	ns
8	Clock High to Address/FC Invalid (minimum)	t_{CHAZn}	0	-	0	-	0	-	0	-	ns
9 ¹	Clock High to \overline{AS} , \overline{DS} Low (maximum)	t_{CHSLx}	-	80	-	70	-	60	-	55	ns
10	Clock High to \overline{AS} , \overline{DS} Low (minimum)	t_{CHSLn}	0	-	0	-	0	-	0	-	ns
11 ²	Address to \overline{AS} , \overline{DS} (read) Low/ \overline{AS} Write	t_{AVSL}	55	-	35	-	30	-	20	-	ns
11A ²	FC valid to \overline{AS} , \overline{DS} (read) Low/ \overline{AS} Write	t_{FCVSL}	80	-	70	-	60	-	50	-	ns
12 ¹	Clock Low to \overline{AS} , \overline{DS} High	t_{CLSH}	-	90	-	80	-	70	-	55	ns
13 ²	\overline{AS} , \overline{DS} High to Address/FC Invalid	t_{SHAZ}	60	-	40	-	30	-	20	-	ns
14 ²	\overline{AS} , \overline{DS} Width Low (read)/ \overline{AS} Write	t_{SL}	535	-	337	-	240	-	195	-	ns
14A ²	\overline{DS} Width Low (Write)	-	285	-	170	-	115	-	95	-	ns
15 ²	\overline{AS} , \overline{DS} Width High	t_{SH}	285	-	180	-	150	-	105	-	ns
16	Clock High to \overline{AS} , \overline{DS} High Impedance	t_{CHSZ}	-	120	-	100	-	80	-	70	ns
17 ²	\overline{AS} , \overline{DS} High to R/ \overline{W} High	t_{SHRH}	60	-	50	-	40	-	20	-	ns
18 ¹	Clock High to R/ \overline{W} High (maximum)	t_{CHRHx}	-	90	-	80	-	70	-	60	ns
19	Clock High to R/ \overline{W} High (minimum)	t_{CHRHn}	0	-	0	-	0	-	0	-	ns
20 ¹	Clock High to R/ \overline{W} Low	t_{CHRL}	-	90	-	80	-	70	-	60	ns
20A	\overline{AS} Low to R/ \overline{W} Valid	t_{ASRV}	-	20	-	20	-	20	-	20	ns
21 ²	Address/Valid to R/ \overline{W} Low	t_{AVRL}	45	-	25	-	20	-	0	-	ns

AC ELECTRICAL SPECIFICATIONS (Continued)
 $V_{CC} = 5.0 \text{ Vdc} \pm 5\%$; $V_{SS} = 0 \text{ Vdc}$; $T_A = 0^\circ\text{C}$ to 70°C , Figure 34)

No.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		Unit
			MK68000-4		MK68000-6		MK68000-8		MK68000-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
21A ²	FC Valid to R/ \overline{W} Low	t_{FCVRL}	80	-	70	-	60	-	50	-	ns
22 ²	R/ \overline{W} Low to \overline{DS} Low (write)	t_{RLSL}	200	-	140	-	80	-	50	-	ns
23	Clock Low to Data Out Valid	t_{CLDO}	-	90	-	80	-	70	-	55	ns
24	Clock High to R/ \overline{W} , \overline{VMA} High Impedance	t_{CHRZ}	-	120	-	100	-	80	-	70	ns
25 ²	\overline{DS} High to Data Out Invalid	t_{SHDO}	60	-	40	-	30	-	20	-	ns
26 ²	Data Out Valid to \overline{DS} Low (write)	t_{DOSL}	55	-	35	-	30	-	20	-	ns
27 ⁵	Data In to Clock Low (set up time)	t_{DICL}	30	-	25	-	15	-	10	-	ns
28 ²	\overline{AS} , \overline{DS} High to \overline{DTACK} High	t_{SHDAH}	0	490	0	325	0	245	0	190	ns
29	\overline{DS} High to Data Invalid (hold time)	t_{SHDI}	0	-	0	-	0	-	0	-	ns
30	\overline{AS} , \overline{DS} High to \overline{BERR} High	t_{SHBEH}	0	-	0	-	0	-	0	-	ns
31 ^{2,5}	\overline{DTACK} Low to Data In (setup time)	t_{DALDI}	-	180	-	120	-	90	-	65	ns
32	\overline{HALT} and \overline{RESET} Input Transition Time	t_{RHrf}	0	200	0	200	0	200	0	200	ns
33	Clock High to \overline{BG} Low	t_{CHGL}	-	90	-	80	-	70	-	60	ns
34	Clock High to \overline{BG} High	t_{CHGH}	-	90	-	80	-	70	-	60	ns
35	\overline{BR} Low to \overline{BG} Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	clk. per.
36	\overline{BR} High to \overline{BG} High	t_{BRHGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37	\overline{BGACK} Low to \overline{BG} High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37A	\overline{BGACK} Low to \overline{BR} High (to Prevent Rearbitration)	t_{BGKBR}	30	-	25	-	20	-	20	-	ns
38	\overline{BG} Low to Bus High Impedance (with \overline{AS} high)	t_{GLZ}	-	120	-	100	-	80	-	70	ns
39	\overline{BG} Width High	t_{GH}	1.5	-	1.5	-	1.5	-	1.5	-	clk. per.
40	Clock Low to \overline{VMA} Low	t_{CLVML}	-	90	-	80	-	70	-	70	ns
41	Clock Low to E Transition	t_{CLE}	-	100	-	85	-	70	-	55	ns
42	E Output Rise and Fall Time	t_{Erf}	-	25	-	25	-	25	-	25	ns
43	\overline{VMA} Low to E High	t_{VMLEH}	325	-	240	-	200	-	150	-	ns
44	\overline{AS} , \overline{DS} High to \overline{VPA} High	t_{SHVPH}	0	240	0	160	0	120	0	90	ns
45	E Low to Address/ \overline{VMA} /FC Invalid	t_{ELAI}	55	-	35	-	30	-	10	-	ns
46	\overline{BGACK} Width	t_{BGL}	1.5	-	1.5	-	1.5	-	1.5	-	clk. per.
47 ⁵	Asynchronous Input Setup Time	t_{ASI}	30	-	25	-	20	-	20	-	ns

AC ELECTRICAL SPECIFICATIONS (Continued)

($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$; $V_{SS} = 0 \text{ Vdc}$; $T_A = 0^\circ\text{C}$ to 70°C , Figure 34)

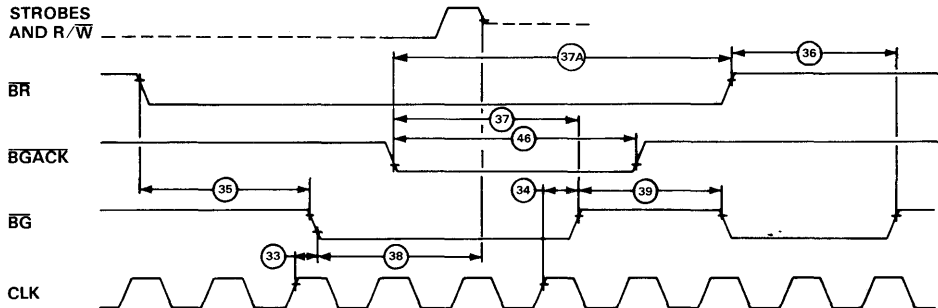
No.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		Unit
			MK68000-4		MK68000-6		MK68000-8		MK68000-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
48 ³	$\overline{\text{BERR}}$ Low to $\overline{\text{DTACK}}$ Low	t_{BELDAL}	50	-	50	-	50	-	50	-	ns
49	E Low to $\overline{\text{AS}}$, $\overline{\text{DS}}$ Invalid	t_{ELSI}	-80	-	-80	-	-80	-	-80	-	ns
50	E Width High	t_{EH}	900	-	600	-	450	-	350	-	ns
51	E Width Low	t_{EL}	1400	-	900	-	700	-	550	-	ns
52	E Extended Rise Time	t_{CIEHX}	80	-	80	-	80	-	80	-	ns
53	Data Hold from Clock High	t_{CHDO}	0	-	0	-	0	-	0	-	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	60	-	40	-	30	-	20	-	ns
55	R/ $\overline{\text{W}}$ to Data bus Impedance change	t_{RLDO}	55	-	35	-	30	-	20	-	ns
56	Halt/ $\overline{\text{RESET}}$ Pulse Width (Note 4)	t_{HRPW}	10	-	10	-	10	-	10	-	clk. per.

NOTES:

- For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.
- Actual value depends on actual clock period.
- If #47 is satisfied for both $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$, #48 may be 0 ns.
- After V_{CC} has been applied for 100 ms.
- If the asynchronous setup time (#47) requirements are satisfied, the $\overline{\text{DTACK}}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) for the following cycle.

AC ELECTRICAL WAVEFORMS - BUS ARBITRATION

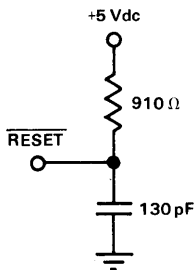
Figure 37



These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

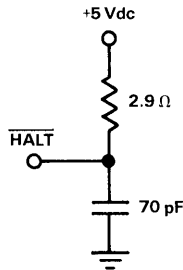
RESET TEST LOAD

Figure 38



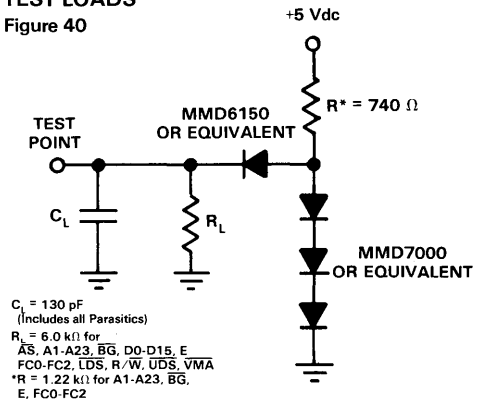
HALT TEST LOAD

Figure 39



TEST LOADS

Figure 40



DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$; $V_{SS} = 0 \text{ Vdc}$; $T_A = 0^\circ\text{C}$ to 70°C , Figures 35, 36, 37)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	0.8	Vdc
Input Leakage Current @ 5.25 V	I_{in} BERR, BGACK, BR, VPA, DTACK, CLOCK, IFL0-IFL2, HALT, RESET	- -	2.5 20	μAdc
Three-State (Off State) Input Current @ 2.4 V/0.4 V	I_{Tst} AS, A1-A23, D0-D15, FC0-FC2, LDS, R/W, UDS, VMA	-	20	μAdc
Output High Voltage ($I_{OH} = -400 \mu\text{Adc}$)	V_{OH} AS, A1-A23, BG, E*** D0-D15, E, FC0-FC2, LDS, R/W, UDS, VMA E*	2.4	- $V_{CC} - 0.75$	Vdc
Output Low Voltage ($I_{OL} = 1.6\text{mA}$) ($I_{OL} = 3.2\text{mA}$) ($I_{OL} = 5.0\text{mA}$) ($I_{OL} = 5.3\text{mA}$)	V_{OL} HALT A1-A23, BG, FC0-FC2 RESET E, AS, D0-D15, LDS, R/W, UDS, VMA	- - - -	0.5 0.5 0.5 0.5	Vdc
Power Dissipation (Clock Frequency = 8 MHz)****	P_D	-	1.5	W
Capacitance (Package Type Dependent) ($V_{in} = 0 \text{ Vdc}$; $T_A = 25^\circ\text{C}$; Frequency = 1 MHz**)	C_{in}	-	20.0	pF

*with external pullup resistor of $1.1\text{K} \Omega$

**capacitance is periodically sampled rather than 100% tested

***without external pullup resistor

****During normal operation instantaneous V_{CC} current requirements may lbe as high as LSA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to + 7.0	Vdc
Input Voltage	V_{in}	-0.3 to + 7.0	Vdc
Operating Temperature	T_A	0 to 70	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 150	$^\circ\text{C}$

MK68000 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX. CLOCK FREQUENCY	TEMPERATURE RANGE
MK68000P-4	Ceramic	4.0 MHz	0° to 70°C
MK68000P-6	Ceramic	6.0 MHz	
MK68000P-8	Ceramic	8.0 MHz	
MK68000P-10	Ceramic	10.0 MHz	