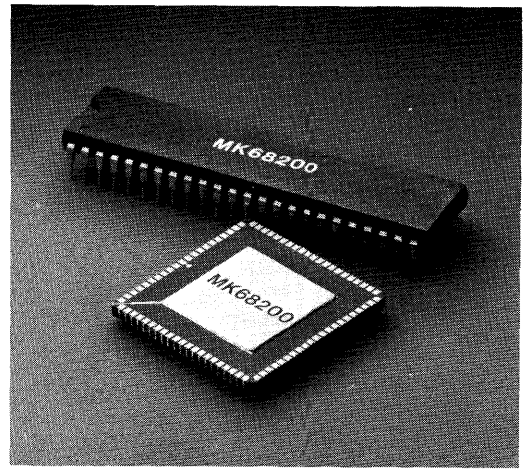
PRELIMINARY

68200 16-BIT SINGLE-CHIP MICROCOMPUTERS MK68201/MK68E201/MK68211/MK68E211

FEATURES

- ☐ 16-bit, high performance, single-chip microcomputer
- ☐ 14 address and data registers
  - Eight 16-bit or sixteen 8-bit data registers
  - Six 16-bit address registers
- ☐ Advanced 16-bit instruction set
  - Bit, byte, and word operands
  - Nine addressing modes
  - Byte and word BCD arithmetic
- ☐ High performance (6 MHz instruction clock)
  - 500 ns register-to-register move or add
  - 3.5 μs 16 x 16 multiply
  - 4.0 μs 32/16 divide
- ☐ Available with 0 or 4K (2K x 16) bytes of ROM
- ☐ 256 byte RAM (128 x 16)
- ☐ Three 16-bit timers
  - Interval modes
  - Event modes
  - One-shot modes
  - Pulse and period measurement modes
  - Two input and two output pins
- ☐ Serial channel
  - Double-buffered receive and transmit
  - Asynchronous to 375 Kbps
  - Synchronous to 1.5 Mbps
  - Address wake-up recognition and generation
  - Internal/external baud rate generation
- ☐ Parallel I/O
  - Up to 40 pins
  - Direction programmable by bit
  - One 16-bit or two 8-bit port(s) with handshaking
- ☐ Interrupt controller
  - 16 independent vectors
  - Eight external interrupt sources
  - One non-maskable interrupt
  - Individual interrupt masking

MK68200
Figure 1

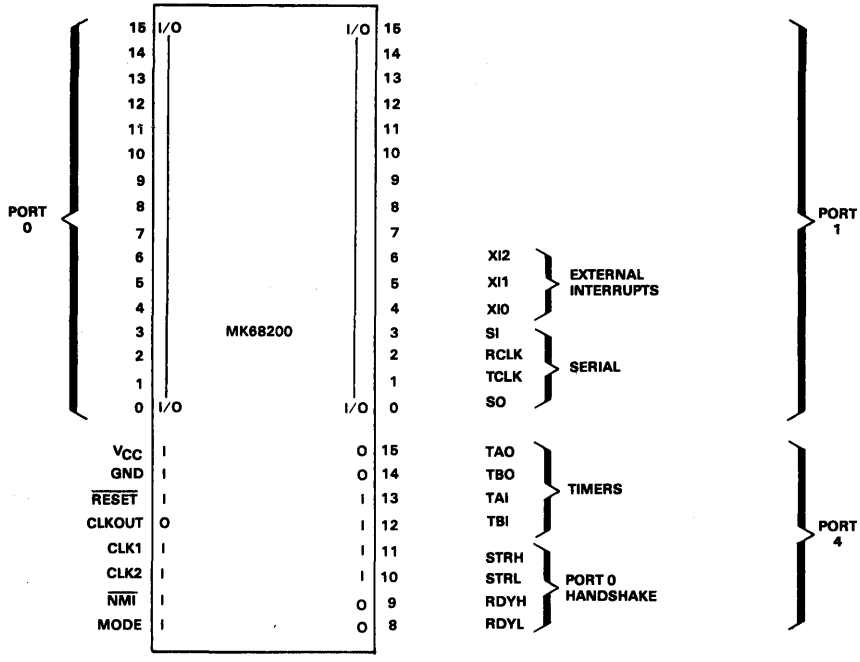


- ☐ Optional external bus
  - 16-bit, multiplexed address/data bus
  - Automatic bus request/grant arbitration
  - Two control bus versions:
    - 68000-compatible bus (UPC)
    - General Purpose Bus (GP)
- ☐ 8 and 12 MHz time base versions produce 4 and 6 MHz instruction clock rates, respectively.
  - Crystal or external TTL clock
- ☐ Single +5 volt power supply
- ☐ 48-pin DIP or 84-pin LCC

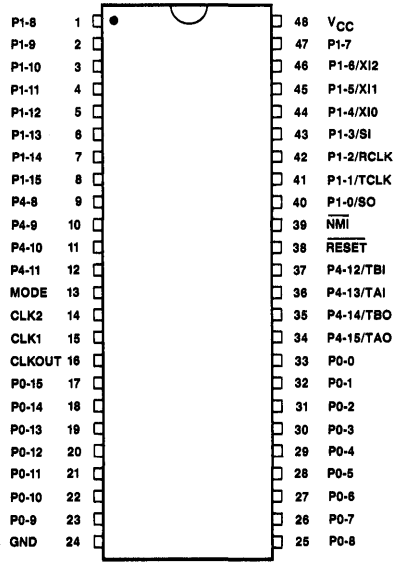
GENERAL DESCRIPTION

MK68200 designates a series of new, high-performance, 16-bit, single-chip microcomputers from Mostek. Implemented in Scaled Poly-5 NMOS, they incorporate an architecture designed for superior performance in computation-intensive control applications. A modern, comprehensive instruction set, which features both high speed execution and code space efficiency, is combined on-chip along with extensive, flexible I/O capabilities. On-chip RAM and optional on-chip ROM are provided within a full 64K byte addressing space.

MK68200 LOGICAL PINOUT SINGLE-CHIP MODE
Figure 2



MK68200 SINGLE-CHIP PIN ASSIGNMENT (48-PIN DIP)
Figure 3



The MK68200 is designed to serve the needs of a wide variety of control applications, which require high performance operation with a minimal parts count implementation. Industrial controls, instrumentation, and intelligent computer peripheral controls are all examples of applications served by the MK68200. High speed mathematical ability, rapid I/O addressing and interrupt response, and powerful bit manipulation instructions provide the necessary tools for these applications. In addition to its single-chip microcomputer configuration, both distributed intelligence and parallel multiprocessing system configurations are supported by the MK68200, as illustrated in Figures 12 and 13.

In applications requiring loosely coupled, distributed intelligence, several MK68200's may be interconnected on a common serial network. The on-chip USART supports a wake-up mode in which an additional bit is appended to the data stream to distinguish a serial data word as address or data. The wake-up logic prevents the serial channel from generating interrupts unless a specific address is recognized.

Alternately, the MK68200 may be configured as an expandable CPU device which can access external memory and I/O resources. In this operating mode, parallel I/O pins are replaced by multiplexed address/data and control lines. Bus arbitration logic is incorporated on the chip to support a direct interface in parallel shared bus multiprocessor system configurations. Two versions exist which support two types of control signals present on the expanded bus configuration. The General Purpose (GP) bus option allows the MK68200 to operate either as an executive or a peripheral processor. As an executive procesor, the MK68200 can control an external system bus and grant the use of it to requesting devices, such as DMA controllers and/or peripheral processors. As a peripheral control processor, the MK68200 can provide intelligent local control of an I/O device in a computer system and, thereby, relieve the executive processor of these tasks. In this configuration, the MK68200 has the capability of effectively performing DMA transfers between system memory and the I/O device. The on-chip resources of ROM, RAM, and I/O are accessed within the MK68200 without affecting the utilization of the shared system bus so that only external communications compete for bus bandwidth.

The Universal Peripheral Controller (UPC) bus option supports a direct interface to a 68000 executive processor. Thus, the MK68200 can be used as a cost-effective, intelligent peripheral controller in 68000 systems. The UPC version's direct bus interface to the 68000 makes the MK68200 particularly well-suited for performing many intelligent I/O functions in a 68000 system. For example, since the MK68200 includes both a serial channel and an external bus capable of performing DMA transfers, it can be programmed to act as serial protocol controller with DMA capability, as shown in Figure 4.

Table 1 summarizes the specific MK68200 device types that are discussed in this data sheet. A complete guide to the part numbering scheme used throughout this document may be found in the Ordering Information section. All MK68200 devices retain most of the I/O features when they are used in the expanded bus mode; however, 24 pins of parallel I/O are sacrificed when this mode is used. When the expanded bus mode is selected, the MK68201/XX generates UPC (68000-compatible) control signals, while the MK68211/XX generates GP control signals. Also available are 84-pin emulator versions of these devices that do not have on-chip ROM, but instead have additional pins to support a second complete address/data bus to access off-chip ROM, RAM, EPROM, or I/O devices. This bus is referred to as the private bus and is not bonded out on 48-pin versions.

For additional information on the MK68200, refer to the MK68200 Principles of Operation Manual, publication number 4420399, and to the MK68200 Programming Reference Guide, publication number 4420465.

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SINGLE-CHIP DESCRIPTION

Figure 2 is a diagram which illustrates the functions of specific pins for a MK68201 or MK68211, operating in a single-chip mode. When the device is operating in one of the expanded bus modes, the pins on Port 0 become the multiplexed address/data bus, and the upper half of Port 1 becomes the control signals (GP or UPC) for the bus. The following description applies to the pins only when the device is used in the non-expanded or single-chip mode. Descriptions of the pin functions for the expanded bus modes may be found in the Expanded Bus Operation section of this data sheet.

V_{CC}, GND
(Power, Ground)
Power Supply pins.
(single +5 V)

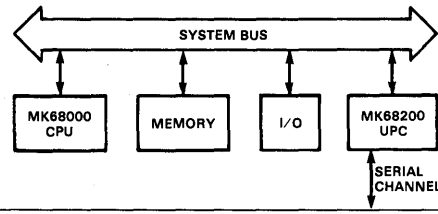
$\overline{\text{RESET}}$
Input, active low. $\overline{\text{RESET}}$ input overrides ongoing execution (including interrupts) and resets the chip to its initial power-up condition. $\overline{\text{RESET}}$ cannot be masked.

CLKOUT
(Clock Output)
Output. CLKOUT will output the instruction clock rate, which is one-half of the frequency provided on CLK1 and CLK2.

CLK1, CLK2
(Time base Inputs)
Inputs. CLK1 and CLK2 may be connected to a crystal, or CLK1 may be connected to an external TTL-compatible oscillator while CLK2 is left floating. The

SERIAL DMA CONTROLLER

Figure 4



DEVICE TYPE SUMMARY

Table 1

Device Type	Expanded Bus Version	ROM (Bytes)	RAM (Bytes)	PKG.
MK68201/04	UPC	0	256	48-pin DIP
MK68201/44	UPC	4096	256	48-pin DIP
MK68E201/04	UPC	0	256	84-pin LCC
MK68211/04	GP	0	256	48-pin DIP
MK68211/44	GP	4096	256	48-pin DIP
MK68E211/04	GP	0	256	84-pin LCC

instruction clock rate is one-half of the frequency provided on CLK1 and CLK2.

$\overline{NMI}$
(Non-Maskable Interrupt)
Input, active low, negative edge triggered. The NMI request line has a higher priority than all of the maskable interrupts. NMI is always enabled regardless of whether the L1E (Level 1 Interrupt Enable) bit is set in the Status Register.

MODE
Input. The MODE pin is used to configure the MK68200 on power-up and reset to one of the following states:

Mode Pin
V_{CC} - No expansion (single chip mode)
GND - Partial Expansion
CLKOUT - Full Expansion

P0-0 - P0-15
(Port 0)
Input/Output. Each bit in Port 0 may be individually programmed for general purpose input or output. Port 0 also has several handshaking modes to allow parallel, asynchronous communication with other devices. The high and low bytes may be programmed individually or jointly to be inputs, outputs, or bidirectional.

P1-0 - P1-15
(Port 1)
Input/Output. Each of the 16 bits in Port 1 may be individually programmed for input or output. Additionally, the lowest seven bits of Port 1 may be programmed to serve specific alternate functions, as listed below.

P1-6/XI2
(External Interrupt 2)
Input, rising or falling edge triggered. The programmer may select the rising or falling edge as active for XI2.

P1-5/XI1
(External Interrupt 1)
Input, fixed falling edge triggered. The XI1 interrupt may be used to interrupt the MK68200 on the falling edge of an input pulse.

P1-4/$\overline{XI0}$
(External Interrupt 0)
Input, low level triggered. The XI0 interrupt input is level-triggered (unlike XI1, XI2). It may be used to produce an internally vectored interrupt or to cause an external fetch of an interrupt vector number when the MK68200 is used in an expanded mode with the GP bus.

P1-3/SI
(Serial Input)
Input, active high. SI is used to input receive serial data when the receiver is enabled.

P1-2/RCLK
(Receive Clock)
Input/Output, active high. Depending on the mode programmed, RCLK can be used by the serial port as either an input or an output pin. When used as an input pin, RCLK provides the receive clock and/or the transmit clock. When RCLK is not providing the transmit or receive clock, it can be used as an output for Timer C. In this mode, the receive clock is being provided by Timer C.

P1-1/TCLK
(Transmit-Clock)
Input/Output, active high. Depending on the mode programmed, TCLK can be used by the serial port as either an input or an output pin. When used as an input pin, TCLK provides the transmit clock. When TCLK is not providing the transmit clock, it can be used as an output for Timer C. In this mode, the transmit clock is being provided by either Timer C or RCLK.

P1-1/SO
(Serial Output)
Output, active high. SO is used to output transmit serial data when the transmitter is enabled.

P4-8 - P4-15
(Port 4)
Inputs and Outputs. P4-8, P4-9, P4-14, and P4-15 may be used as general purpose outputs, and P4-10, P4-11, P4-12, and P4-13 may be used as general purpose inputs. Interrupts may be generated on the positive transitions on P4-10 and P4-11. Depending on the mode selected, interrupts may be generated on the positive or negative transitions on P4-12, or they may be generated on the positive, negative, or combined transitions on P4-13. Additionally, these bits may be programmed to serve specific alternate functions, as listed below.

P4-15/TAO
(Timer A Output)
Output. TAO may be programmed for special functions in the interval, event, and pulse modes for Timer A. In the interval mode, TAO's state is determined by the Timer A latch (high or low) that is currently active. That is, if the counter is using the high latch for comparison, TAO is high. If the counter is using the low latch for comparison, TAO is low. In the event mode, TAO is initialized to a "1" state and toggles each time the counter matches the Timer A high latch. In the pulse/period modes, TAO is initiated to a "1" state and toggles on positive transitions on TAI.

P4-14/TBO
(Timer B Ouput)
Output. TBO may be programmed for special functions in the interval and one-shot modes for Timer B. In the interval mode, TBO is initialized to a "1" state and toggles each time the counter matches the Timer B latch value. In the one-shot modes, TBO is initialized to a "1" state, and the counter begins counting in response to the occurrence of an active edge on TBI. TBO will not go low until the counter matches the value loaded into the Timer B latch.

P4-13/TAI
(Timer A Input)
Input, positive and/or negative edge triggered. TAI may be programmed for special functions in the event mode or pulse/period modes for Timer A. In the event mode, the counter is incremented on each active transition (positive or negative edge programmable) on TAI. In the pulse/period modes, the counter measures the time during which the signal on TAI remains high and low.

P4-12/TBI
(Timer B Input)
Input, positive or negative edge triggered. TBI may be programmed for special functions for the Timer B one-shot modes. In the one-shot modes, TBI acts as a trigger input

P4-11/STRH, P4-10/STRL
(Strobe High Byte, Strobe Low Byte)
Input, active high. STRH and STRL are both used for input, output, and bidirectional handshaking on Port 0.

1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the MK68200.

2) Input mode: The stobe is issued by the peripheral to load data from the peripheral into the Port 0 input register. Data is latched into the MK68200 on the negative edge of this signal.

3) Bidirectional mode: When the STRH signal is active, data from the Port 0 output register is gated onto the Port 0 bidirectional data bus.

The negative edge of STRH acknowledges the receipt of the output data. The negative edge of the signal applied to the STRL signal is used to latch input data into Port 0.

P4-9/RDYH, P4-8/RDYL
(Ready High Byte, Ready Low Byte)
Output, active high. RDYH and RHYL are used for input, output, and bidirectional handshaking on Port 0.

1) Output mode: The ready signal goes active to indicate that the Port 0 output register has been loaded, and the peripheral data is stable and ready for transfer to the peripheral device.

2) Input mode: The ready signal is active when the Port 0 input register is empty and is ready to accept data from the peripheral device.

3) Bidirectional mode: The RDYH signal is active when data is available in Port 0 output register for transfer to the peripheral device. In this mode, data is not placed on the Port 0 data bus unless STRH is active. The RDYL signal is active when the Port 0 input register is empty and is ready to accept data. from the peripheral device.

PROCESSOR ARCHITECTURE

The MK68200 microcomputer contains an advanced processor architecture, combining the best properties of both 8- and 16-bit processors. Thus a large majority of instructions operate on either byte or word operands. A block diagram shown in Figure 5 summarizes the internal architecture of the MK68200.

REGISTERS

The MK68200 register set includes three system registers, six address registers, and eight data registers. The three 16-bit system registers, as shown in Figure 6, include a Program Counter, a Status Register, and a Stack Pointer. The six address registers may be used either for 16-bit data or for memory addressing. The eight 16-bit data registers are used for data and may also be referenced as sixteen 8-bit registers, providing great flexibility in register allocation.

ADDRESSING

The MK68200 directly addresses a 64K byte memory space, which is organized as 32K 16-bit words. The memory is byte-addressable, but most transfers occur 16 bits at a time for increased performance over 8-bit microcomputers. All input/output is memory-mapped, and the on-chip I/O is situated in the top 1K bytes of the address space. In the single-chip mode, all resources including ROM, RAM, and I/O, are accessed via an internal or private bus. The memory map, which is accessed by this bus in the single-chip mode, is depicted in Figure 7.

Nine addressing modes provide ease of access to data in the MK68200, as depicted in Table 2. The four register indirect forms utilize the address registers and the Stack Pointer and support many common data structures such as arrays, stacks, queues, and linked lists. I/O Port addressing is a short form addressing mode for the first 16 words of the I/O port space and allows most instructions to access the most often referenced I/O ports in just one word. Many microcomputer applications are I/O intensive and short, fast addressing of I/O has a significant impact on performance.

INSTRUCTION SET

The MK68200 instruction set has been designed with regularity and ease of programming in mind. In addition, instructions have been encoded to minimize code space, a feature which is especially important in single-chip microcomputers. Small code space is related to execution speed, and most instructions execute in either three or six instruction clock periods. (An instruction clock period is equal to 167 ns with a 6 MHz instruction clock). See Table 3.

In addition to operations on bytes and words, the MK68200 has rapid bit manipulation instructions that can operate on registers, memory, and ports. The bit to be affected may be an immediate operand of the instruction, or it may be dynamically specified in a register. Operations available include bit set, clear, test, change, and exchange; and all bit operations perform a bit test as well. Since each instruction is indivisible, this provides the necessary test-and-set function for the implementation of semaphores.

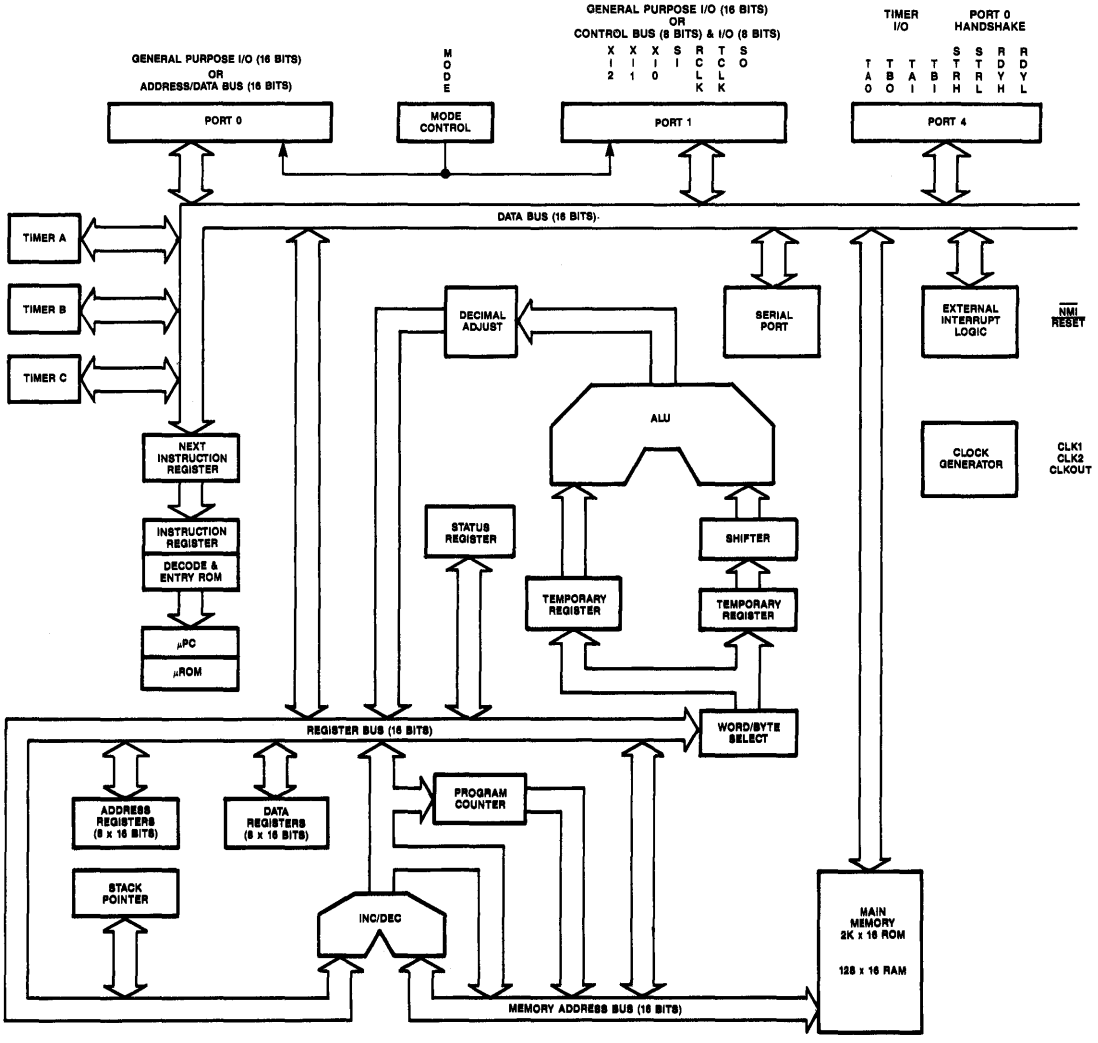
The MOVE group of instructions has the most extensive capabilities. A wide variety of addressing mode combinations is supported including memory-to-memory transfers. A special move multiple is included to save and restore a specified portion of the registers rapidly.

In total, the MK68200 instruction set provides a programming environment, similar to the 68000, which has been optimized for the needs of the single-chip microcomputer marketplace. A summary of the instruction set is provided in Table 4.

ADDRESSING MODES
Table 2

Register
Register Indirect
Register Indirect with Post-increment
Register Indirect with Pre-decrement
Register Indirect with Displacement
Program Counter Relative
Memory Absolute
Immediate
I/O Port

MK68200 BLOCK DIAGRAM
Figure 5



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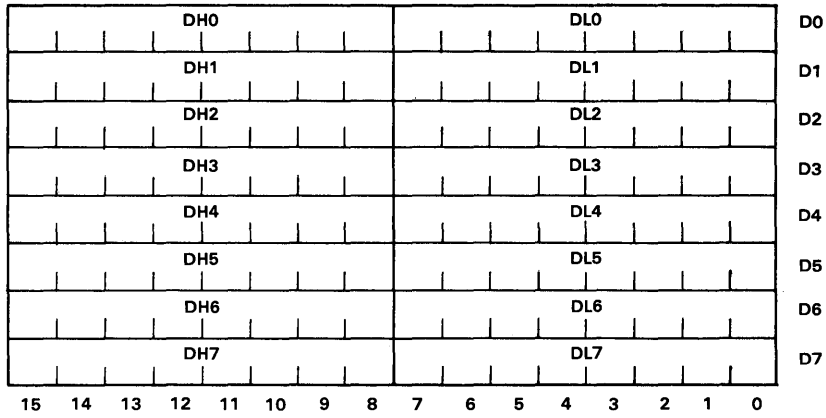
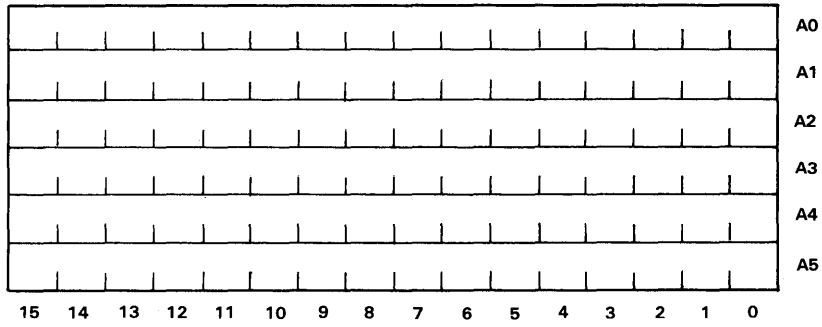
REGISTER SET

Figure 6

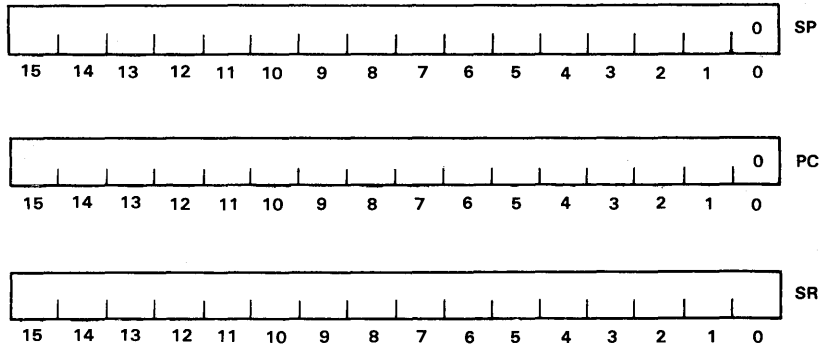
DATA REGISTERS:



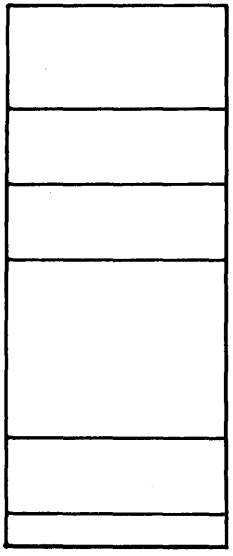
ADDRESS REGISTERS:



SYSTEM REGISTERS:



ADDRESSING SPACE FOR SINGLE-CHIP CONFIGURATION
Figure 7



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INSTRUCTION EXECUTION TIMES
Table 3

Instruction Type	Clock Periods	Execution Time with 6 MHz clock (μs)
Move Register-to-register	3	0.5
Add Register-to-register (binary or BCD)	3	0.5
Move Memory-to-register	6	1.0
Add Register-to-memory	9	1.5
Multiply (16 x 16)	21	3.5
Divide (32/16)	23	3.84
Move Multiple (save or restore all registers)	55	9.2

INSTRUCTION SET SUMMARY

Table 4

INST.	DESCRIPTION	INST.	DESCRIPTION
ADD	ADD	HALT	HALT
ADD.B	ADD BYTE	JMPA	JUMP ABSOLUTE
ADDC	ADD WITH CARRY	JMPR	JUMP RELATIVE
ADDC.B	ADD WITH CARRY BYTE	LIBA	LOAD INDEXED BYTE ADDRESS
AND	LOGICAL AND	LIWA	LOAD INDEXED WORD ADDRESSED
AND.B	LOGICAL AND BYTE	LSR	LOGICAL SHIFT RIGHT
ASL	ARITHMETIC SHIFT LEFT	LSR.B	LOGICAL SHIFT RIGHT BYTE
ASL.B	ARITHMETIC SHIFT LEFT BYTE	MOVE	MOVE
ASR	ARITHMETIC SHIFT RIGHT	MOVE.B	MOVE BYTE
ASR.B	ARITHMETIC SHIFT RIGHT BYTE	MOVEM	MOVE MULTIPLE REGISTERS
BCHG	BIT CHANGE	MOVEM.B	MOVE MULTIPLE REGISTERS BYTE
BCLR	BIT CLEAR	MULS	MULTIPLY SIGNED
BEXG	BIT EXCHANGE	MULU	MULTIPLY UNSIGNED
BSET	BIT SET	NEG	NEGATE
BTST	BIT TEST	NEG.B	NEGATE BYTE
CALLA	CALL ABSOLUTE	NEGC	NEGATE WITH CARRY
CALLR	CALL RELATIVE	NEGC.B	NEGATE WITH CARRY BYTE
CLR	CLEAR	NOP	NO OPERATION
CLR.B	CLEAR BYTE	NOT	ONE'S COMPLEMENT
CMP	COMPARE	NOT.B	ONE'S COMPLEMENT BYTE
CMP.B	COMPARE BYTE	OR	LOGICAL OR
DADD	DECIMAL ADD	OR.B	LOGICAL OR BYTE
DADD.B	DECIMAL ADD BYTE	POP	POP
DADDC	DECIMAL ADD WITH CARRY	POPM	POP MULTIPLE REGISTERS
DADDC.B	DECIMAL ADD WITH CARRY BYTE	PUSH	PUSH
DI	DISABLE INTERRUPTS	PUSHM	PUSH MULTIPLE REGISTERS
DIVU	DIVIDE UNSIGNED	RET	RETURN FROM SUBROUTINE
DJNZ	DECREMENT COUNT AND JUMP IF NON-ZERO	RETI	RETURN FROM INTERRUPT
		ROL	ROTATE LEFT
DJNZ.B	DECREMENT COUNT BYTE AND JUMP IF NON-ZERO	ROL.B	ROTATE LEFT BYTE
		ROLC	ROTATE LEFT THROUGH CARRY
DNEG	DECIMAL NEGATE	ROLC.B	ROTATE LEFT THROUGH CARRY BYTE
DNEG.B	DECIMAL NEGATE BYTE		
DNEGC	DECIMAL NEGATE WITH CARRY	ROR	ROTATE BYTE
DNEGC.B	DECIMAL NEGATE WITH CARRY BYTE	ROR.B	ROTATE RIGHT BYTE
		RORC	ROTATE RIGHT THROUGH CARRY
DSUB	DECIMAL SUBTRACT	RORC.B	ROTATE RIGHT THROUGH CARRY BYTE
DSUB.B	DECIMAL SUBRTRACT BYTE		
DSUBC	DECIMAL SUBTRACT WITH CARRY	SUB	SUBTRACT
DSUBC.B	DECIMAL SUBTRACT WITH CARRY BYTE	SUB.B	SUBTRACT BYTE
		SUBC	SUBTRACT WITH CARRY
EI	ENABLE INTERRUPTS	SUBC.B	SUBTRACT WITH CARRY BYTE
EOR	EXCLUSIVE OR	TEST	TEST
EOR.B	EXCLUSIVE OR BYTE	TEST.B	TEST BYTE
EXG	EXCHANGE	TESTN	TEST NOT
EXG.B	EXCHANGE BYTE	TESTN.B	TEST NOT BYTE
EXT	EXTEND SIGN		

INPUT/OUTPUT ARCHITECTURE

The I/O capabilities of the MK68200 are extensive, encompassing timers, a serial channel, parallel I/O, and an interrupt controller. All of these devices are accessible to the programmer as ports within the top 1K bytes of the address space, and the most commonly accessed ports may be accessed with the short port addressing mode. A description of these ports is given in Table 5.

In total, 40 pins out of the 48 are used for I/O, and the functions they perform are highly programmable by the user. In particular, many pins can perform multiple functions, and the programmer selects which ones are to be used. For example, TAI may be used as an input for Timer A, an interrupt source, or a general purpose input pin, and the interrupt source may be selected simultaneously with either of the other functions.

PORT DESCRIPTIONS

Table 5

PORT	ADDRESS	READ/WRITE	BYTE-ADDRESSABLE	FUNCTION
0	$FC00	READ/WRITE	YES	16 EXTERNAL I/O PINS OR ADDRESS/DATA BUS
1	$FC02	READ/WRITE	YES	16 EXTERNAL I/O PINS (INCLUDING INTERRUPT, SERIAL I/O PINS, AND BUS CONTROL)
2	$FC04	—	—	(RESERVED)
3	$FC06	LOW BYTE: READ/WRITE HIGH BYTE: READ	YES	SERIAL TRANSMIT (LOW BYTE) AND RECEIVE (HIGH BYTE) BUFFER
4	$FC08	INPUTS: READ ONLY OUTPUTS: READ/WRITE	NO	8 EXTERNAL I/O PINS (TIMER CONTROL AND PORT 0 HANDSHAKE CONTROL)
5	$FC0A	—	—	(RESERVED)
6	$FC0C	—	—	(RESERVED)
7	$FC0E	READ/WRITE	NO	INTERRUPT LATCH REGISTER
8	$FC10	READ/WRITE	NO	INTERRUPT MASK REGISTER
9	$FC12	STATUS: READ ONLY CONTROL: READ/WRITE	NO	SERIAL I/O RECEIVE CONTROL AND STATUS
10	$FC14	STATUS: READ ONLY CONTROL: READ/WRITE	NO	SERIAL I/O TRANSMIT CONTROL AND STATUS
11	$FC16	READ GETS COUNTER WRITE GOES TO LATCH	NO	TIMER B LATCH
12	$FC18	READ GETS COUNTER OR LATCH WRITE GOES TO LATCH	NO	TIMER A, LOW LATCH
13	$FC1A	READ GETS COUNTER OR LATCH WRITE GOES TO LATCH	NO	TIMER A, HIGH LATCH
14	$FC1C	READ/WRITE	NO	TIMER CONTROL, INTERRUPT EDGE SELECT
15	$FC1E	READ/WRITE	NO	PORT 0 HANDSHAKE MODE BITS, FAST/STANDARD, BUS LOCK, BUS SEGMENT BITS
16	$FC20	READ/WRITE	NO	PORT 0 DIRECTION CONTROL (DDR0)
17	$FC22	READ/WRITE	NO	PORT 1 DIRECTION CONTROL (DDR1)
18	$FC24	READ/WRITE	NO	SERIAL I/O MODE AND SYNC REGISTER
19	$FC26	READ GETS COUNTER WRITE GOES TO LATCH AND COUNTER	NO	TIMER C LATCH

TIMERS

The MK68200 includes three on-chip timers, each with unique features. They are denoted Timer A, Timer B, and Timer C. All three timers are a full 16 bits in width, and count at the instruction clock rate of the MK68200 processor. Thus, this rate provides a resolution equal to the instruction clock period (tc) of the MK68200. The maximum count interval is equal to tc $*2^{16}$. For a 6 MHz MK68200, a 167 nanosecond clock is provided with a maximum count interval of 10.945 milliseconds. Each timer has the capability to interrupt the processor when it matches a predetermined value stored in an associated latch.

Timer A is capable of operating in interval, event, and two pulse/period modes. There is one 16-bit counter and two 16-bit latches (high and low) associated with Timer A. Once Timer A is initialized in the interval mode, the counter is reset, and then it increments at the instruction clock rate until the value loaded into the high latch is reached. The counter is then reset, and it increments until the low latch value is reached, and the cycle is repeated. In the event mode, the counter is incremented for every active edge on TAI (programmable as positive or negative) until the value in the high latch is reached, at which time the counter is reset, and the cycle repeats. In the pulse/period modes, the time that the pulse applied stays high and low is measured. The counter is reset on the occurrence of any transition on TAI, and it increments at the instruction clock rate until occurrence of the next transition. The value in the counter at the end of the high level or low level time is loaded into the appropriate latch. Interrupts may be generated each time the counter reaches the high latch or low latch value in the interval mode or when the counter reaches the high latch in the event mode. An interrupt is also generated whenever the counter overflows. See the Pin Description section of this data sheet for TAI and TAO functions in the various Timer A modes.

Timer B is capable of operating in interval and one-shot modes. There is one 16-bit counter and one 16-bit latch associated with Timer B. In the interval mode, the counter is initially reset and incremented at the instruction clock rate until the value in the latch is reached. The counter is then reset, and the cycle repeats. In the one-shot modes, the counter begins incrementing in response to an active transition (programmable as positive or negative) on TBI. The counter is reset when the value in the Timer B latch is reached. In the retriggerable one-shot mode, active transitions on TBI always cause the counter to reset and begin incrementing. In the non-retriggerable one-shot mode, active transitions on TBI have no effect until the counter reaches the latch value. Interrupts may be generated each time the counter reaches the latch value. See the Pin Description section of this data sheet for TBI and TBO functions in the various Timer B modes.

Timer C has a 16-bit down counter and latch associated with it and operates only in the interval mode. The output of Timer C toggles each time the counter value rolls over from 0 to the latch value and may be used to internally supply the baud rate clock for the serial port. An interrupt may also be generated each time the counter rolls over to the latch value. Timer C may be output on the TCLK pin (P1-3) depending on the mode programmed.

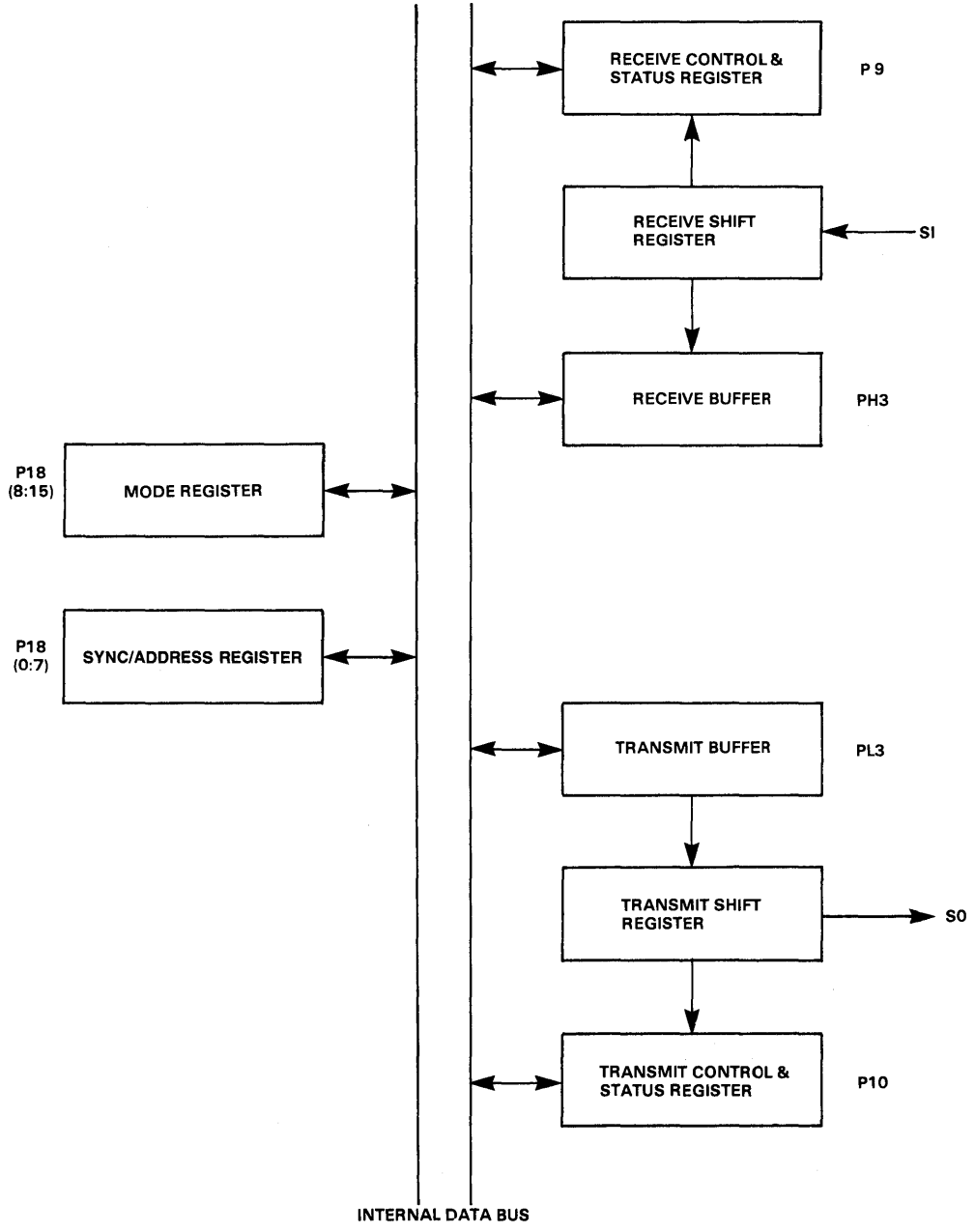
TIMER MODES
Table 6

Timer	Modes
A	Interval
A	Event
A	Pulse Width and Period Measurement
B	Interval
B	Retriggerable One-shot
B	Non-retriggerable One-shot
C	Interval
C	Baud Rate Generation

SERIAL CHANNEL

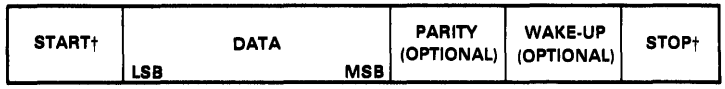
The serial channel on the MK68200, as shown in Figure 8, is a full-duplex USART with double buffering on both transmit and receive. Word length, parity, stop bits, and modes are fully programmable. The asynchronous mode supports bit rates up to 375 Kbps, and the byte synchronous mode operates up to 1.5 Mbps. Either internal or external clocks may be used.

SERIAL CHANNEL
Figure 8



In addition to the typical USART functions, the serial channel can operate in a special wake-up mode with a wake-up bit appended to each data word, as illustrated in Figure 9. This wake-up bit is used to differentiate normal data words and special address words. The receiver can be programmed to receive only address words or only address words with a specific data value. In this way, the processor can be interrupted only when it receives its particular address and can then change mode to receive the following data words. Wake-up capability is especially useful when several MK68200 microcomputers are interconnected on one serial link.

SERIAL FRAME FORMAT
Figure 9



†USED IN ASYNCHRONOUS MODE ONLY

PARALLEL I/O

Two 16-bit ports, P0 and P1, may be used for parallel I/O. If individual bits are desired, each of the 32 bits may be separately defined as input or output. Bits may be grouped to provide the exact data widths desired. Port 0 has the additional capability of operating under the control of external handshaking signals. Eight- or sixteen-bit sections of P0 may be individually controlled as input, output, or bidirectional I/O. Two pairs of Ready and Strobe signals, which are available as programmable options on Port 4, provide the necessary control.

INTERRUPT CONTROLLER

The MK68200 interrupt controller provides rapid service of up to 15 interrupt sources, each with a unique internal vector. The lowest 16 words of the address space contain the starting addresses of the service routines of each potential interrupt source and reset, as shown in Figure 10.

INTERRUPT AND RESET VECTORS
Figure 10

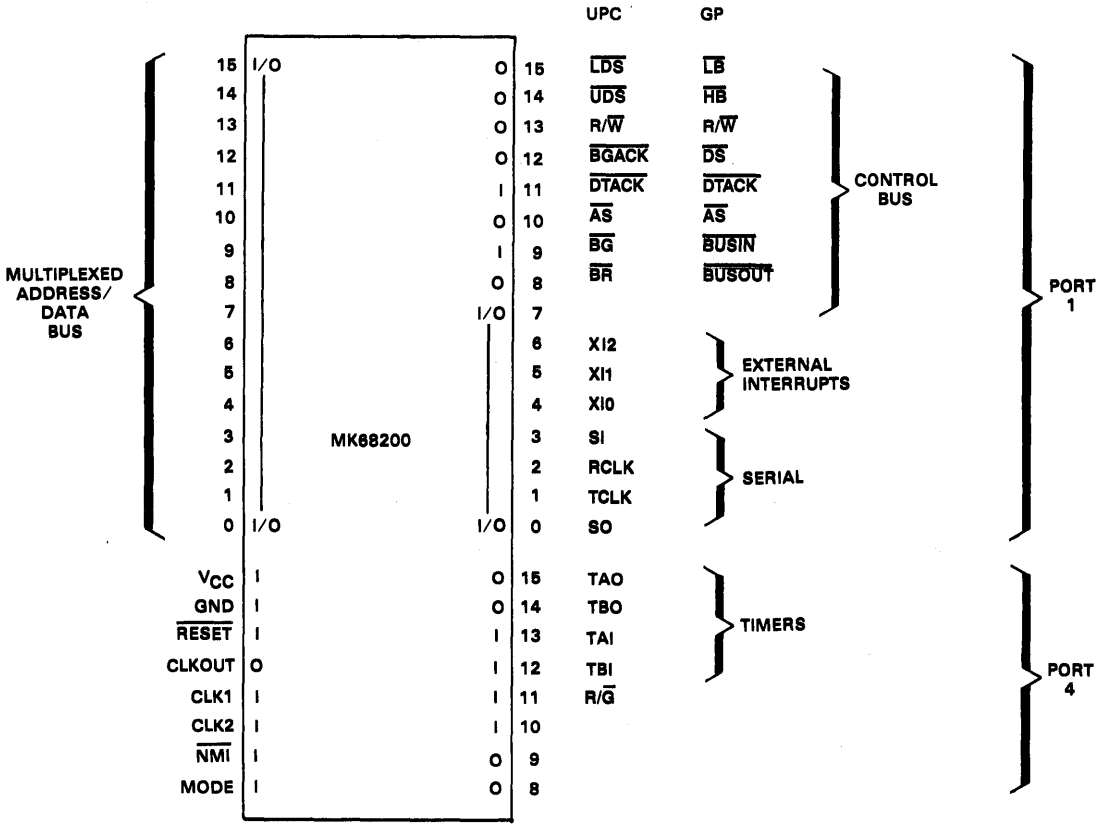
VECTOR NUMBER	NAME	MNEMONIC	VECTOR LOCATION	
0	RESET	RESET	0000	
1	NON-MASKABLE INTERRUPT	NMI	0002	LEVEL 2
2	SPARE	SPARE	0004	
3	EXTERNAL INTERRUPT 2	XI2	0006	
4	STROBE LOW	STRL	0008	
5	TIMER A OUTPUT	TAO	000A	
6	TIMER A INPUT	TAI	000C	
7	STROBE HIGH	STRH	000E	
8	RECEIVE SPECIAL CONDITION	RSC	0010	LEVEL 1
9	RECEIVE NORMAL	RN	0012	
A	EXTERNAL INTERRUPT 1	XI1	0014	
B	TIMER B OUTPUT	TBO	0016	
C	TIMER B INPUT	TBI	0018	
D	EXTERNAL INTERRUPT 0	XI0	001A	
E	TRANSMIT	XMT	001C	
F	TIMER C	TC	001E	

Interrupt sources and RESET are prioritized in the order shown in Figure 10, with RESET having the highest priority. NMI is the only non-maskable interrupt. All of the other sources share an interrupt enable bit in the processor Status Register. This bit is automatically cleared whenever an interrupt is acknowledged. Also, each of these sources has a corresponding individual mask bit. This feature allows selective masking of particular interrupts, including the ability to choose any priority scheme desired with only minimal software overhead. In fact, 15 levels of nested priority may be programmed.

EXPANDED BUS OPERATION

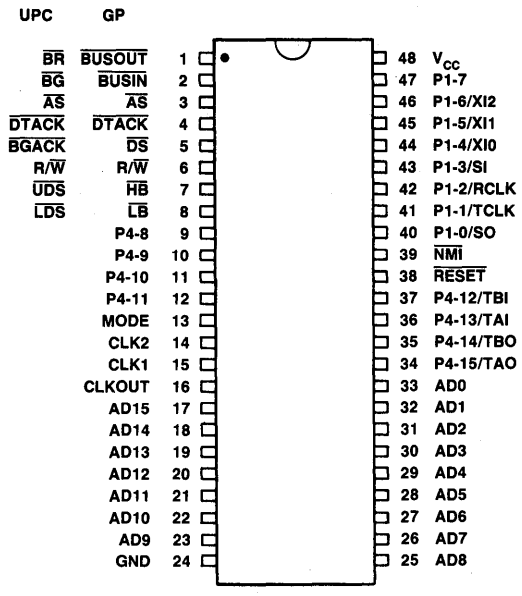
When it is necessary to expand beyond the on-chip complement of RAM, ROM, or I/O, or when operation in a parallel multiprocessing system is desired, the MK68200 may be placed in an external bus mode. The MODE pin is used to select the expansion capability on reset. The MODE pin has three states, which select fully expanded external bus, partially expanded external bus, or no expanded bus (single-chip configuration). The MK68200 may also be reconfigured dynamically through software. In an expansion mode, Port 0 becomes the 16-bit multiplexed, address/data bus, and eight bits from Port 1 become control signals which handle data transfer and bus arbitration. Sixteen lines are still available for I/O functions, including eight lines from Port 1 and all eight lines of Port 4.

MK68200 LOGICAL PINOUT EXPANDED BUS
Figure 11



MK68200 EXPANDED BUS

Figure 12

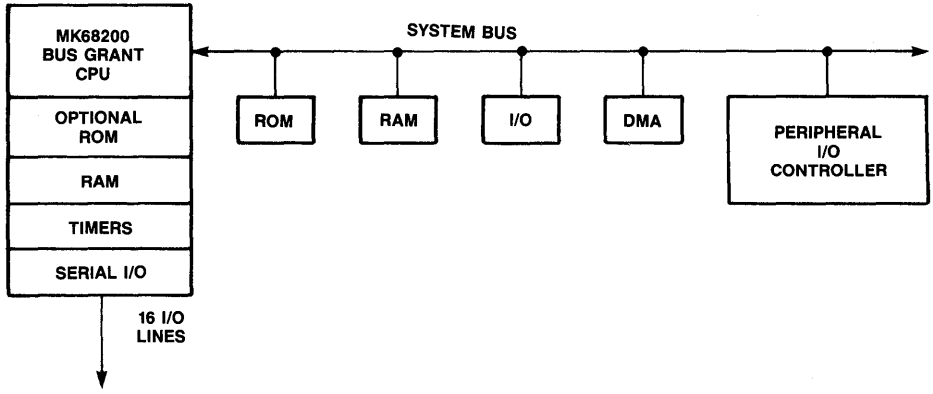


As shown in Figure 11, two different control bus versions are available : a Universal Peripheral Controller (UPC), which generates 68000-compatible signals, and a General Purpose (GP) bus, which can be used to interface to a wide variety of existing microprocessor buses. With the selection of an expanded bus mode, the MK68200 can act either as a general purpose CPU chip (bus grant device) or as an intelligent peripheral I/O controller to a host CPU (bus request device). These two system configurations are illustrated in Figures 13 and 14.

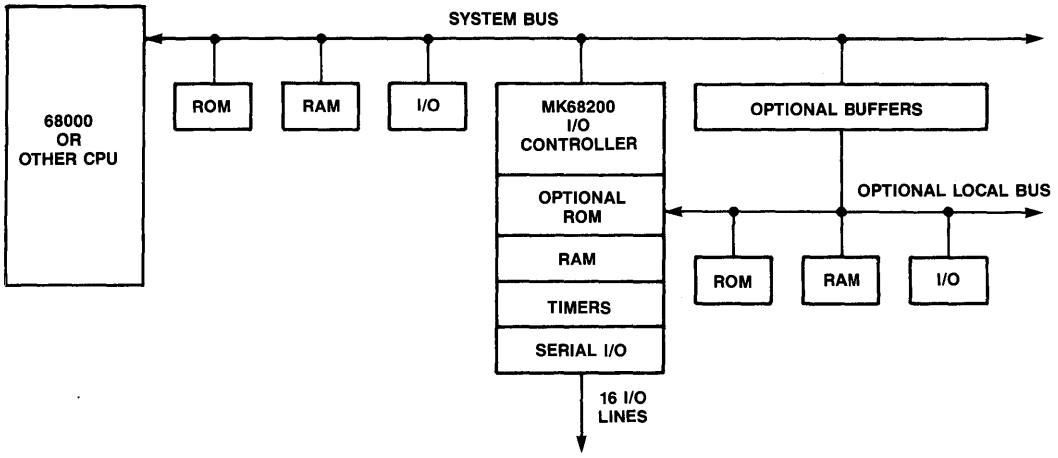
With the GP bus option, the user may configure the MK68200 in either of the two ways shown in Figures 13 and 14. As a host CPU (Figure 13), the MK68200 bus arbitration logic causes the device to act as the system bus grantor. In other words, the MK68200 would normally have control of the system bus and would grant its use to DMA devices or peripheral CPUs. Alternately, the MK68200 may be configured as a peripheral CPU (Figure 14) that must issue a request to the bus grant device before being allowed to use the system bus. The selection of one of these two configurations is accomplished by the P4-11 pin at reset time. During reset, P4-11 serves as the R/$\overline{G}$ input (0 = bus grantor, 1 = bus requestor). Following reset and at all times during program execution, P4-11 may be used as a general purpose input pin.

HOST CPU HARDWARE CONFIGURATION

Figure 13



PERIPHERAL I/O CONTROLLER CONFIGURATION
Figure 14

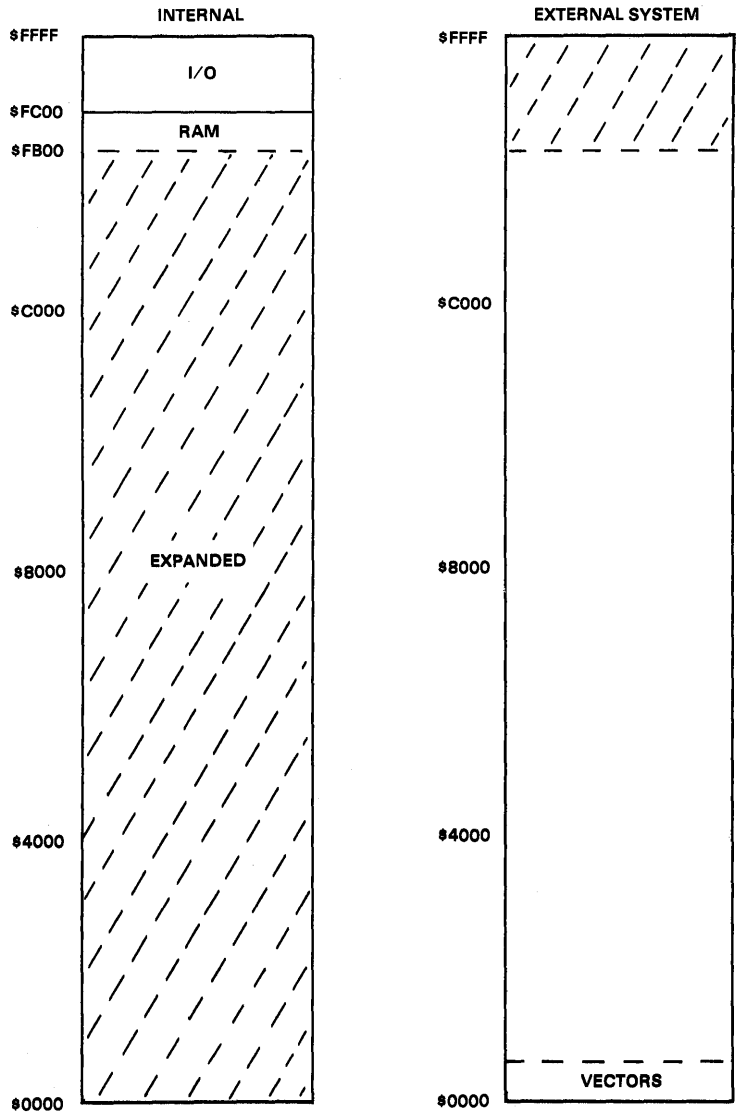


With the GP bus operating in the host CPU configuration, the MK68200 may be used to interface with external memory and I/O devices in a manner that is analogous to any general purpose microprocessor. Additionally, the MK68200 retains its on-chip RAM and I/O resources, with on-chip ROM as an option, depending on the expansion configuration selected. $\overline{\text{BUSIN}}$ and $\overline{\text{BUSOUT}}$ are used to perform the bus arbitration handshake function, where $\overline{\text{BUSIN}}$ acts as the bus request input and $\overline{\text{BUSOUT}}$ as the bus grant output.

In the full expansion configuration, any on-chip ROM which may exist on the device is disabled, and program memory starting at location $0000 is located off-chip and is addressed via the expanded bus, as shown in Figure 15. In effect, the internal bus from locations $0000-$FAFF is mapped onto the external bus. In the partially expanded configuration (Figure 16), on-chip ROM may be accessed on the internal bus. To gain greater addressability in the partial expansion configuration, a scheme is implemented to allow access of a full 64K-byte address space in four segments on the expanded system bus through the 16K byte "window" on the internal bus. Basically, the most significant two bits of address on the expanded bus are replaced with two user-defined segment bits available to the programmer in an internal I/O control port location.

As a peripheral I/O controller, the MK68200 operates as a bus requestor that gains mastership of the system bus from the bus grant CPU. The GP bus version may be selected to implement this system configuration in cases where an interface to a general purpose CPU is desired. In this case, the $\overline{\text{BUSIN}}$ and $\overline{\text{BUSOUT}}$ lines are again used to perform the bus arbitration handshake function, where $\overline{\text{BUSOUT}}$ now acts as bus request output, and $\overline{\text{BUSIN}}$ acts as bus grant input. In this configuration, the MK68200 can conceivably act as a complete peripheral I/O control subsystem on a single chip, with 16 lines of I/O and its on-chip ROM, RAM, timers, and serial I/O performing the necessary interface to the I/O device. The UPC bus version provides the peripheral I/O control function with a direct interface to a 68000 bus grant CPU. Note that the UPC bus version can operate only as a bus request device. Once the MK68200 has gained mastership of the system bus via the 68000 bus arbitration handshake lines ($\overline{\text{BR}}$, $\overline{\text{BG}}$, and $\overline{\text{BGACK}}$), it may proceed to perform DMA transfers and communicate with system memory or other I/O devices in the system.

FULL EXPANSION BUS GRANTOR MEMORY MAP
Figure 15



As in the case of the GP bus grant configuration, the portion of the internal (or private) bus address space that is mapped onto the expanded bus when the part is operating as either a GP or a UPC bus request device is determined by the expansion configuration selected. In the partial expansion bus requestor case, the resulting memory map is identical to that shown for the GP grant configuration in Figure 16. During the time the MK68200 is executing its program from ROM and accessing internal RAM and I/O resources, the expanded bus is held in a tri-state condition. The bus arbitration logic within the MK68200 monitors each memory reference to detect external bus addresses (referenced in segments via the 16K byte DMA window). Whenever such an external reference occurs, the logic automatically holds the processor in a wait state as it proceeds to obtain mastership of the bus. As soon as use of the system bus is obtained, the processor is allowed to continue the reference. This procedure is transparent to the programmer. In the case of successive external references, the expanded bus is retained until an internal reference is encountered.

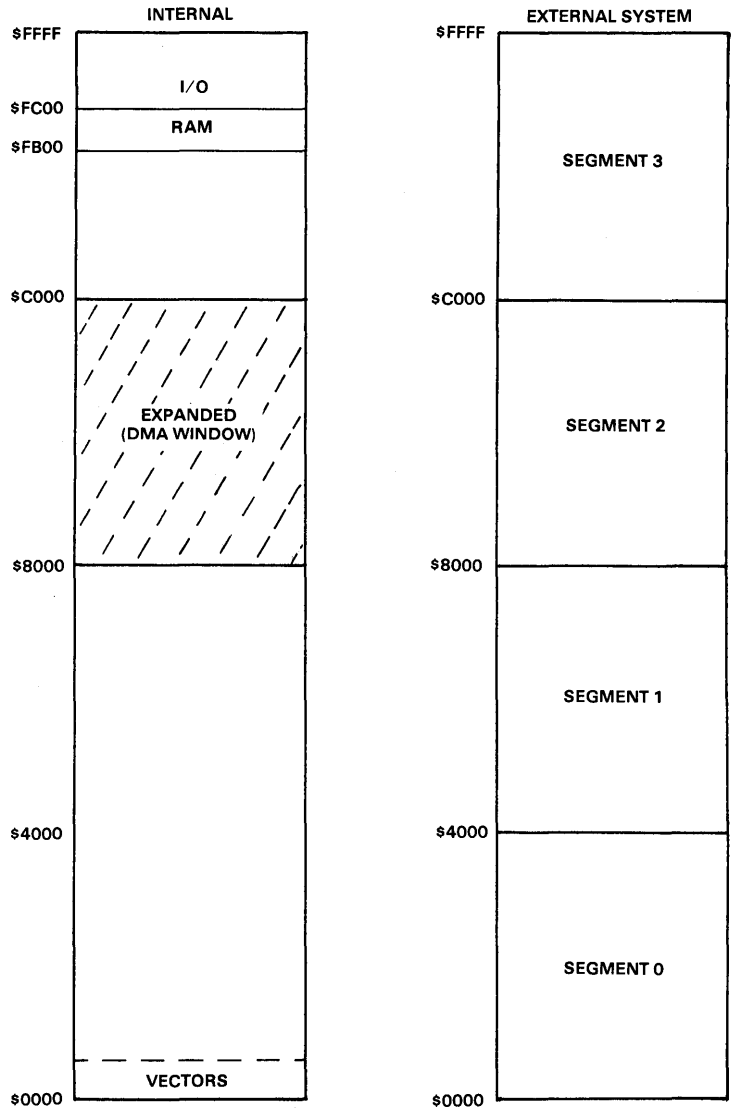
Finally, if the on-chip resources are insufficient to perform the control task in the bus requestor configuration, the internal bus address range (excluding on-chip RAM, I/O) may be mapped onto an external local bus, which is physically the same as the system bus but logically separated with bus buffers. This is the full expansion bus requestor configuration. The memory map for this configuration is shown in Figure 17. The bus arbitration sequence is still performed only when a reference to the system bus through the DMA window is made. In this manner, the I/O subsystem is isolated from the host CPU.

When operating as a bus request device, it is possible to retain the external bus for an indefinite period of time using a bus lock feature. This will help facilitate the transfer of large blocks of data. Thus, the on-chip bus arbitration logic allows a maximum amount of concurrent processing in parallel, multiprocessing configurations with a minimum of hardware and software overhead. The bus lock feature may be used by the MK68200 in a bus grantor mode to keep any peripheral from gaining mastership of the bus.

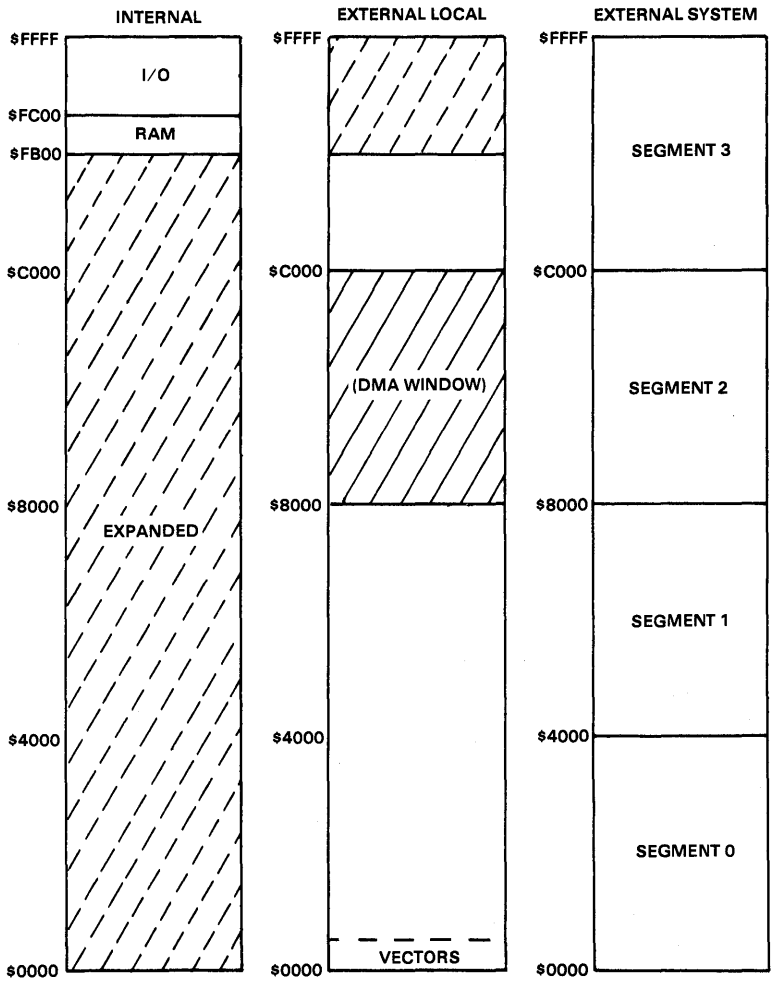
In any of the GP expanded bus modes, the MK68200 may respond to peripheral devices on the expanded bus which generate an interrupt request on XI0. The MK68200 will obtain the XI0 interrupt vector number from the requesting peripheral on the bus during an interrupt acknowledge cycle. When responding to an interrupt on XI0, the MK68200 will wait for the bus arbitration logic to gain control of the bus and then asserts neither $\overline{HB}$ nor $\overline{LB}$ while asserting $\overline{AS}$ to signify that an interrupt acknowledge cycle is in progress.

Timing diagrams and design parameters for the read, write, and bus arbitration cycles are given in the AC Electrical Specifications section for both the GP and the UPC bus options. Bus timing for the interrupt acknowledge cycle is given for the GP device in the AC Electrical Specifications section. There is a user-programmable speed selection associated with the read and write cycles for both the UPC and GP mask option parts. A bit in an internal I/O port allows the user to select either the standard or the fast read/write cycle on the expanded bus. The standard bus cycle is four clock periods, while the fast bus cycle is three clock periods.

PARTIAL EXPANSION MEMORY MAP
Figure 16



FULL EXPANSION BUS REQUESTOR MEMORY MAP
Figure 17



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EXPANDED BUS SIGNALS (Common for GP and UPC Options)

R/$\overline{W}$
(Read/Write)
Output, active high and low. R/$\overline{W}$ determines whether a read or a write is being performed during the current bus cycle. It is stable for the entire bus operation. A high signal denotes a read, and a low signal denotes a write.

$\overline{DTACK}$
(Data Transfer Acknowledge)
Input, active low. When the addressed device has either placed the requested read data on the bus or taken the write data from the bus, $\overline{DTACK}$ should be brought low to signify completion. The data portion of the bus cycle will be extended indefinitely until this signal is asserted. For systems using the GP bus, in which no devices need wait states, $\overline{DTACK}$ may be strapped low.

$\overline{AS}$
(Address Strobe)
Output, active low. $\overline{AS}$ is used to signify that the address is stable on the multiplexed bus. $\overline{AS}$ is high at the beginning of each bus cycle and goes low after the address has stabilized. It then returns to the high state near the end of the bus cycle.

UPC BUS SIGNALS

$\overline{UDS}$
(Upper Data Strobe)
Output, active low. $\overline{UDS}$ is used to signify the data portion of the bus cycle for the upper byte of the data bus. For read operations, $\overline{UDS}$ should be used by the external device to gate its most significant byte onto the multiplexed address/data bus. For writes, $\overline{UDS}$ signifies that the upper byte of the bus contains valid data to be written from the processor.

$\overline{LDS}$
(Lower Data Strobe)
Output, active low. $\overline{LDS}$ is used to signify the data portion of the bus cycle for the lower byte of the data bus. For read operations, $\overline{LDS}$ should be used by the external device to gate its least significant byte onto the multiplexed address/data bus. For writes, $\overline{LDS}$ signifies that the lower byte of the bus contains valid data to be written from the processor.

$\overline{BR}$
(Bus Request)
Output, active low, open drain. $\overline{BR}$ goes low when the MK68200 requires the use of the external bus as a bus master.

$\overline{BG}$
(Bus Grant)
Input, active low. $\overline{BG}$ notifies the MK68200 that it has been granted the external bus.

$\overline{BGACK}$
(Bus Grant Acknowledge)
Output, active low, open drain. The MK68200 will assert $\overline{BGACK}$ when it assumes mastership of the system bus.

GP BUS SIGNALS

P4-11 / R/$\overline{G}$
(Request/Grant)
During reset, P4-11 serves as the R/$\overline{G}$ input (0 = bus grantor, 1 = bus requestor). Following reset, and at all times during program execution, P4-11 may be used as a general purpose input pin.

$\overline{DS}$
(Data Strobe)
Output, active low. $\overline{DS}$ is used to signify the data portion of the bus cycle. For read operations, $\overline{DS}$ should be used by the external device to gate its contents onto the multiplexed address/data bus. For writes, $\overline{DS}$ signifies that valid data from the processor is on the bus.

$\overline{HB}$
(High Byte)
Output, active low. $\overline{HB}$ signifies that the upper byte of the data is to be read or written. It remains active for the entire bus cycle.

$\overline{LB}$
(Low Byte)
Output, active low. $\overline{LB}$ signifies that the lower byte of the data bus is to be read or written. (Both $\overline{HB}$ and $\overline{LB}$ active imply that an entire word is to be read or written). $\overline{LB}$ remains active for the entire bus cycle.

$\overline{BUSIN}$
(Bus Input)
Input, active low. $\overline{BUSIN}$ provides one of two functions: bus request or bus grant. When the MK68200 is the bus grant device, its $\overline{BUSIN}$ signal is a bus request input from a requesting device on the bus. When the MK68200 is a bus request device, its $\overline{BUSIN}$ signal is a bus grant from the granting device on the bus.

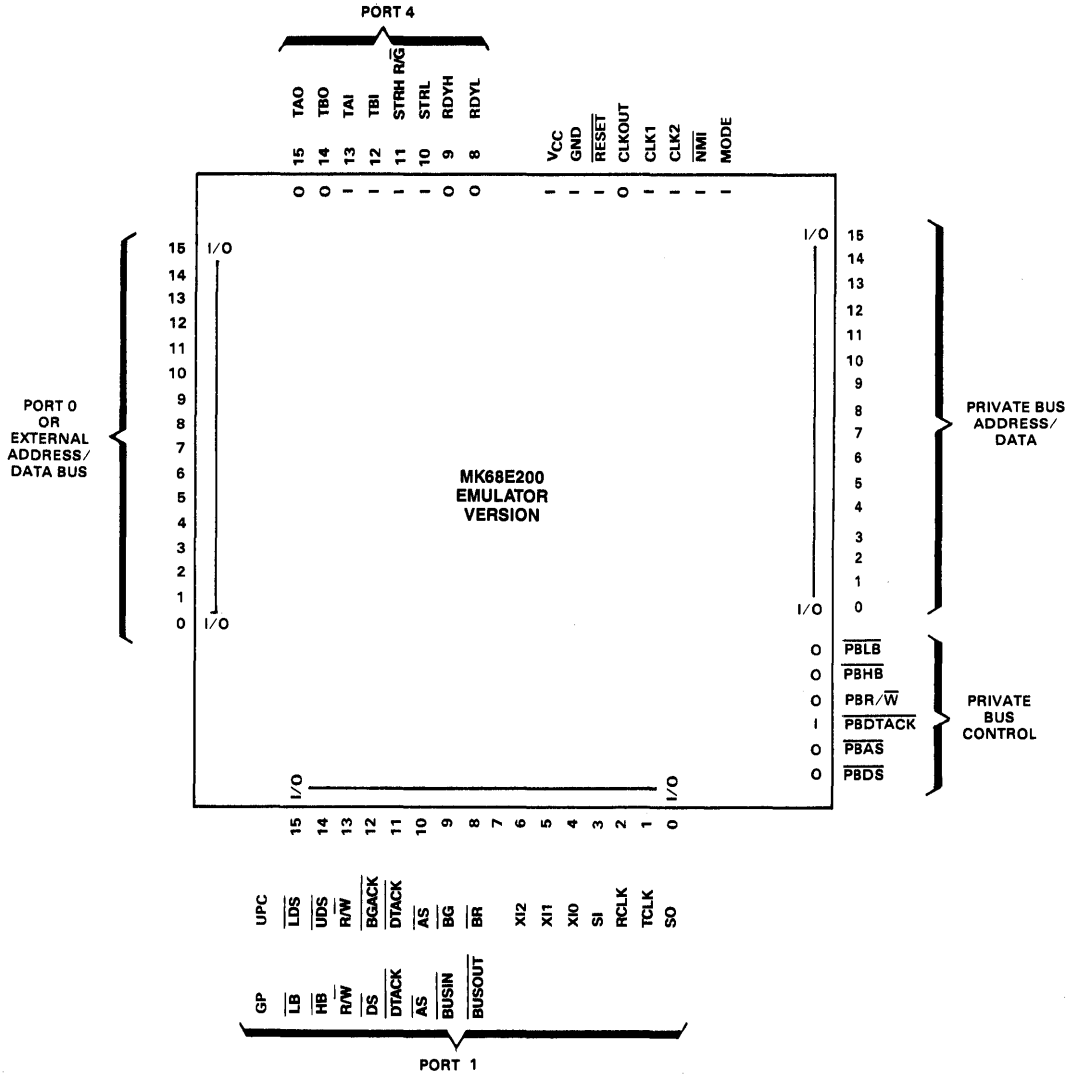
$\overline{BUSOUT}$
(Bus Output)
Output, active low. $\overline{BUSOUT}$ provides the opposite function of $\overline{BUSIN}$. When $\overline{BUSIN}$ is a bus request signal, $\overline{BUSOUT}$ is the corresponding bus grant, and vice versa.

EMULATOR VERSION

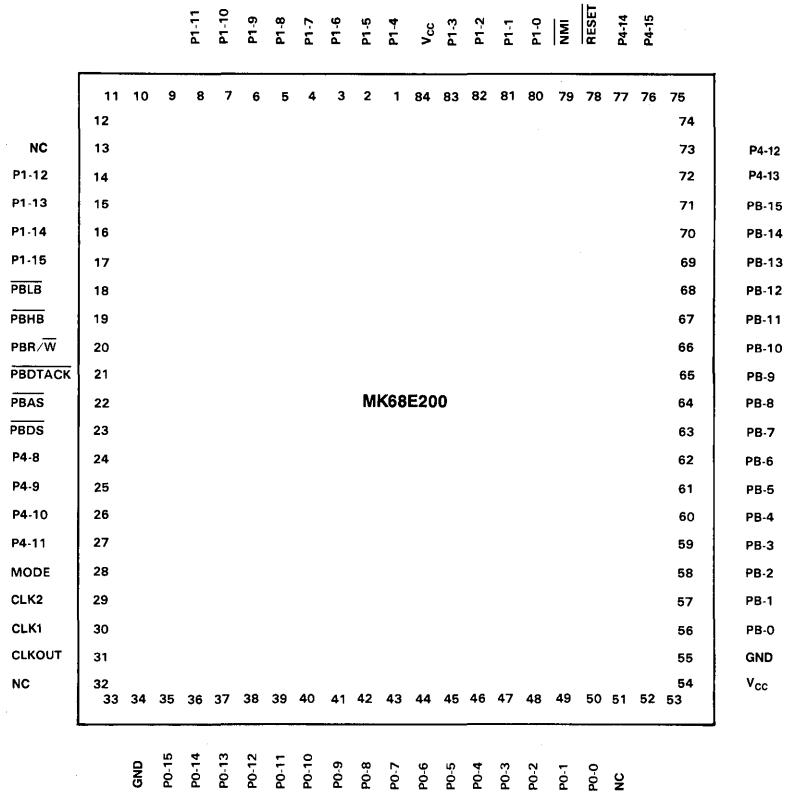
The emulator versions of the MK68200 are available in 84-pin, leadless chip carrier packages. Figure 18 illustrates the logical pinout of the emulator version. Table 1 summarizes the emulator parts described in this data sheet. The emulator versions have no on-chip ROM, but instead they include a second complete bus, referred to as the private bus. The private bus includes a multiplexed address/data bus as well as bus control signals. There are 22 pins associated with the private bus. All of the 40 I/O port pins that exist on the 48-pin versions are available to the user for configuration either as general purpose or special I/O pins, or as expanded bus pins.

MK68E200 LOGICAL PINOUT

Figure 18



MK68E200 PIN ASSIGNMENT (84-PIN LCC)
EMULATOR VERSION
Figure 19



PRIVATE BUS OPERATION

The address/data lines and control signals that constitute the private bus are functionally equivalent to the internal signals used to access internal resources on the 48-pin versions of the MK68200. Thus, the private bus may be used to interface EPROM memory in emulating mask ROM versions of the MK68200. Alternately, any combination of ROM, RAM, and I/O may reside on the private bus.

The address that is generated on the private bus is identical to that which is internally generated for 48-pin versions. When the part is used in a configuration that supports system bus addressing through the DMA window, any references in this region of the memory map produce an address on the private bus identical to that specified by the programmer. In other words, the segment bits have no effect on the private bus address. Write data appears on the private bus pins for all write operations, regardless of whether the reference is on-chip or off-chip. The MK68200 emulator version reads data from the private bus, unless data is read from on-chip RAM or I/O or from the external bus formed by the Port 0 and Port 1 I/O pins.

The I/O port range of the memory map ($FC00-$FFFF) is actually subdivided into space which is exclusively reserved for on-chip I/O ($FC00-$FDFF) and space which is exclusively reserved for in-circuit-emulator, or AIM, use ($FE00-$FFFF). The user should ensure that no external devices reside in the in-circuit-emulator area.

The private bus interface is the same as that for the GP expanded bus. All read/write transfers made exclusively on the private bus are three clock periods, regardless of the state of the Fast/Standard (F/S) bus timing selection bit. The user should ignore all activity on the private bus while accesses are in progress on the expanded bus. Care should also be taken that no external devices reside on the private bus in the memory space intended for expanded bus accesses. Note that there are three pins shown on the pin diagram of Figure 19 which are labeled "NC" and are not to be connected. They are reserved for use in future versions of the emulator device.

CRYSTAL SELECTION

The wide frequency range of crystals that can be chosen for the MK68200 offers the user a large degree of flexibility. To aid in the selection of a suitable crystal, the suggestions shown in Figure 20 should be considered by the user. The MK68200 offers an output pin that will provide a system clock signal at one-half of the crystal frequency.

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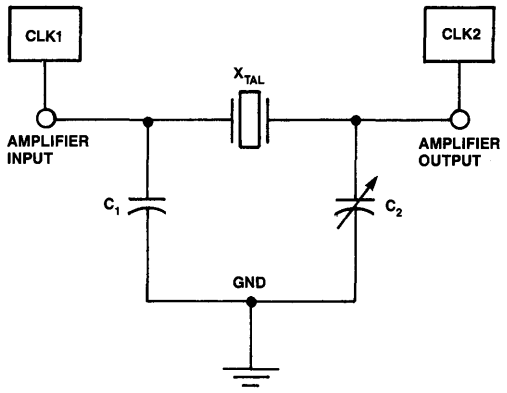
CRYSTAL CONNECTION
Figure 20



C_1 = 10 pf typical
C_2 = 20 pf typical

If it is desirable to "tune" the oscillator to a precise frequency, C_2 may be a variable capacitor.

C_2 should be in the range of $C_1 \leq C_2 \leq 2\ C_1$.

For a high frequency operation
$C_1 \approx 5 - 10$ pf.

SUMMARY OF CRYSTAL SPECIFICATIONS

Figure 21

FREQUENCY RANGE	SPECIFICATION
1 MHz - 12.0 MHz	PARALLEL RESONANCE FUNDAMENTAL MODE C_L = 20 pf to 40 pf AT CUT

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −.3 V to +7 V
Power Dissipation . . . . . 1.5 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MK68200 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_a = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input low voltage; all inputs	−0.3	0.8	V	
V_{IH}	Input high voltage; all inputs	2.0	V_{CC}	V	
V_{OL}	Output low voltage; all outputs		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output high voltage; all outputs	2.4		V	I_{OH} = −250μA
I_{CC}	Input power supply current		200	mA	
I_{LI}	Input leakage current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Tri-state output leakage current in float		±10	μA	V_{OUT} = 0.4 V to V_{CC}

CAPACITANCE

TA = 25°C, f = 12 MHz with unmeasured pins returned to ground.

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance	10	pf	Unmeasured pins returned to ground
C_{OUT}	Tri-state Output Capacitance	10	pf	

MK68200 AC ELECTRICAL SPECIFICATIONS

NO.	DESCRIPTION	4 MHz		6MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
1	$\overline{\text{RESET}}$ low time	20		20		state times	1
2	CLK 1 width high (external clock input)	45		30		ns	
3	CLK 1 width low (external clock input)	45		30		ns	
4	CLK 1 period (external clock input)	125	1000	83	1000	ns	
5	Crystal input frequency	1.000	8.000	1.000	12.000	MHz	
6	Clock Period (PHI 1)	250		167		ns	
7	PHI 1 low to PHI 1 high	125		83		ns	
8	PHI 1 high to PHI 1 low	125		83		ns	
9	PHI 1 low to CLKOUT low		40		27	ns	
10	PHI 1 high to CLKOUT high		40		27	ns	

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MK68200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (UPC, GP, AND PRIVATE BUSES)

NO.	DESCRIPTION	4MHz		6MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
11	PHI 1 low to R/$\overline{\text{W}}$, $\overline{\text{HB}}$, or $\overline{\text{LB}}$ valid		115		76	ns	2
12	PHI 1 high to $\overline{\text{AS}}$ low		115		76	ns	2
13	PHI 1 low to address valid		115		76	ns	2
14	$\overline{\text{AS}}$ low to address invalid	70		50		ns	2
15	PHI 1 low to tristate address		90		60	ns	2
16	Tristate address to $\overline{\text{DS}}$, $\overline{\text{LDS}}$, or $\overline{\text{UDS}}$ starting low (fast cycle)	10		10		ns	2
17	PHI 1 low to $\overline{\text{DS}}$, $\overline{\text{LDS}}$, or $\overline{\text{UDS}}$ low (fast cycle)		165		110	ns	2
18	PHI 1 low to data out valid during write		115		76	ns	2
19	PHI 1 low to R/$\overline{\text{W}}$, $\overline{\text{HB}}$, $\overline{\text{LB}}$ invalid	0		0		ns	2
20	PHI 1 low to address/data bus driven	0		0		ns	2
21	$\overline{\text{AS}}$ low to $\overline{\text{DS}}$, $\overline{\text{LDS}}$, or $\overline{\text{UDS}}$ starting low (fast cycle)	100	225	70	150	ns	2

MK68200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (UPC AND GP BUSES)

NO.	DESCRIPTION	4 MHz		6MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
22	Tristate address to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ starting low (standard cycle)	135		90		ns	
23	PHI 1 high to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ low (standard cycle)		165		110	ns	2
24	Valid Data Setup to PHI 1 low	10		5		ns	2
25	$\overline{AS}$ low to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ starting low (standard cycle)	225	350	150	230	ns	2
26	R/$\overline{W}$, $\overline{HB}$, or $\overline{LB}$ valid to $\overline{AS}$ starting low	60		60		ns	
27	Address valid to $\overline{AS}$ starting low	60		60		ns	
28	Input data hold time from PHI 1 low	45		30		ns	
29	Input data hold time from $\overline{DS}$, $\overline{LDS}$ or $\overline{UDS}$ high	0		0		ns	
30	PHI 1 low to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ high		180		120	ns	
31	$\overline{DTACK}$ low setup to PHI 1 high	15		10		ns	
32	$\overline{LDS}$, $\overline{UDS}$, or $\overline{DS}$ high to $\overline{DTACK}$ high (hold time)	−30		−30		ns	
33	$\overline{LDS}$, $\overline{UDS}$, or $\overline{DS}$ pulse width	240		150		ns	
34	PHI 1 high to $\overline{AS}$ high		90		60	ns	
35	PHI 1 low to data out invalid	0		0		ns	
36	$\overline{AS}$ inactive	235		150		ns	
37	$\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ high to data out invalid	180		110		ns	
38	$\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ high to $\overline{AS}$ high	5		5		ns	

MK68200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (UPC BUS)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
39	$\overline{BGACK}$ low to $\overline{BR}$ high	100	450	100	300	ns	
40	$\overline{BG}$ low to $\overline{BGACK}$ low	50	600	50	400	ns	
41	$\overline{BGACK}$, $\overline{AS}$, $\overline{DTACK}$, inactive to $\overline{BGACK}$ low; $\overline{BG}$ already low	0	600	0	400	ns	
42	$\overline{BGACK}$ low to $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, or address/data bus driven	40	135	40	90	ns	
43	$\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ or address/data bus tristate to $\overline{BGACK}$ high	0	180	0	120	ns	

MK68211 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (GP BUS)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
44	Tristate $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$ to $\overline{BUSOUT}$ low (bus grantor, fast cycle, no wait states)	175		100		ns	
45	$\overline{BUSIN}$ low to $\overline{BUSOUT}$ low (bus grantor, fast cycle, no wait states)		1900		1200	ns	
46	$\overline{BUSOUT}$ high to $\overline{AS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$ driven (bus grantor)	15		15		ns	
47	$\overline{BUSIN}$ high to $\overline{BUSOUT}$ high (bus grantor)	520	900	300	600	ns	
48	Tristate address/data bus to $\overline{BUSOUT}$ low (bus grantor)	70		70		ns	
49	$\overline{BUSOUT}$ high to address/data bus driven (bus grantor)	50		50		ns	
50	$\overline{BUSOUT}$ low to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$ driven (bus requestor, $\overline{BUSIN}$ low)	240		150		ns	
51	$\overline{BUSIN}$ low to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$,$\overline{LB}$, $\overline{HB}$ driven (bus requestor, $\overline{BUSOUT}$ low)	270	650	180	500	ns	
52	Tristate $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$, to $\overline{BUSOUT}$ high (bus requestor)	180		100		ns	
53	$\overline{BUSOUT}$ high to $\overline{BUSIN}$ high (bus requestor)		530		400	ns	
54	$\overline{BUSIN}$ low to address/data bus driven (bus requestor)	350		250		ns	
55	Tristate address/data bus to $\overline{BUSOUT}$ high (bus requestor)	100		65		ns	

MK68E200 BUS AC ELECTRICAL SPECIFICATIONS (PRIVATE BUS)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
56	Valid Data Setup to PHI 1 low	30		20		ns	
57	PBR/$\overline{W}$ valid to $\overline{PBAS}$ starting low	40		40		ns	
58	Address valid to $\overline{PBAS}$ starting low	35		35		ns	
59	Input data hold time from PHI 1 low	0		0		ns	
60	Input data hold time from $\overline{PBDS}$ high	−25		−25		ns	

MK68E200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (PRIVATE BUS) (Cont.)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
61	PHI 1 low to $\overline{\text{PBDS}}$ high		130		105	ns	
62	$\overline{\text{PBDTACK}}$ low setup to PHI 1 high	20		15		ns	
63	$\overline{\text{PBDS}}$ high to $\overline{\text{PBDTACK}}$ high (hold time)	−15		−15		ns	
64	$\overline{\text{PBDS}}$ pulse width	190		125		ns	
65	PHI 1 high to $\overline{\text{PBAS}}$ high		100		75	ns	
66	PHI 1 low to data out invalid	10		10		ns	
67	$\overline{\text{PBAS}}$ inactive	200		135		ns	
68	$\overline{\text{PBDS}}$ high to data out invalid	200		135		ns	
69	$\overline{\text{PBDS}}$ high to $\overline{\text{PBAS}}$ high	15		15		ns	

MK68200 INPUT/OUTPUT AC ELECTRICAL CHARACTERISTICS

NO.	DESCRIPTION		4 MHz		6 MHz		UNITS	NOTES
			MIN	MAX	MIN	MAX		
70	Active and inactive pulse times	For XI2, XI1, STRH, STRL, TAI, TBI, $\overline{\text{NMI}}$	5		5		state times	1
		For XI0	3		3			
71	Input data setup to falling edge of STRH, STRL		50		35		ns	
72	Input data hold from the falling edge of STRH, STRL		60		40		ns	
73	RDYH, RDYL low time		1	3	1	3	state times	1
74	Delay from STRH, STRL high to RDYH, RDYL low			110		75	ns	
75	Delay from data valid to RDYH, RDYL high during output			3		3	state times	1
76	Delay from STRH high to data out			125		85	ns	
77	Port 0 data hold time from STRH low		15		10		ns	
78	Delay to Port 0 float from STRH low			75		50	ns	
79	TCLK,RCLK period (asynchronous) TCLK,RCLK period (synchronous)		4.0 1.0	DC DC	2.67 .667	DC DC	μs	
80	TCLK, RCLK width low		4	DC	4	DC	state times	1
81	TCLK, RCLK width high		4	DC	4	DC	state times	1

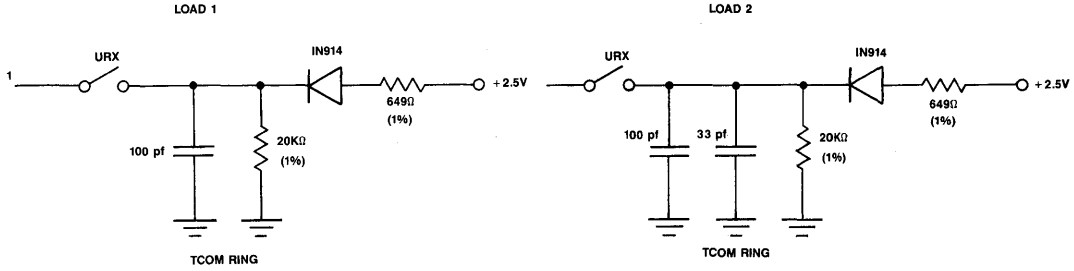
MK68200 INPUT/OUTPUT AC ELECTRICAL SPECIFICATIONS

NO.	DESCRIPTION		4 MHz		6 MHz		UNITS	NOTES
			MIN	MAX	MIN	MAX		
82	TCLK low to SO delay (sync mode)	TCLK as input	330		220		ns	
		TCLK as output	75		50			
83	SI to RCLK high setup time (sync mode)	RCLK as input	30		20		ns	
		RCLK as output	180		120			
84	SI hold time from RCLK high (sync mode)	RCLK as input	45		30		ns	
		RCLK as output	0		0			

NOTES
1. One state time is equal to one-half of the instruction clock (PHI 1) period.
2. For the private bus case, the signals referenced apply to the equivalent private bus signals.

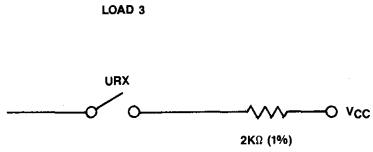
VI

OUTPUT TEST LOAD
Figure 22



TEST LOAD 1 IS APPLICABLE TO ALL PINS EXCEPT THOSE LISTED UNDER TEST LOAD 2 AND TEST LOAD 3.

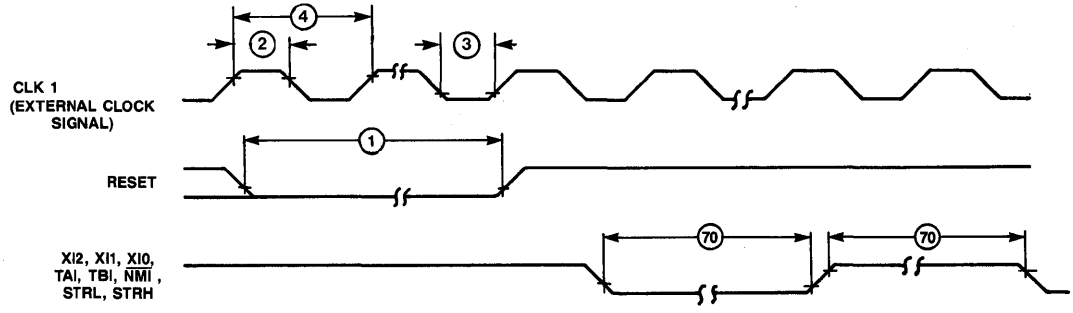
TEST LOAD 2 IS APPLICABLE TO THE FOLLOWING PINS: CLKOUT, $\overline{PBLB}$, $\overline{PBHB}$, PBR/$\overline{W}$, $\overline{PBDS}$, P4-15, P4-14, P4-9, P4-8, AND $\overline{PBAS}$.



TEST LOAD 3 IS APPLICABLE TO THE FOLLOWING PINS: P1-12 AND P1-8.

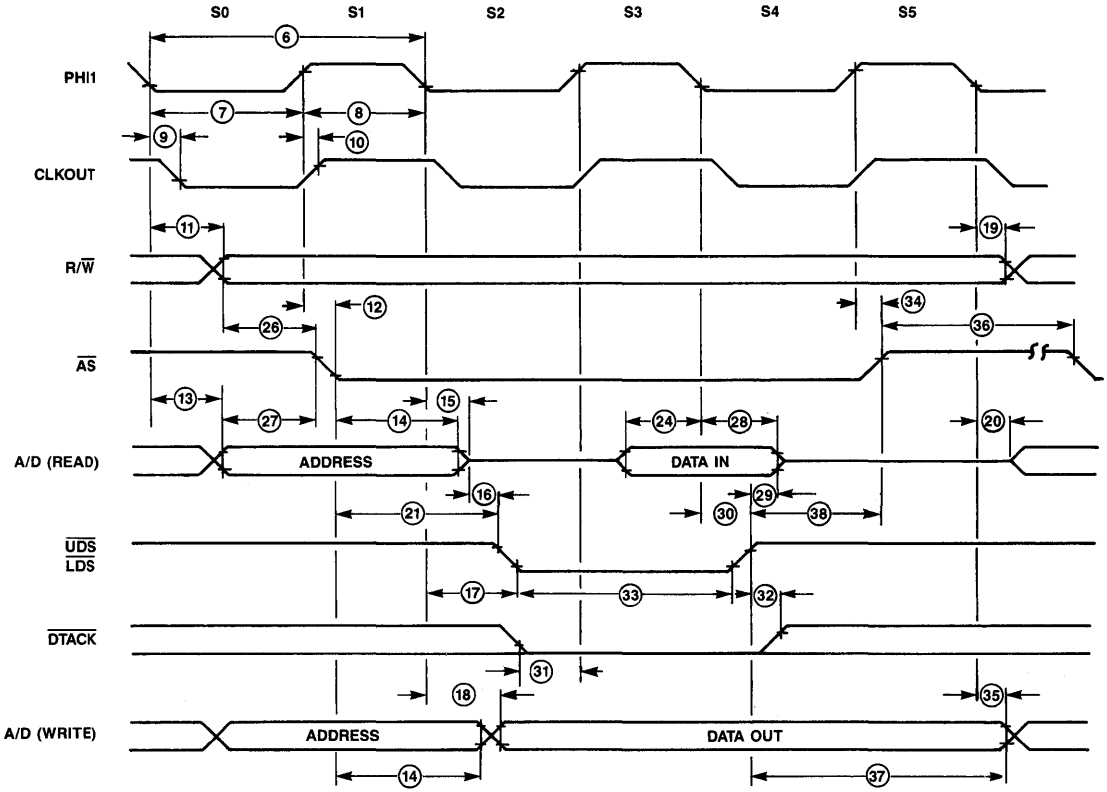
MK68200 AC TIMING

Figure 23



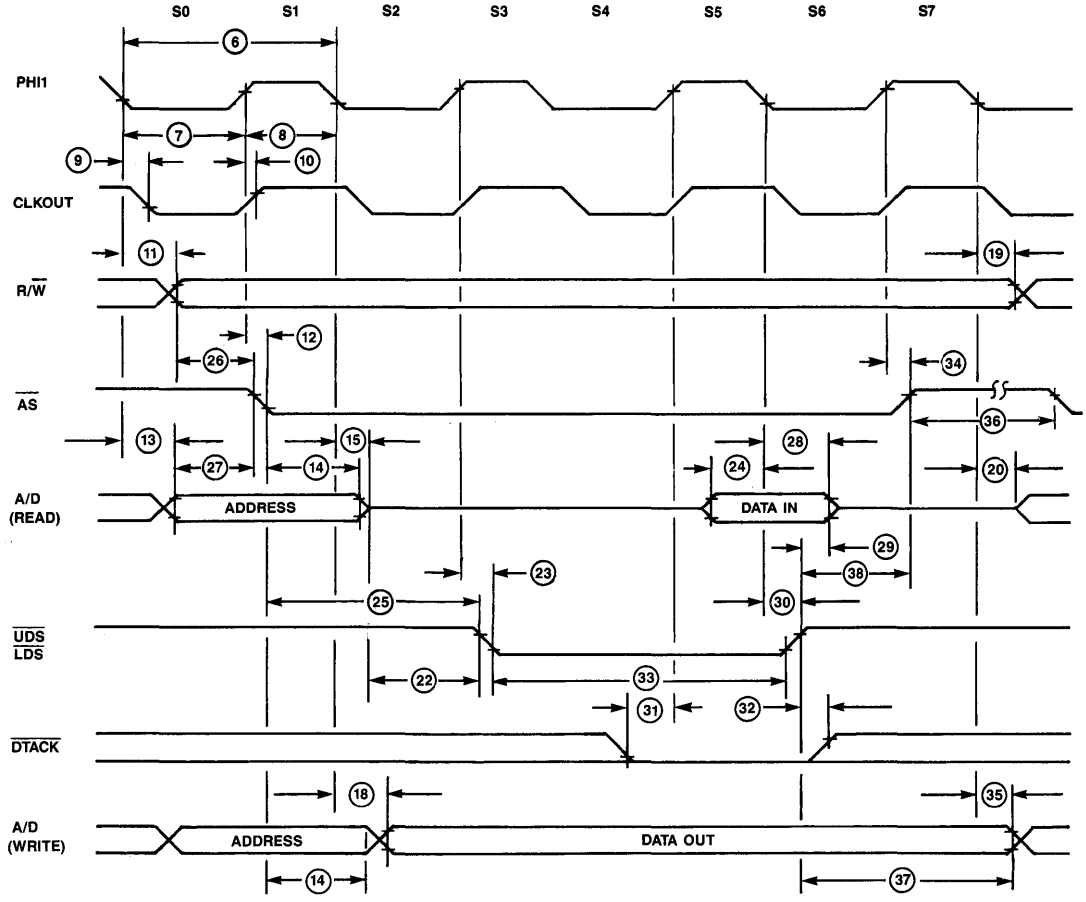
MK68201 UPC BUS TIMING (FAST CYCLE)

Figure 24



MK68201 UPC BUS TIMING (STANDARD CYCLE)

Figure 25



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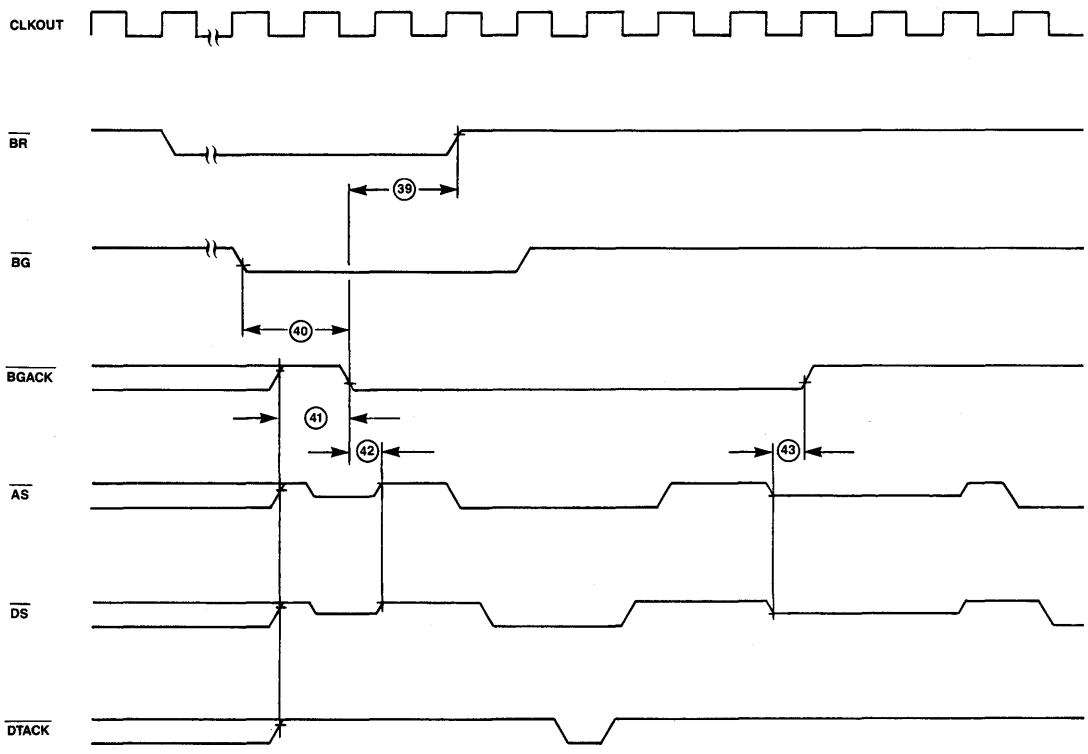
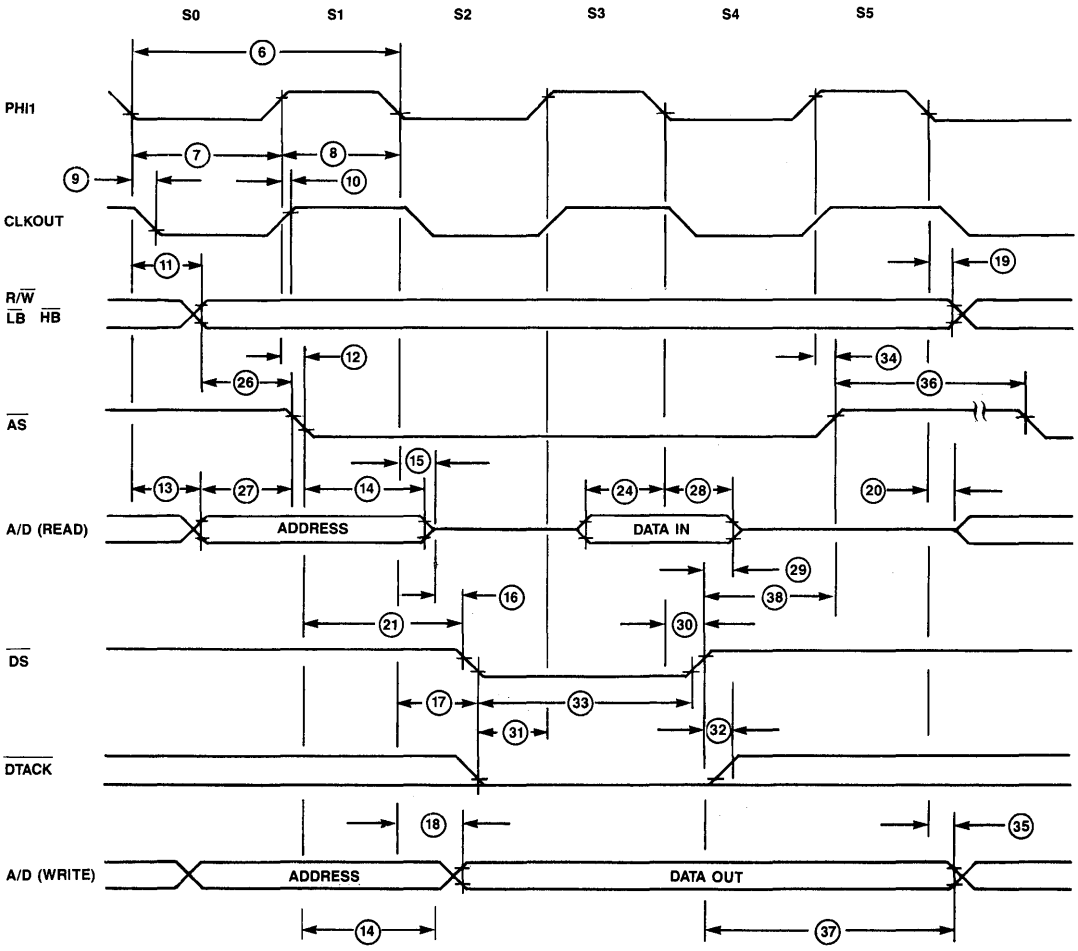
MK68201 UPC BUS ARBITRATION TIMING
Figure 26



MK68211 GP BUS TIMING (FAST CYCLE)
Figure 27



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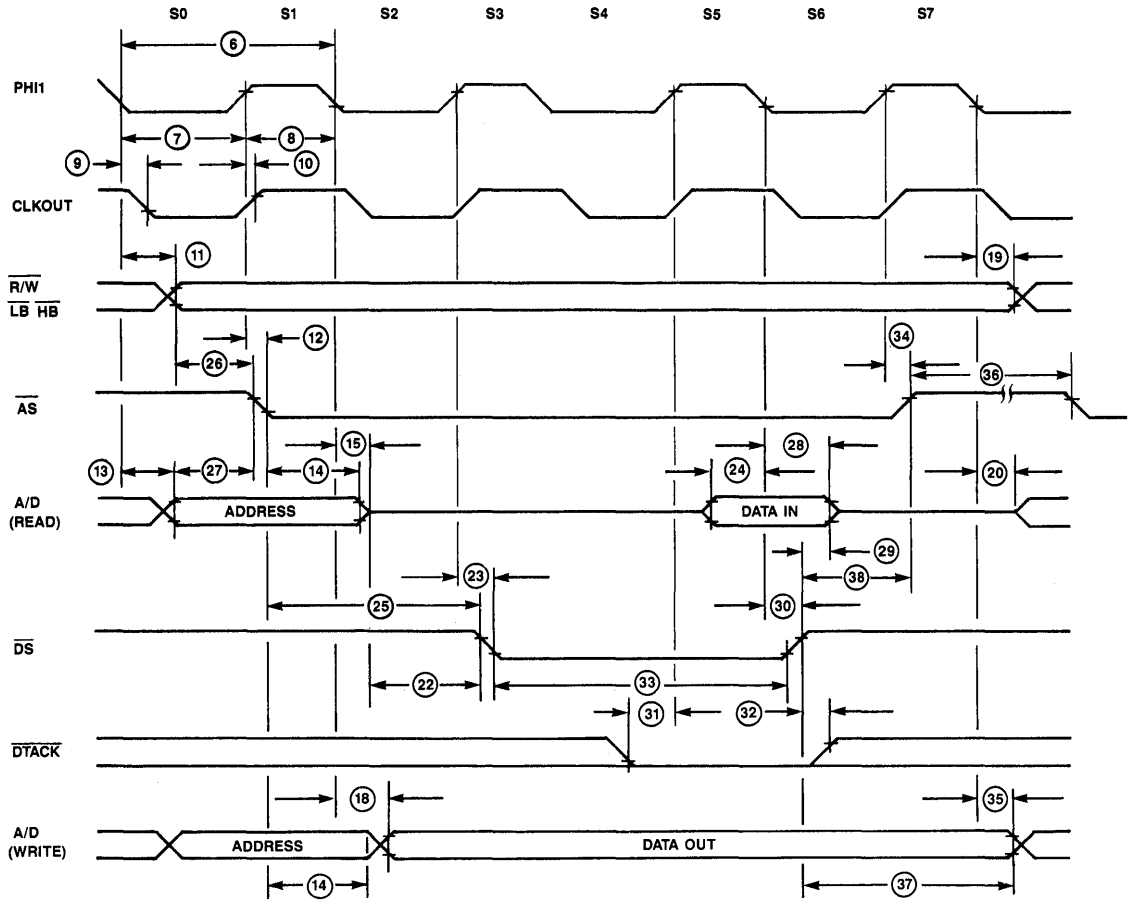
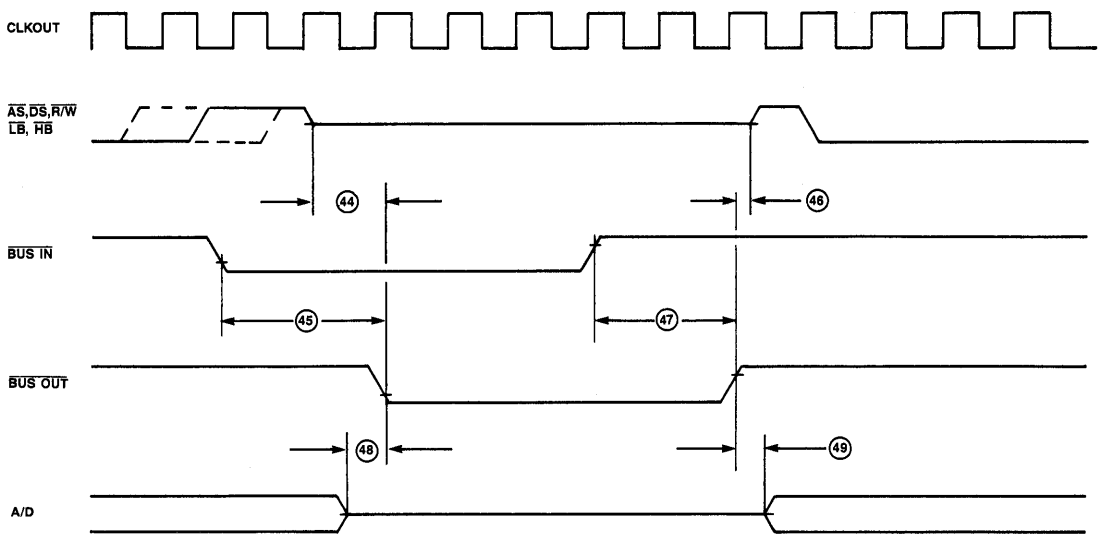
MK68211 GP BUS TIMING (STANDARD CYCLE)

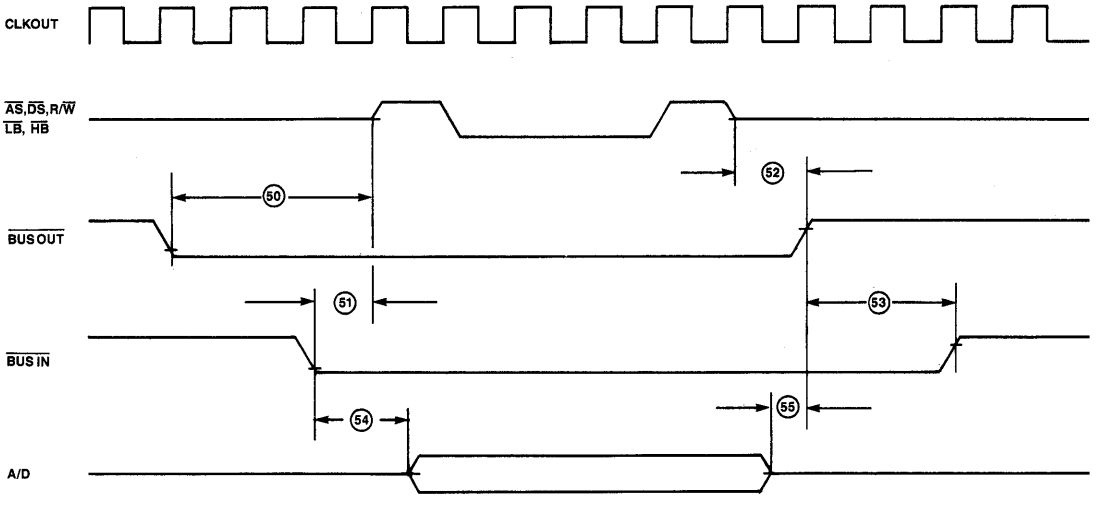
Figure 28



MK68211 GP BUS ARBITRATION TIMING (BUS GRANTOR)
Figure 29

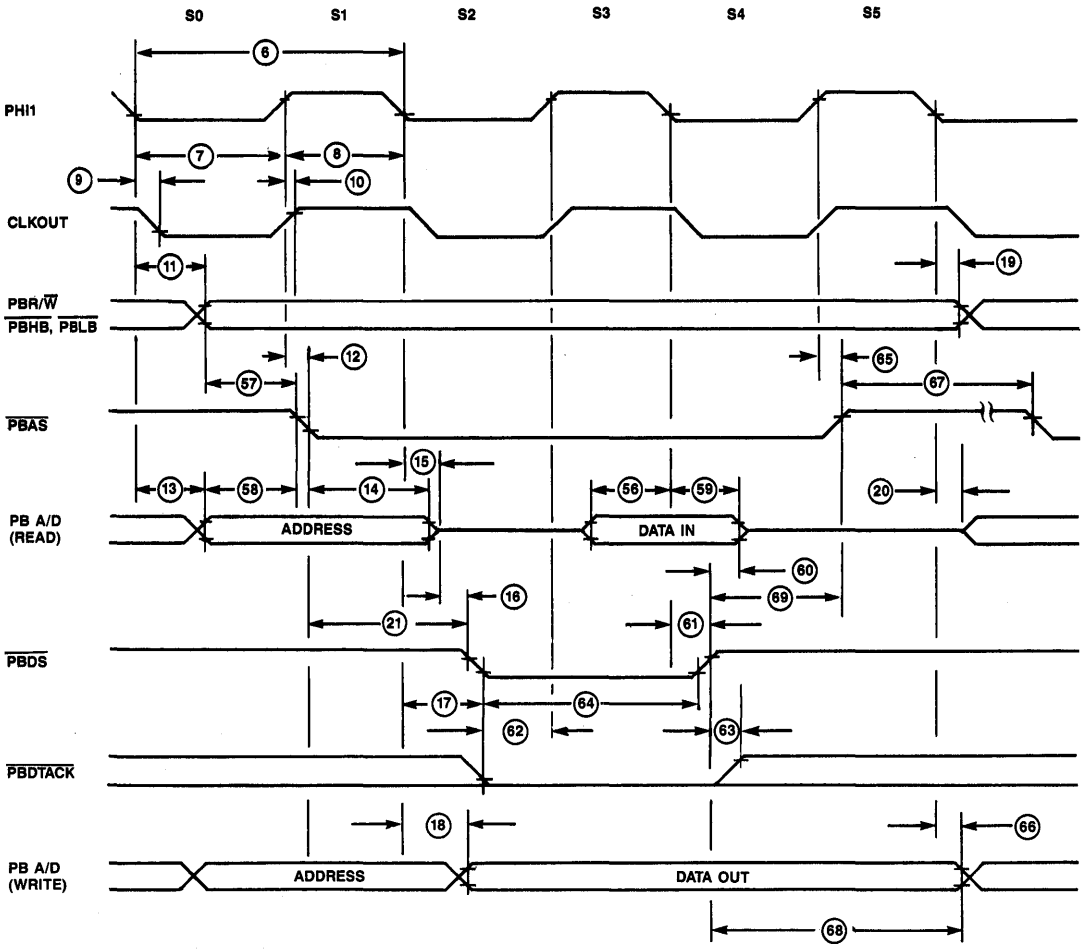


MK68211 GP BUS ARBITRATION TIMING (BUS REQUESTOR)
Figure 30

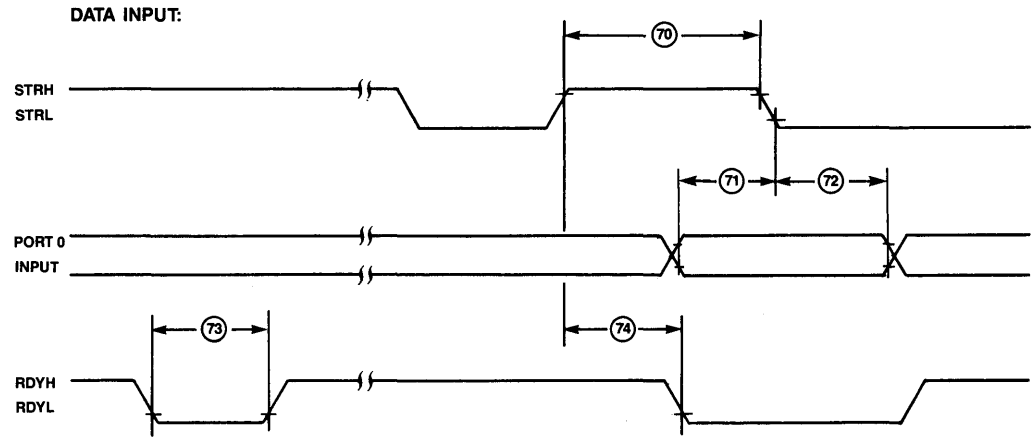


MK68200 PRIVATE BUS TIMING (FAST CYCLE)

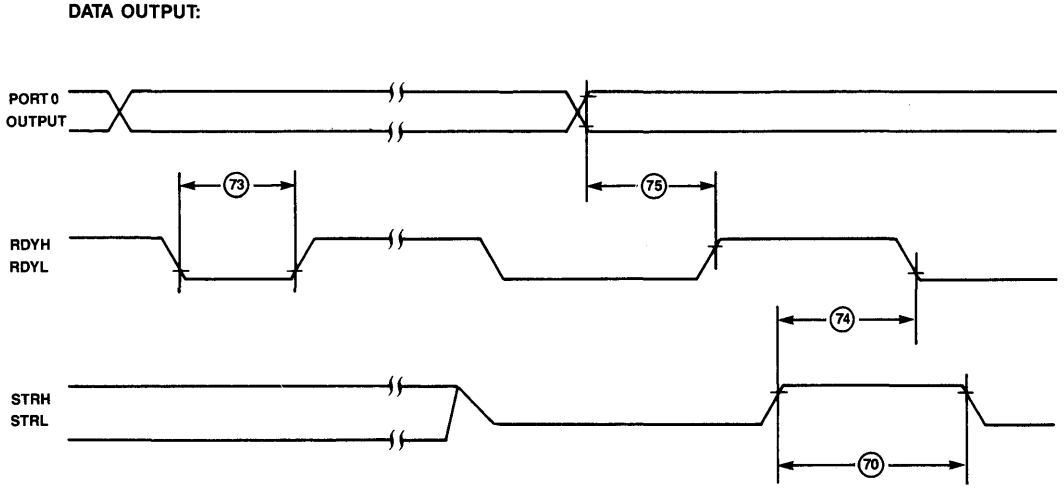
Figure 31



INPUT/OUTPUT AC TIMING
Figure 32

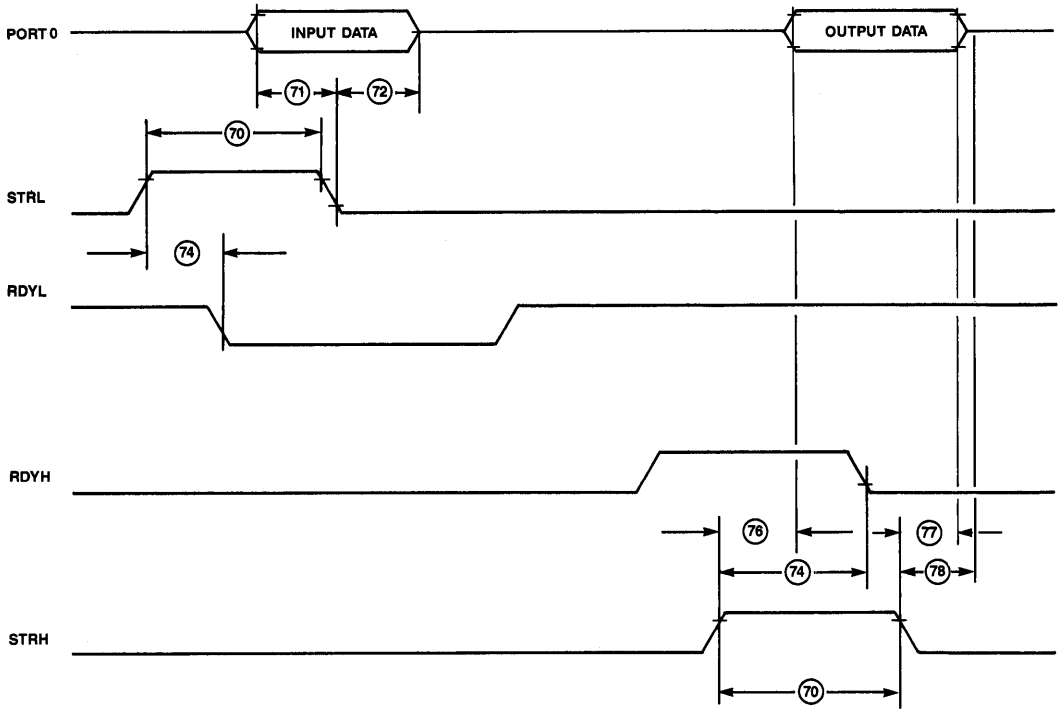


INPUT/OUTPUT AC TIMING
Figure 33

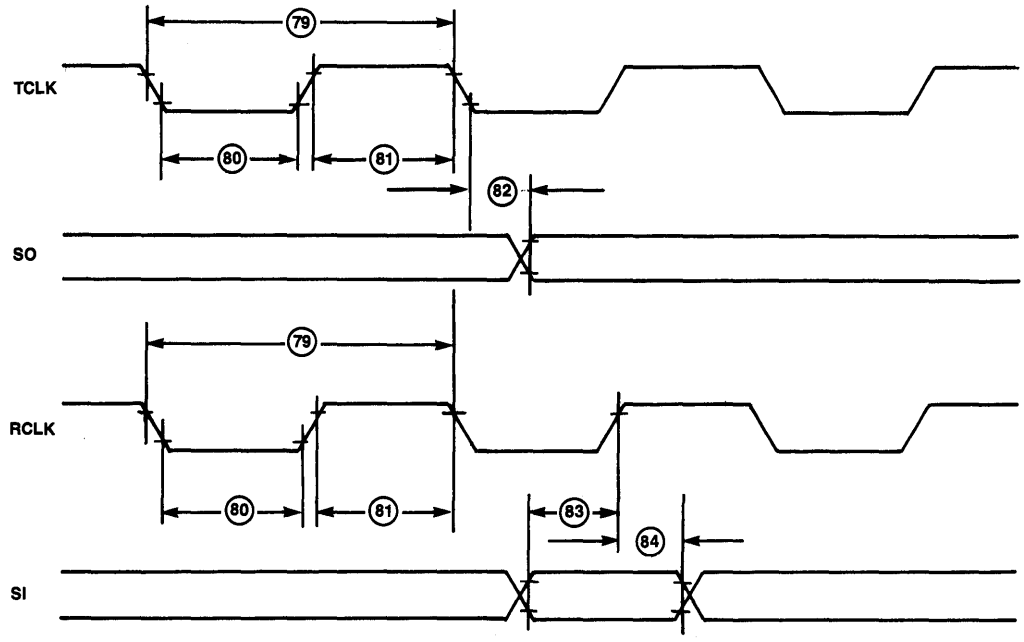


INPUT/OUTPUT AC TIMING
Figure 34

BIDIRECTIONAL I/O:



SERIAL I/O:

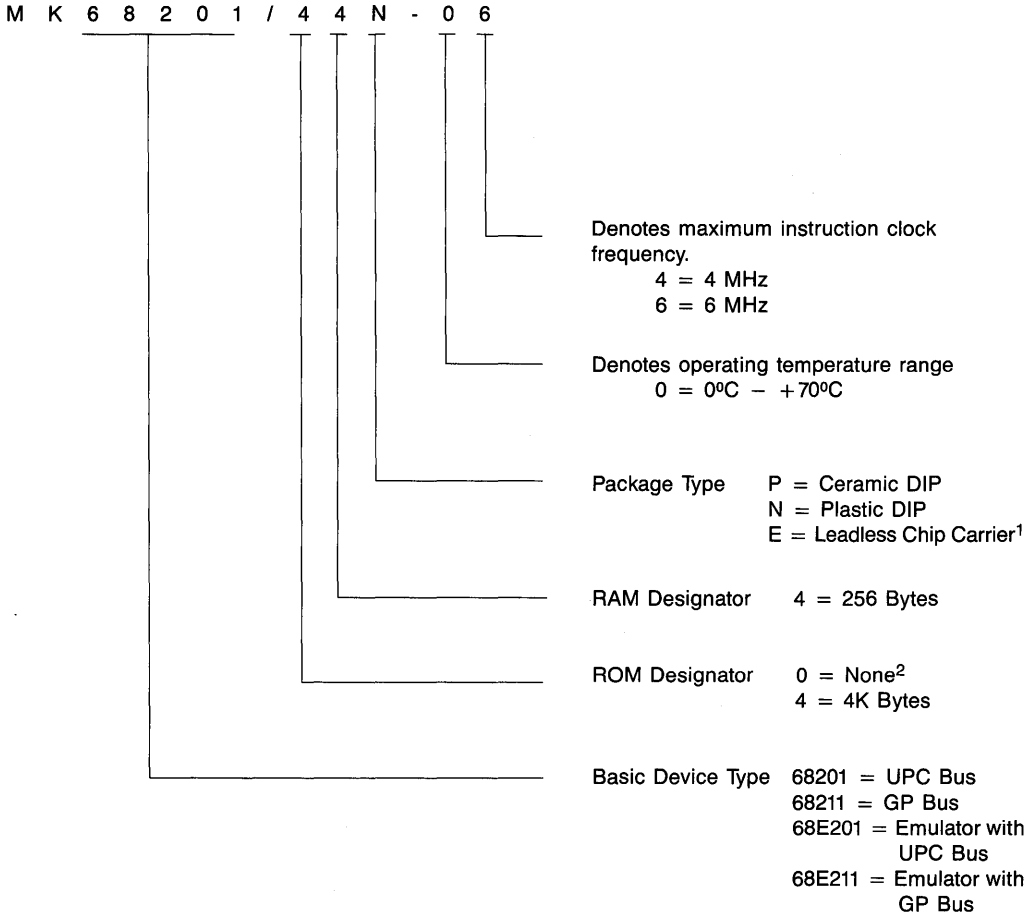


PART NUMBERING INFORMATION

There are two types of part numbers for the 68200 family of devices. The generic part number describes the basic device type, the amount of ROM and RAM, the desired package type, temperature range, power supply tolerance, and expandable bus interface type.

Generic Part Number

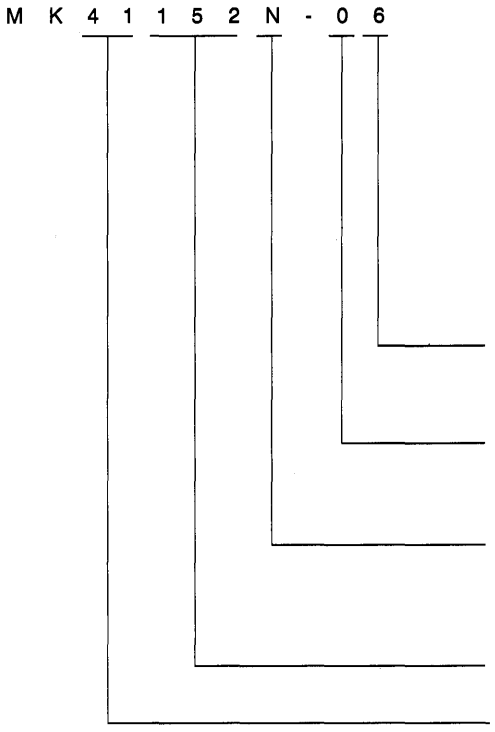
An example of the generic part number is shown below:



NOTES
1. Available for emulator only.
2. Must be "0" when specifying the emulator.

Device Order Number

An example of the device order number is shown below:



VI

NOTES
1. Available for emulator only.

ORDERING INFORMATION

The device selection table shown below lists available versions of the 68200.

GENERIC PART NO.	DEVICE ORDER NO.	PACKAGE TYPE	MAXIMUM CLOCK FREQUENCY	TEMPERATURE RANGE
MK68201/04-06	MK41000N-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68201/44-06	MK41XXXN-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68E201/04-06	MK40000E-06	Ceramic LCC	6 MHz	0° to 70°C
MK68211/04-06	MK42000N-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68211/44-06	MK42XXXN-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68E211/04-06	MK40010E-06	Ceramic LCC	6 MHz	0° to 70°C
MK68201/04-04	MK41000N-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68201/44-04	MK41XXXN-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68E201/04-04	MK40000E-04	Ceramic LCC	4 MHz	0° to 70°C
MK68211/04-04	MK42000N-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68211/44-04	MK42XXXN-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68E211/04-04	MK40010E-04	Ceramic LCC	4 MHz	0° to 70°C