PROGRAMMABLE COUNTERS USING THE MC10136 AND MC10137 MECL 10K UNIVERSAL COUNTERS

INTRODUCTION

Phase-locked loop and frequency synthesis applications often require programmable counters with high frequency capability. As the family of MECL 10K MSI functions has grown to include two new universal counters the MC10136 and MC 10137, programmable counters may now be designed with an operating frequency capability in excess of 100 megahertz. This performance is about 4 times that possible with standard 7400 Series TTL MSI in the same application.

The preset and count (up or down) features of these two synchronous counters are utilized to design counting systems with variable divide moduli. To exploit maximum frequency capabilities of the MC10136 and MC10137, pulse "gobbling"* techniques (see below) are also used in the system design.

COUNTER OPERATION

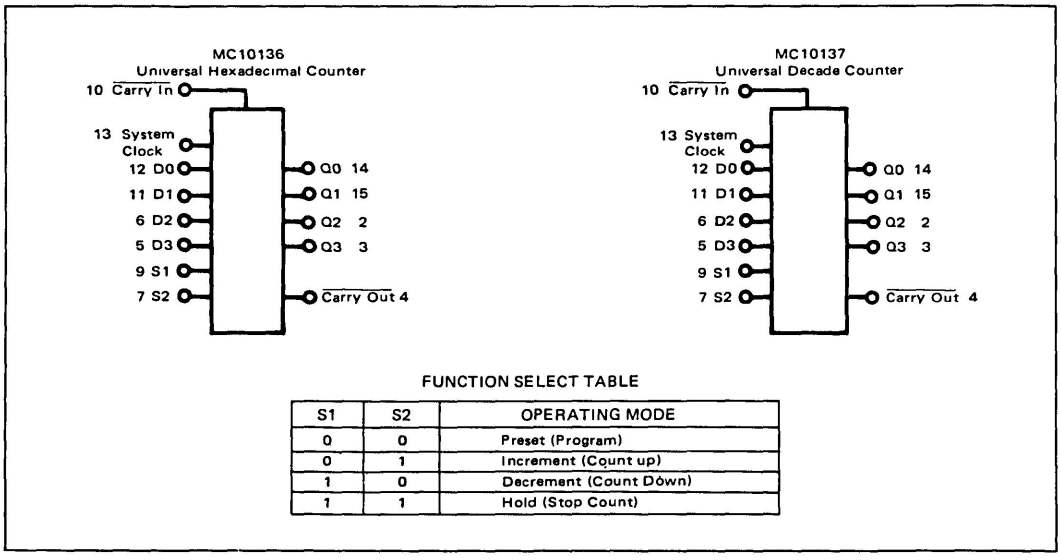
The MC10136 and MC10137 are both fully sunchronous counters. The MC10136 is a hexadecimal (0 thru 15 binary) counter, and the MC10137 is a BCD decade counter. Operation of both counters is similar; that is, three control lines (S1, S2, $\overline{C}_{in}$) determine the operational mode of the counter. Lines S1 and S2 control one of four operations: preset (program); increment (count up); decrement (count down); or hold (stop count). Figure 1 shows the logic configurations for each counter and the function select table applicable to both counters.

In the preset mode a clock pulse is necessary to load the counter. When the S1 and S2 select lines are both in the LOW state, the information present on the data inputs (D0, D1, D2, D3) will be entered into the counter on the positive transition of the clock.

The system clock is defined as positive going, and the counters change state only on the rising edge of the clock signal. Due to the master-slave construction of the flip-flops, any other data or control input may change at any time other than during the positive transition of the clock (observing proper set-up and hold times).

The $\overline{C}_{in}$ line overrides the clock when the counter is in either the increment mode or the decrement mode of operation. This input allows several devices to be cascaded into a fully synchronous multistage counter.

*Pulse "gobbling": A technique by which an external flip-flop is used to "hold" a pulse, thus acting as an auxiliary counter.



FUNCTION SELECT TABLE

S1	S2	OPERATING MODE
0	0	Preset (Program)
0	1	Increment (Count up)
1	0	Decrement (Count Down)
1	1	Hold (Stop Count)

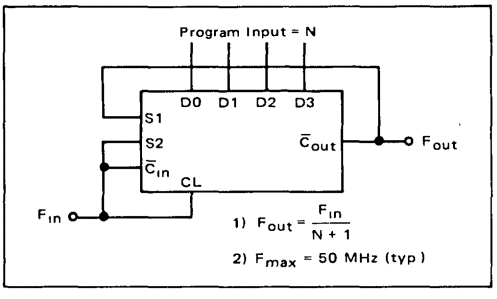
FIGURE 1 — MECL 10K Universal Counter Logic Diagrams and Function Select Table.

The $\overline{C}_{out}$ output goes LOW on the terminal state of the counter, whether in the increment mode or the decrement mode of operation. With both counters, the $\overline{C}_{out}$ output goes LOW on the zero state when operating in the count-down mode. The count-up mode causes the $\overline{C}_{out}$ to go LOW at the count of 15 for the MC10136, and at the count of 9 for the MC10137.

$\overline{C}_{out}$ is obtained by ORing $\overline{C}_{in}$ with the outputs of the counter. In this manner the carry is rippled through the counter for multistage applications.

PROGRAMMABLE COUNTERS USING NO EXTERNAL GATING

Both the MC10136 and MC10137 may be used in a programmable counter without external gating. Figure 2 illustrates a technique in which $\overline{C}_{out}$ is used to control the counter's operational mode.



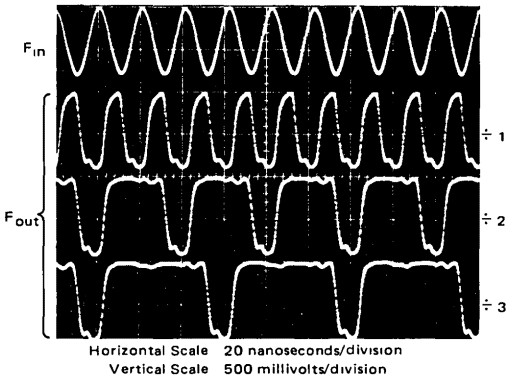


FIGURE 2 – Programmable Counter Using no External Gating. Divide Modulus M = N + 1.

The counter is normally in the decrement mode and counts down from the number N preset into the device. On reaching the "zero" state the $\overline{C}_{out}$ goes LOW and allows the next clock pulse to reload the number N into the counter. The divide modulus M then is equal to N+1.

The clock signal is tied common to the $\overline{C}_{in}$ and S2 control lines to prevent a latch-up state when reloading the counter. In the program mode $\overline{C}_{out}$ is forced LOW and $\overline{C}_{in}$ is disabled. $\overline{C}_{out}$, fed back to the S1 line, would latch up the counter unless the clock is tied to the other control lines.

As noted previously, the range in divide modulus will determine the choice between the MC10136 or the MC10137. For the MC10136, M may vary from 1 to 16; for the MC10137, M may vary from 1 to 10. Maximum toggle frequency in both cases is over 50 MHz, Figure 2 shows typical waveforms at 50 MHz.

If a larger divide modulus is required, two or more devices may be used in a larger counter – at a sacrifice in maximum operating frequency. Figure 3 shows a two-stage configuration with maximum frequency typically 35 MHz. The divide modulus is extended to 256 with the MC10136 and to 100 with the MC10137.

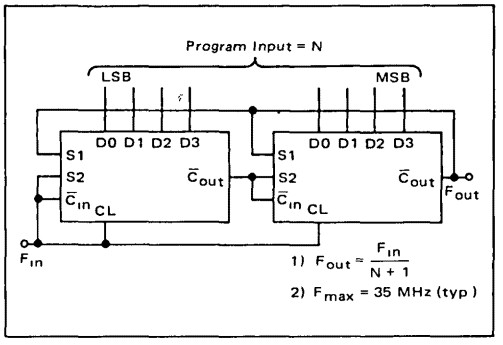


FIGURE 3 – Two-Stage Programmable Counter. Divide Modulus M is 256 Maximum with MC10136.

HIGHER FREQUENCY COUNTERS

Other techniques may be used to produce higher frequency programmable counters. External decoding and pulse "gobbling" allow higher performance at the cost of an increased package count.

One of the above improvements is used in the counter of Figure 4. A gate is used to externally decode the preset condition for the counter. This can decrease delay time by 2 to 3 nanoseconds. Using a MECL 10K gate, maximum operating frequency is typically 75 MHz.

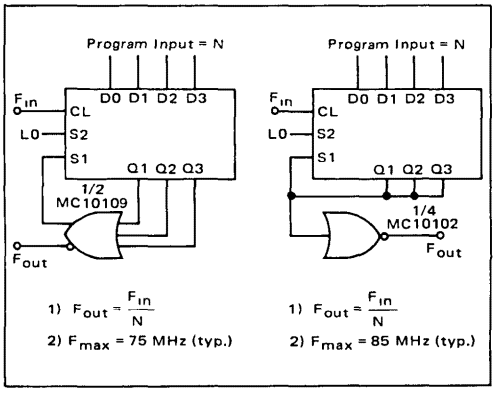
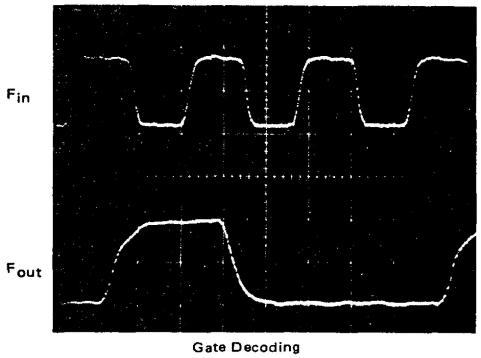


FIGURE 4 – Programmable Counter Using External Decoding. Either a Gate or a Wired-OR May be Used.

The divide modulus for this counter is equal to the program input N, (M = N). The preset condition is decoded one clock pulse before the zero state of the counter. In this manner the clock pulse necessary for preset is included in the programmed input number N. For the MC10136, M may vary from 2 to 15, and from 2 to 9 for the MC10137.

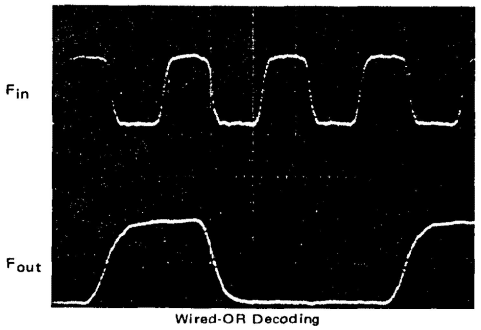
A wired-OR may be used in place of the OR gate. Maximum operating frequency can be extended to 85 MHz with this technqiue. A gate should still be used, however, to buffer the signal out (F_{out}).

In Figure 5, F_{out} and F_{in} waveshapes are shown for both circuit configurations. Notice that the frequency of the Wired-OR is displayed at 85 MHz, as opposed to the 75 MHz shown for the gate version. Both are dividing by a modulus of 3.



Gate Decoding

Horizontal Scale: 5 nanoseconds/division
Vertical Scale: 500 millivolts/division



Wired-OR Decoding

Horizontal Scale: 5 nanoseconds/division
Vertical Scale: 500 millivolts/division

FIGURE 5 – Waveforms for Programmable Counters Using External Decoding.

A second higher frequency technique incorporates pulse "gobbling" (Figure 6). In addition to externally decoding the preset condition, a flip-flop is used to "gobble" a pulse and provide an even shorter preset delay time than the external decoding version.

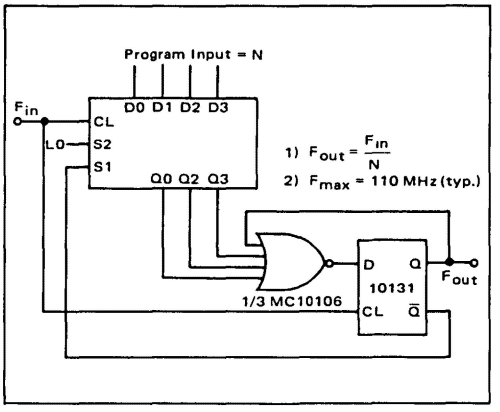


FIGURE 6 – Programmable Counter Using External Decoding and Pulse Gobbling. Divide Modulus M = N.

The pulse diagram in Figure 7 shows the sequence of signals for this counter. The S1 line is HIGH during the count phase of operation. On reaching the count of 2, the D input line to the flip-flop is forced HIGH. On the next clock pulse the HIGH state is clocked into the flip-flop, causing the S1 line and the D input line both to go LOW. The succeeding clock pulse presets the counter and loads a LOW back into the flip-flop, causing the S1 line to return to a HIGH state. The counter is then ready to proceed in the decrement count mode. In the diagram the number 8 was loaded into the counter.

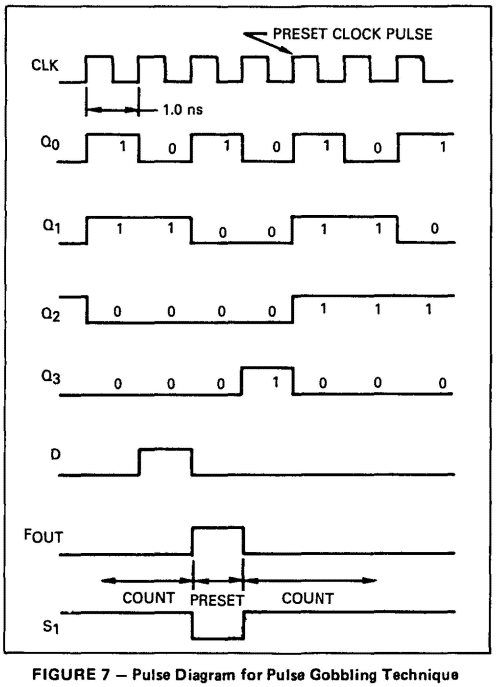
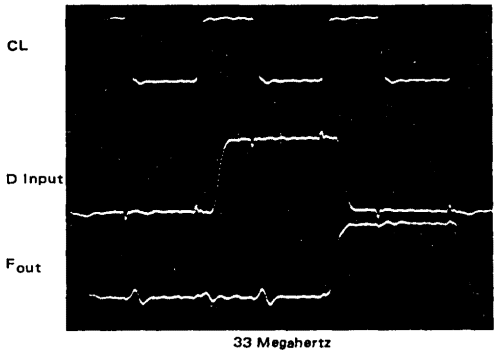


FIGURE 7 – Pulse Diagram for Pulse Gobbling Technique

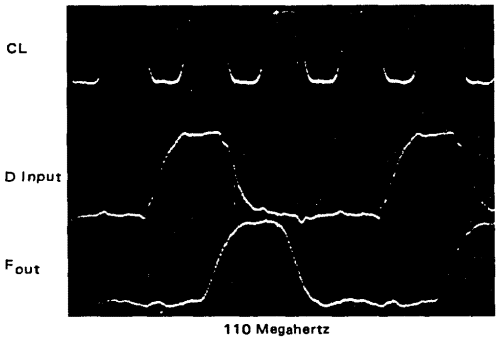
The advantage of this technique is that the decode delay and set-up time for presetting the counter do not have to occur within one clock period. These two times occur within separate clock periods. Again this allows a higher frequency of operation. Maximum frequency is typically about 110 MHz.

Examples of some of the actual waveforms idealized in the pulse diagram are presented in Figure 8. The F_{in} (or CL), the D input to the flip-flop, and F_{out} are shown. The sequence is as discussed in the previous paragraphs, although the divide modulus is 3. Two frequencies – 33 MHz and 110 MHz – are shown.

The divide modulus M is similar to the preceding design, that is, M equals the program input N. For larger moduli counters, two counters may be cascaded using the pulse gobbling technique (Figure 9). The divide modulus may be extended to 255 with two MC10136's. The maximum frequency is about 80 MHz for such a configuration.



33 Megahertz
Horizontal Scale: 10 nanoseconds division
Vertical Scale. 500 millivolts division



110 Megahertz
Horizontal Scale: 5 nanoseconds/division
Vertical Scale· 500 millivolts/division

FIGURE 8 – Waveforms for Programmable Counter Using Pulse Gobbling

CONCLUSION

In the preceding designs, either universal counter may be used. The choice of either the MC10136 or the MC-10137 will normally be based upon the range in divide modulus desired. In all cases the program input N is binary coded (hexadecimal or BCD). The number preset or loaded into the counter is the initial state from which decrement starts.

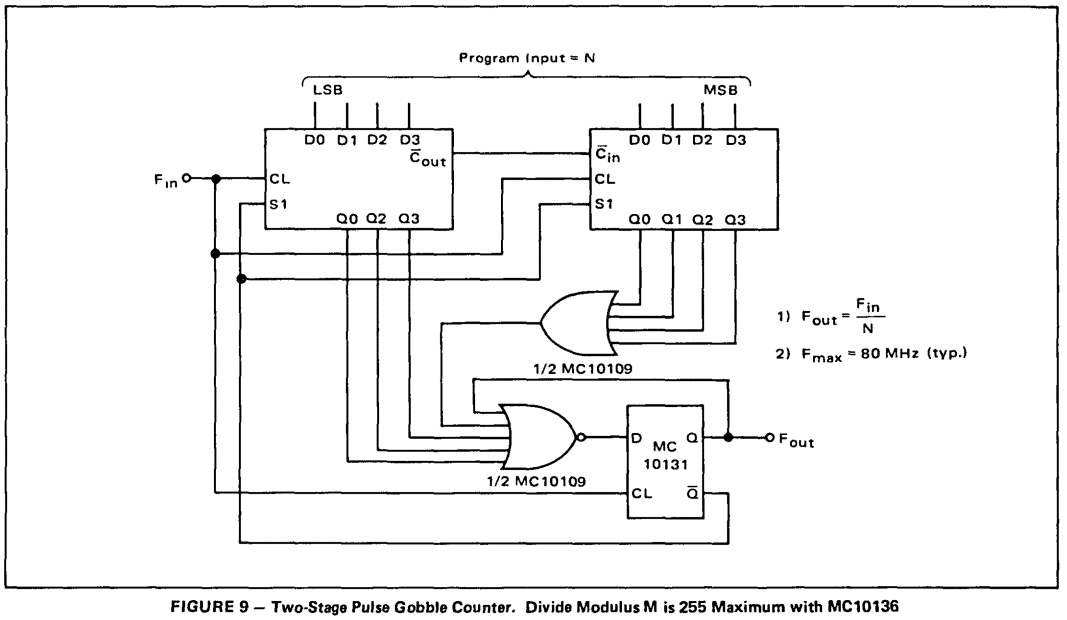


FIGURE 9 – Two-Stage Pulse Gobble Counter. Divide Modulus M is 255 Maximum with MC10136