APPLICATION NOTES

THE MECL LINE OF DIGITAL INTEGRATED CIRCUITS

INTRODUCTION

The MECL family of monolithic integrated circuits consists of a wide selection of emitter coupled current mode logic circuits. Since MECL employs transistors in the non-saturating mode, it is inherently the fastest type of logic available. MECL is produced in two temperature ranges: the MC300 Series (-55°C to +125°C) and the MC350 Series (0°C to +75°C). Supply voltage is nominally -5.2 V ± 10% which yields a power dissipation between 35 and 40 mW per gate. Delay times range from 5 ns to 10 ns. The noise margin for all possible noise inputs is 200 mV or better over the full temperature range for at least 90% of the devices tested at a fan-out of one. Noise margin at room temperature is typically 300 mV.

The MECL gate employs a differential amplifier input, resulting in high input impedance, and good rejection of power supply variations. The very low output impedance of the emitter followers results in high fan-out and fast rise time for capacitive loads. Resistors and logic levels are chosen to prevent saturation of the input transistors, thus eliminating storage time. The 1.24 k resistor as shown in Figure 1 stabilizes circuit operation for wide variations of transistor β. A logical "1" for MECL is -.75 V which corresponds to one base-emitter voltage drop below ground. Logical "0" is -1.55 V which yields a nominal voltage swing of 800 mV.

Normal circuit operations is as follows: a fixed reference voltage of -1.15 V is applied to the V_{BB} input as shown in Figure 1. This voltage is chosen half way between the "0" and "1" logic levels which establishes the noise margins of the basic circuit. For example with no input to the gate, A_1, A_2 at a zero level or less, transistors A_1 and A_2 will be in a cutoff condition. Point E will now be one V_{B-E} drop below V_{BB} or at -1.90 V. For a logic "0" input A_1 and A_2 are forward biased by only .35 V which is insufficient to cause any current flow. If a logic "1" is now applied to A_1 or A_2, point E is one V_{B-E} drop lower in potential or (-.75 V) -.75 V or -1.50 V. Transistor B is now only forward biased by .35 V which leaves it cutoff. The current that passed through B has now been switched to the input transistor. The current through B was $\frac{-1.90\text{ V} - (-5.2\text{ V})}{1.24\text{ k}} = 2.66$ mA while the current for a "1" input is $\frac{-1.50\text{ V} - (-5.2\text{ V})}{1.24\text{ k}} =$ 2.98 mA which yields a gate that draws almost constant current.

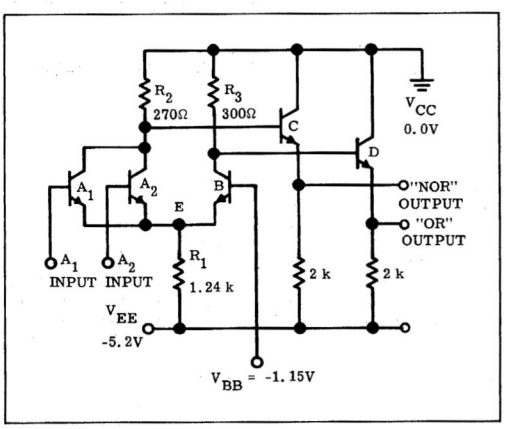


FIGURE 1 — OPERATION OF THE BASIC MECL GATE

The voltage at the collector of B (when conducting) is 0 - (300Ω x 2.66 mA) = -800 mV, while the voltage across the 270Ω resistor for a "1" input is 0 - (270Ω x 2.98 mA) = 800 mV. Transistors C and D are emitter followers; therefore the "NOR" and "OR" output voltage will follow the respective base voltage with a difference of -.75 V. If inputs are all low (logic "0"), the base of C will be at ground potential and the NOR output will be -.75 V (logic "1"). If one or more of the inputs are high, the base of C is at -.800 V and the NOR output drops to a logic "0". Operation of the OR output is similar only with no logic inversion.

The ratios of the collector resistors to the emitter resistor of the differential inputs determine the output "0" levels. Since accurate ratios of resistors are easier to obtain than absolute values of resistance, MECL output levels exhibit good uniformity from device to device. The absolute values of resistance are chosen as a compromise between speed of operation and power dissipation. As the power supply voltage is increased, the "0" level will move more negative while the "1" level remains constant. If V_{BB} is obtained from a Bias Driver connected to the same supply, the reference voltage will track with supply voltage changes or temperature variations, thus keeping V_{BB} in the center of the logic levels. At V_{EE} = -6 V for example, the nominal logic swing is 1.0 V. Not only is the logic swing increased and the noise margin bettered by about 50 mV, but power dissipation is increased as the square of the voltage. It is seen that the choice of V_{EE} = -5.2 V is a compromise between noise immunity and power dissipation. Nominal power dissipation for the basic gate is 37 mW while worst case should be considered as 20% higher.

Since the "1" level output is clamped to one V_{B-E} drop below V_{CC}, any noise appearing on the V_{CC} bus will appear on the output with very little attenuation. While any noise on the V_{EE} line will be attenuated by a factor of 4 to 5 which is primarily due to the ratio of R_1 to R_2 or R_1 to R_3. In most systems the ground plane or bus is the lowest impedance and therefore has the most constant potential and least induced noise. For this reason, the V_{CC} supply for MECL is usually obtained from ground. Another advantage of having V_{CC} at ground potential is that the gate outputs may be shorted to ground without drawing excessive current. If an output is accidently shorted to V_{EE} set at -5.2 V, the gate will draw excessive current (about 200 mA) but permanent damage does not occur until V_{EE} is increased to -8 V or -9 V and the current exceeds 400 mA.

Figure 2 shows the typical input characteristics of a MECL gate (input current vs. input voltage). Figure 3 shows output voltage vs output current over the full temperature range.

The input current is less than .1 mA and the output voltage level does not degrade for a load of 2.5 mA. D.C. fan-out is then 2.5 mA/.1 mA or 25. This is a D.C. fan-out and does not hold for high frequency operation. In fact, a maximum A.C. fan-out of 15 is recommended for high-speed operation. This decrease in fan-out is caused by the input capacitance of a gate, about 5 pF, and the wiring capacitance associated with a practical circuit. For a fan-out of 15, rise time is increased by about 5 ns while fall time will be increased by about 15 ns compared to the nominal values at a fan-out of one. The reason for the increase is that when switching from a zero to a one level, the low output impedance of the emitter follower charges the shunt capacitance, while switching from a one to a zero it is primarily the 2 k resistor that discharges the capacitance to the zero level.

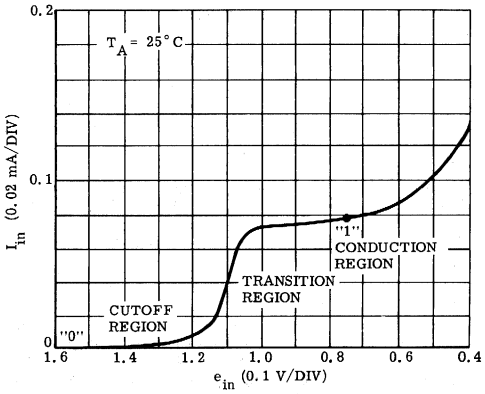


FIGURE 2 — INPUT CHARACTERISTICS OF A MECL GATE

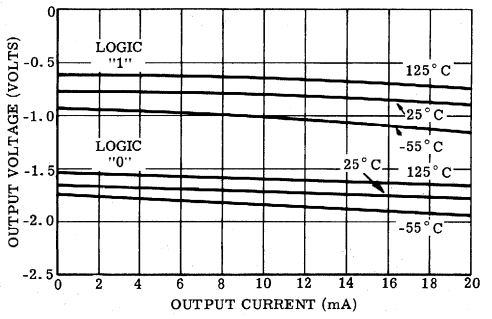


FIGURE 3 — OUTPUT VOLTAGE versus OUTPUT CURRENT

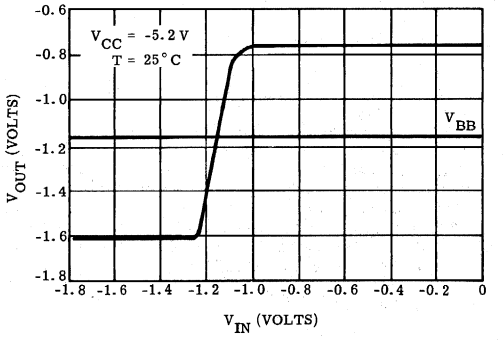


FIGURE 4 — TYPICAL "OR" TRANSFER CHARACTERISTICS

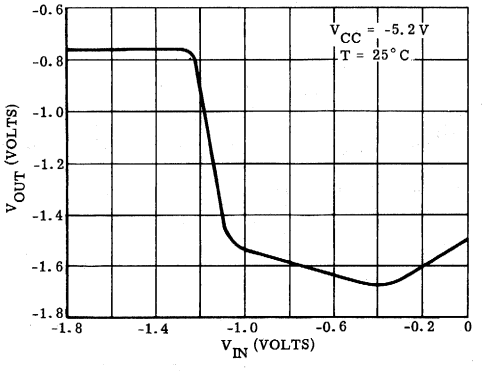


FIGURE 5 — TYPICAL "NOR" TRANSFER CHARACTERISTICS

The output of two gates may be connected in a "wired-OR" configuration, i.e. the gate outputs are wired together and whenever one or the other or both go high, the output goes high. For wired-OR operation, the worst case fan-out is 5 gate loads. Note that the pull down resistor is now effectively 1 k instead of 2 k and the fall time will be corresponding shorter.

Examination of the "OR" characteristic (Figure 4) shows that as the input voltage goes positive from a "0" level, the OR output may start to go positive at about -1.3 volts and will have reached a "1" level by about -1.0 V input. It may be shown that the 10%- to 90% transistion width is approximately 115 mV at 25°C regardless of circuit characteristics.* From Figure 1 it can be seen that as the input goes more positive, transistor B remains cut off and the output level remains constant. The "NOR" characteristics show that the width of the active region is about 200 mV. As the input goes more positive than the transition, the output continues to go more negative with a slope of about 1:4. This slope is due to the collector of the particular input transistor going more negative as the input goes more positive (the transistor is approaching saturation). As the input voltage approaches about -.4 volts at 25°C or -.6 V at 125°C, the input transistor reaches saturation. Saturation occurrs with about .45 volts forward bias on the base-collector junction at 25°C and about; .3 V forward bias at +125°C. Under saturation, the collector voltage will start to follow the base input and hence the output will also start to follow the input. The slope is about 0.8:1 since the voltage across the base to collector junction increases with heavier saturation. It should be noted that saturation does not start until an input of -.6 V is reached at 125°C ambient. The worst case "1" level is -.525 V which allows very slight saturation under absolute worst case conditions. The saturation is minimal so that the output rise and fall times are only slightly affected. For high speed operation, input levels should never go more positive than a most positive "1" level.

In consideration of maximum D.C. fan-out at maximum temperature, the input characteristics in Figure 2 show increasing current for -.6 to -.5 volts input, which may occur at worst case at high temperature. Fan-out does not actually decrease since if 25 inputs all drawing high current were connected to a gate with V_{out} = -.525 V, higher than normal current would be drawn from the emitter follower and drop the output level to perhaps -.58 V. The 25 loading gates now have a more negative input and will draw less current. These two effects balance each other and maximum fan-out need not be reduced at high temperature. Worst case fan-out cannot occur at high temperature for a most positive "1" level and actually increased fan-out is available.

The following curves illustrate worst case noise margins of MECL IC'S. The curves include the variations of

*Characterization of Integrated Logic Circuits, J.A. Narud and C.S. Meyer p 1551. Proceedings of the IEEE Special issue on Integrated Electronics, Dec. 1964

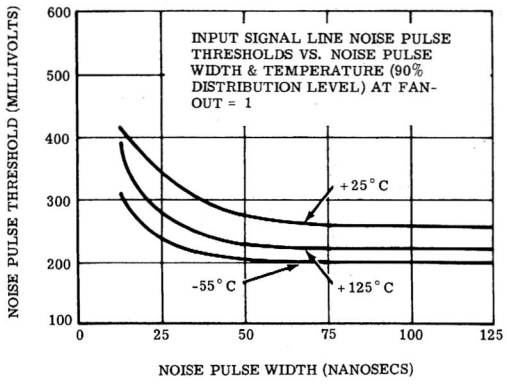


FIGURE 6 — INPUT SIGNAL LINE NOISE PULSE THRESHOLDS versus NOISE PULSE WIDTH AND TEMPERATURE

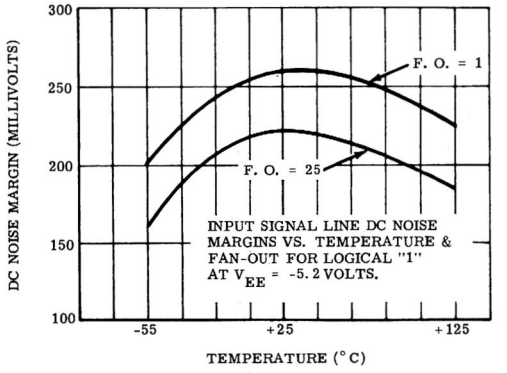


FIGURE 7 — INPUT SIGNAL LINE D.C. NOISE MARGIN versus TEMPERATURE AND FAN-OUT

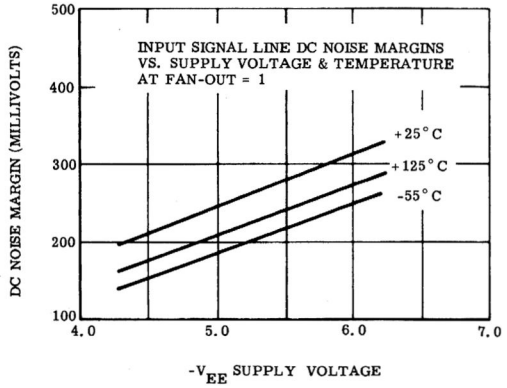


FIGURE 8 — INPUT SIGNAL LINE D.C. NOISE

V_{BB} and assure that 90% of the devices tested will have greater noise immunity than that shown:

Noise margins are slightly better for noise injected on the V_{CC} supply to the MECL gate under test and about four times better for noise injected on the V_{EE} supply.

Since the MECL gate has a differential amplifier input, it is of interest to note the common and differential mode gains. To measure these gains, one input transistor and the reference transistor are biased in the active region, i.e. neither transistor is cut off or saturated. To measure the common mode gain, a gate input such as (A_2) and the (V_{BB}) input are commoned. (Refer to Figure 1.) A nominal input of -1.15 V will center both transistors in the active region. An incremental voltage is now applied to the input while the "NOR" or "OR" output voltage with respect to common is recorded. The "NOR" common mode gain is approximately 1/9 or -19 dB while the "OR" common mode gain is about 1/7.5 or -17.5 dB. The difference arises due to the values of the collector resistors being different (270 and 300 ohms). The differential gain of the input is measured by connecting the V_{BB} input to -1.15 V and applying an incremental voltage centered around -1.15 V to an input transistor such as A_2, the "NOR" or "OR" output voltage is then noted with respect to ground. The differential "NOR" gain is about 5.6 or 14.5 dB while the differential "OR" gain is typically 6.0 application note AN-187. 100 foot twisted pair lines may be driven without problems by using MECL. The "OR" and "NOR" outputs of a gate drive one end of the line while a logic input and the V_{BB} input of a gate act as a differential receiver for the line. The line is terminated at the receiver input with a resistor of about 130Ω.

A better understanding of MECL may also be obtained from the typical curves (Figures 9, 10, and 11) that follow. These curves will answer system questions, concerning power dissipation vs temperature and supply voltage, and change in transfer characteristics with change in supply voltage.

GENERAL DESIGN RULES FOR MECL

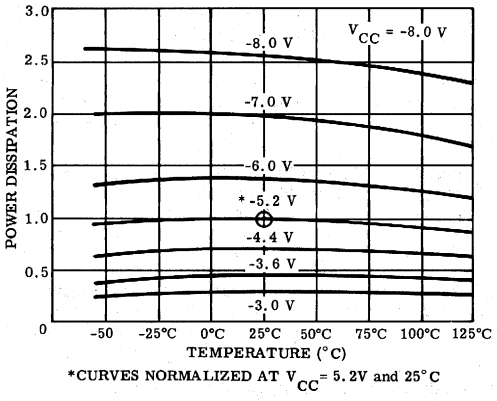
1. The maximum recommended A.C. fan-out for MECL is 15 unit input loads. D.C. fan-out is 25 unit loads. The A.C. fan-out is lower than the D.C. fan-out due to the increase in fall time and rise time with high fan-out. Also, if high fan-outs and long leads are used, overshoot due to lead inductance becomes a problem.

2. The Bias Driver (MC304, MC354) will fan-out to 25 gate loads. A dual gate or Half Adder is equivalent to two gate input loads for the Bias Driver.

3. Each $\overline{J}$ or $\overline{K}$ input to a flip flop is equivalent to one and one-half loads. For example, a $\overline{J}$ and $\overline{K}$ input tied together as a flip flop clock input would be a load of three, allowing a gate to drive five flip flops. All other inputs are a load of unity.

4. The outputs of two gates may be tied together to perform the "wired-OR" function, in which case a maximum fan-out of 5 is allowed. If only one pull down resistor is utilized, each additional common output is equivalent to one gate load. For example, if 6 gates are wired together with only one pull-down resistor connected, the fan-out would be (15) -5 or a fan-out of 10 remaining.

5. All unused inputs must be tied to V_{EE} for reliable operation. As seen from the gate input characteristics, the input impedance of a gate is very high when at a low level voltage. Any leakage to the input and/or wiring capacity of the gate will gradually build up a voltage on the input. This may ef-



*CURVES NORMALIZED AT V_{CC} = 5.2V and 25°C

FIGURE 9 — NORMALIZED POWER DISSIPATION FOR A MECL SYSTEM versus TEMPERATURE AND SUPPLY VOLTAGE

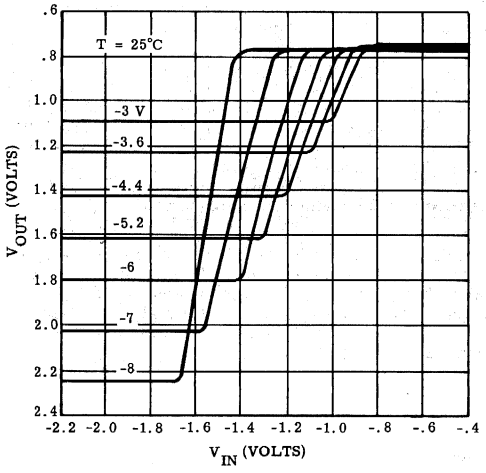


FIGURE 10 — TYPICAL "OR" TRANSFER CHARACTERISTICS versus SUPPLY VOLTAGE

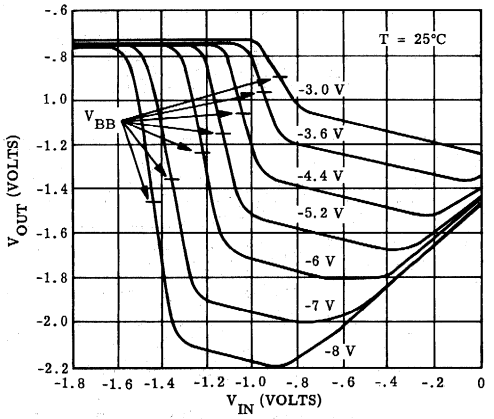


FIGURE 11 — TYPICAL "NOR" TRANSFER CHARACTERISTICS versus SUPPLY VOLTAGE

fect noise immunity of the gate or hinder switching characteristics at low repetition rates. Returning the unused inputs to V_{EE} insures no buildup of voltage on the input and a noise immunity dependent only upon the inputs used.

6. A recommended maximum of three input expanders should be used. For example, the MC306/MC307, MC356/MC357 gates would then have a fan-in of 18 available. If more than three input expanders are used, the NOR output rise and fall times suffer noticeably because of the increased capacitance at the collector node of the input transistors. For low frequencies, higher fan-ins may be employed if rise and fall times are of no significance.
7. Each gate package must have external bias supplied (V_{BB}) except for gates with internal reference such as MC312, MC313, MC362A, MC363, MC369, and the flip flops.

MECL IC's -55°C to +125°C

MC301	5-input OR, NOR
MC302	DC R-S Flip Flop, Outputs buffered, Reset input expandable
MC303	Half Adder--Sum, Carry, NOR
MC304	Bias Driver
MC305	5-input Expander
MC306	Expandable 3-input OR, NOR
MC307	Expandable 3-input OR, NOR, No pull-down resistors
MC308	J-K Flip Flop, DC R-S, Buffered outputs
MC309	Dual 2-input NOR, Both pull-down resistors
MC310	Dual 2-input NOR, One pull-down resistor, One optional
MC311	Dual 2-input NOR, One optional pull-down resistor
MC312	Dual 3-input NOR
MC312A	Dual 3-input NOR with Bias Driver
MC313F	Quad 2-input NOR with Bias Driver
MC314	J-K Flip Flop, DC R-S, High speed, Buffered outputs
MC315	Line Driver
MC316	Lamp Driver
MC317	Lever Translator MECL to DTL
MC318	Level Translator DTL to MECL

MECL IC's 0° to +75°C

MC351	5-input OR, NOR
MC352	DC R-S Flip Flop, No output buffers, Reset input expandable
MC352A	Same as MC302
MC353	Half Adder--Sum, Carry, NOR
MC354	Bias Driver
MC355	5-input Expander
MC356	Expandable 3-input OR, NOR
MC357	Expandable 3-input OR, NOR, No pull-down resistors
MC358A	J-K Flip Flop, DC R-S, Buffered outputs
MC359	Dual 2-input NOR, Both pull-down resistors
MC360	Dual 2-input NOR, One pull-down resistor, One optional
MC361	Dual 2-input NOR, One optional pull-down resistor
MC362	Dual 3-input NOR
MC362A	Dual 3-input NOR with Bias Driver
*MC363F	Quad 2-input NOR with Bias Driver
MC364	J-K Flip Flop, DC R-S, High speed, Buffered outputs
MC365	Line Driver
MC366	Lamp Driver
MC367	Level Translator MECL to DTL
MC368	Level Translator DTL to MECL
*MC369G	Dual-2 OR, NOR Clock Driver and High speed gate
*MC369F	Dual-4 OR, NOR Clock Driver and High speed gate

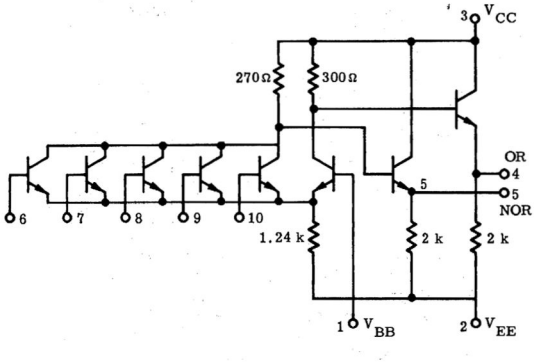
*F indicates a 14 lead flat package
*G indicates a TO-5 type package

TABLE 1 — MECL LOGIC ELEMENTS

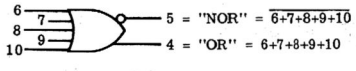
THE MECL FAMILY OF IC LOGIC ELEMENTS

The following section includes a complete explanation of each logic element. Schematics, logic diagrams, logic equations, and truth tables, where applicable, are included along with a detailed description of each circuit.

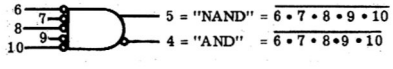
5 INPUT OR, NOR: MC301, MC351



POSITIVE LOGIC
SINGLE GATE

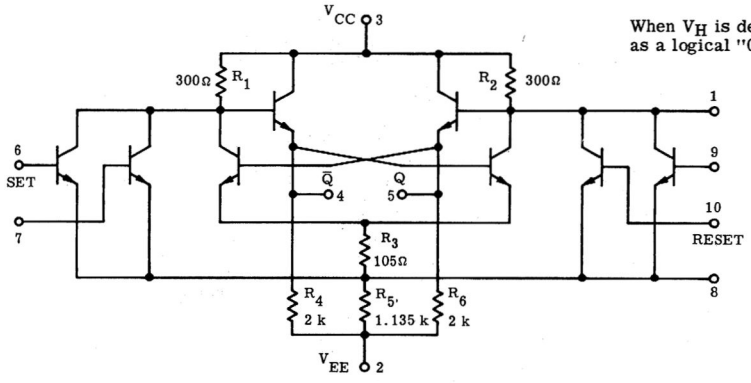


NEGATIVE LOGIC
SINGLE GATE

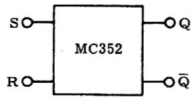


The 5-input gate obtains the maximum number of inputs for a standard TO-5 10-pin can. A pair of the gates may be wire-OR'd to form a 10-input gate. If desired, both NOR's and OR's may be wired together giving a gate that has the properties of a single gate with a fan-out of 5, fast fall time, and 10 inputs. Nominal power dissipation of the gate is 37 mW over the temperature range. Typical propagation delay is 8 ns with rise and fall times of 8 ns. As fan-out increases above 5, the fall time increases more rapidly than the rise time.

DC R-S FLIP-FLOP: MC352



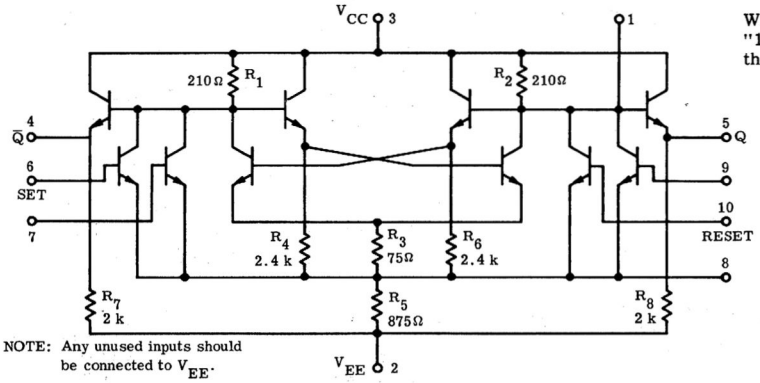
When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:



R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

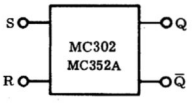
The D.C. R-S flip flop is most useful as a storage element. Dual inputs allow the OR function to be performed at the Set or Reset inputs. As may be noted from the schematic the Reset input is expandable. A maximum of 2 or 3 expanders is recommended for high speed operation since the additional collector node capacitance increases rise and fall times. The Set input may also be expanded by redefining inputs and switching the wiring of Q and $\overline{Q}$. The Set and Reset inputs should be standard MECL levels for optimun operation. Input rise and fall time is unimportant unless high speed operation is desired. Typically, the maximum speed of Set-Reset operation is 65 MHz, propagation delay 6.5 ns, rise and fall times 8 ns, and power dissipation 42 mW. The maximum Set-Reset speed is obtained for inputs with about 6 ns rise and fall times and a pulse widths of about 9 ns.

DC R-S FLIP-FLOP, OUTPUTS BUFFERED, RESET INPUT: MC302, MC352A



NOTE: Any unused inputs should be connected to V_{EE}.

When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:

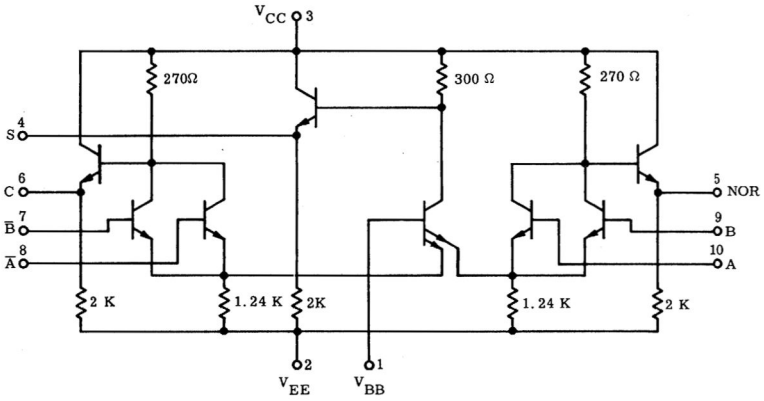


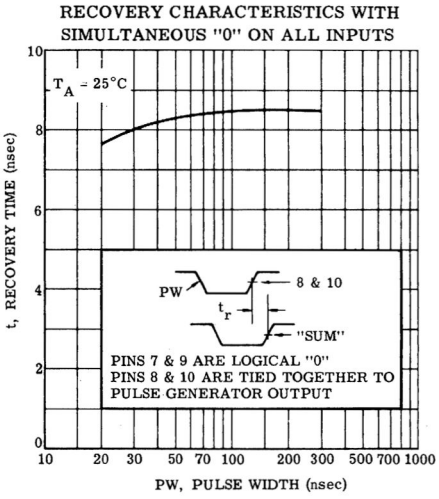
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

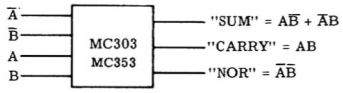
This flip flop is essentially the same as the MC352 with the exception that the outputs are isolated. The MC352 is sensitive to noise on the output lines because they feed back directly into the bases of the bistable transistors. The output emitter followers on the MC302, MC352A isolate each output from the respective base of each bistable transistor; giving about 800 mV noise margin for noise coupled into the output.

It should be noted that if both the set and reset inputs are high, both outputs will be low. Bringing both inputs to "0" simultaneously leaves the output in an undefined state, i.e. either a "0" or a "1". Typical parameters: rise time 11.5 ns fall time 12.5 ns, propagation delay time 11 ns, power dissipation 45 mW. The flip flop may be set and reset at a maximum rate of about 50 MHz. Optimum input pulses for 50 MHz operation should have rise and fall times of 6 ns or less with pulse widths of about 14 ns.

HALF ADDER, SUM, CARRY, NOR: MC303, MC353







HALF ADDER Truth Table

Pin #	A 10	B 9	$\overline{A}$ 8	$\overline{B}$ 7	OUT 4
	Lo	Lo	Hi	Hi	Lo
	Lo	Hi	Hi	Lo	Hi
	Hi	Lo	Lo	Hi	Hi
	Hi	Hi	Lo	Lo	Lo

The Half Adder is a very useful element of the MECL family. It can be used as a digitally controlled inverter, a digital comparator, or to provide SUM, CARRY, and NOR, or SUM and $\overline{SUM}$ if desired. Normally two bits and their compliments are applied to the Half Adder so that two of the inputs are always high as shown in the schematic. If all four of the inputs are low, the V_{BB} transistor will be sinking twice the normal current at 25°C and the SUM output will drop to -2.3 V. This does no harm but to saturate the V_{BB} transistor. The graph shown above illustrates the recovery time at 25°C for saturation of the V_{BB} transistor. At higher temperatures it would take longer to recover.

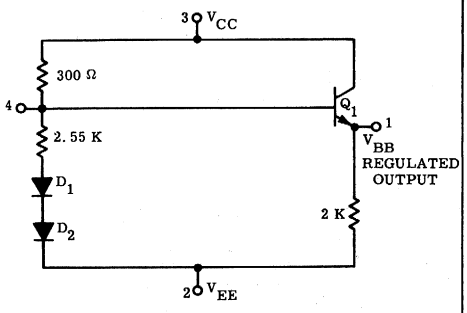
The Half Adder gating functions are the same as the general MECL gate shown in Figure 1 with the exception that the bias transistor performs the AND function, in that when both emitters are high, the SUM output is also high. With reference to the schematic and the letters representing the inputs, it is seen that the collector of the V_{BB} transistor is high when A and $\overline{B}$ are high or $\overline{A}$ and B are high. This represents the exclusive OR function or the sum of A and B. The Carry and NOR outputs may be wired together to form $A\overline{B} + \overline{A}B$ which may be recognized as $\overline{SUM}$. By the rules of Boolean Algebra: $SUM = A\overline{B} + \overline{A}B$ then $\overline{SUM} = \overline{A\overline{B} + \overline{A}B} = \overline{(A\overline{B})} \cdot \overline{(\overline{A}B)} = (\overline{A}+B)(A+\overline{B}) = \overline{A}\overline{B} + AB$ which is the wired output.

A digitally controlled inverter is one unique application of the MECL Half Adder. The inputs are connected in the same manner as for the SUM function. If A is considered as the digital information input and $\overline{B}$ as the control level (inversion or not inversion), then A appears at the S output if $\overline{B}$ is high and $\overline{A}$ appears at the S output if B is high. Thus A or $\overline{A}$ is obtained on the same wire according to the level of B.

The propagation delay of the circuit is typically 8 ns for the SUM output and 6 ns for the Carry and NOR outputs at room temperature at a fan-out of one gate. Rise times are typically 6.5 ns for all outputs while fall times are 8.5 ns for SUM and 8.0 ns for NOR and CARRY. Typical power dissipation is 65 mW.

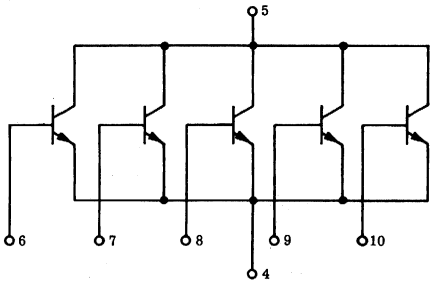
The Half Adder is shown in a digital comparator circuit and a five bit asynchronous adder in the last section of the paper.

BIAS DRIVER: MC304, MC354



The Bias Driver provides a temperature and voltage compensated reference for MECL logic. Any of the three MECL voltages may be grounded, but the common voltage of the Bias Driver must correspond to that of the logic system. The device has a unique application when coupling a signal through a capacitor to pin 4. First the gate acts as a level translator from any voltage to MECL levels. If the input is 800 mV p-p, the standard MECL levels will appear at pin 1. For low level A.C. and R.F. inputs, the output will be centered in the active region of a MECL gate which may then be used as an amplifier. A low quality, high bandwidth differential amplifier may be obtained by using two bias drivers, one connected to a normal gate input and the other connected to the V_{BB} input of a MECL gate. The "OR" and "NOR" outputs then provide a very low impedance differential output. The A.C. input impedance of the Bias Driver is 250Ω in parallel with about 5 pF which will terminate a low impedance line fairly well. If V_{CC} contains excessive noise the output on pin 1 may be filtered by connecting a capacitor between pin 4 and 2. Typical power dissipation is 17 mW. The Bias Driver will fan-out to 25 unit input loads.

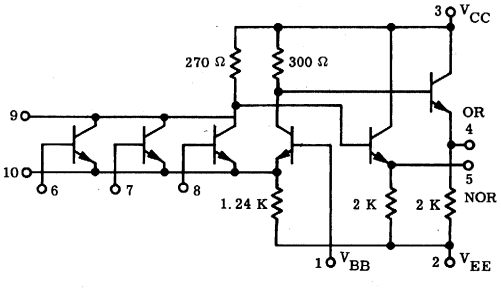
5 INPUT EXPANDER: MC305, MC355



The Gate Expander acts as a 5-input NOR gate when referring to the collectors or as a 5-input OR gate when referring to the emitters. This infers a resistor connected from the collector to a high level voltage while the emitter node is connected to a low voltage through another resistor.

The maximum number of recommended expanders to be used with a gate is three for high speed operation. If more than three expanders are used, the output rise and fall times will become excessive for high speed operation. When used with a MECL gate, power dissipation is negligible.

EXPANDABLE 3 INPUT OR, NOR: MC306, MC356

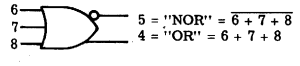


This gate may be expanded to 18 inputs by use of the MC305 or MC355, otherwise operation is the same as the basic MECL gate shown in Figure 1.

POSITIVE LOGIC

When V_H is defined as a logical "1" and V_L as a logical "0" the "OR"/"NOR" function is performed:

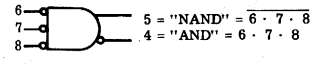
Single Gate



NEGATIVE LOGIC

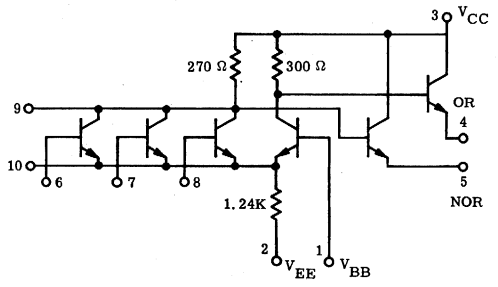
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "AND"/"NAND" function is performed:

Single Gate



Propagation delay time is typically 6.5 ns with a rise and fall time of 7 ns. Typical power dissipation is 37 mW.

EXPANDABLE 3 INPUT OR, NOR, NO PULL-DOWN RESISTORS: MC307, MC357

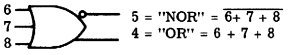


This gate is the same as MC306, MC356 except that the output pull-down resistors have been removed lowering the power dissipation. Propagation delay time is nominally 6.5 ns with rise and fall times of 7 ns with a normal load. The output of this gate may be wire-OR'd with other MC307, MC357 gates and one gate that has a pull-down resistor to -5.2 V. This will result in a large power savings since the gate only dissipates 16 mW at V_{EE} = -5.2 V. The maximum recommended number of gates connected in this manner is: 1 gate with a pull-down resistor, 14 gates with no pull-down resistor and the input of another MECL gate. In other words, the gate with the pull-down resistor, such as the MC301 or MC306, has a recommended maximum fan-out of 15. Each of the other wire-OR'd gates is the equivalent of one load, resulting in a fan-out of 1 to the input of another MECL gate.

POSITIVE LOGIC

When V_H is defined as a logical "1" and V_L as a logical "0" the "OR"/"NOR" function is performed:

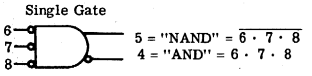
Single Gate



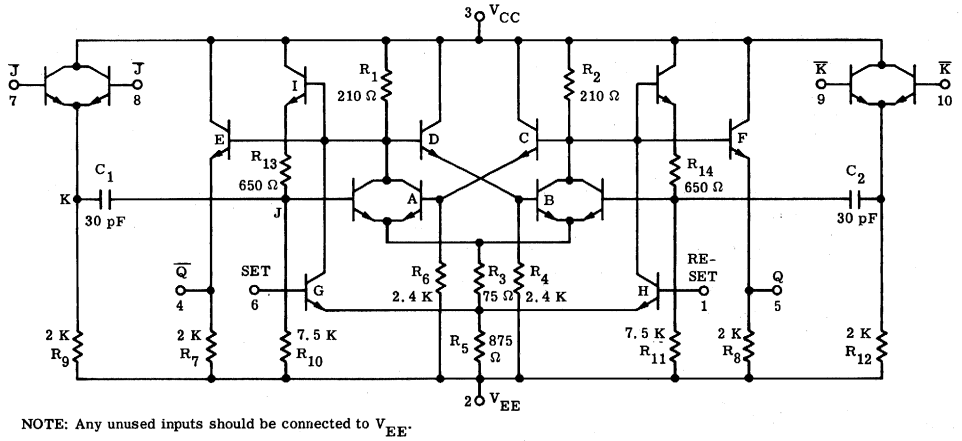
NEGATIVE LOGIC

Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "AND"/"NAND" function is performed:

Single Gate

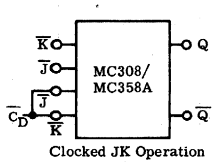


J-K FLIP-FLOP, DC R-S, BUFFERED OUTPUTS: MC308, MC358A



NOTE: Any unused inputs should be connected to V_{EE}.

When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:



Clocked JK Operation

State #	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^{n+1}
1	ø	ø	0	Q^n
2	0	0	1	$\overline{Q}^n$
3	0	1	1	1
4	1	0	1	0
5	1	1	1	Q^n

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state.

Set-Reset operation is the same as MC302.

Operation of the MC308, MC358A

Transistors A and B form the "heart" or bistable pair of the flip flop. The collector of B is coupled back to the base of A through C, likewise D couples A back to B forming the bistable element. The output of A is buffered through E to give the $\overline{Q}$ output, while F buffers B to give the Q output. When the Set input (pin 6) goes to a high level (-0.75 V), the collector of G goes low pulling A and D low. The collector of B then goes high which holds the collector of A low through C. The flip flop is now Set to the "1" state, i.e. Q high and $\overline{Q}$ low. Likewise a high level in or a positive pulse on pin 1 resets the flip flop to the "0" state. Since the base of either A or B is at a one level (-0.75 V), the emitters will be one V_{BE} drop lower or at -1.50 V. The potential at the node between R_3 and R_5 is then -1.8 V which corresponds to a

continued

nominal 400 mV noise immunity for a Set or Reset input normally at -1.55 V (logic "0"). The Set, Reset input transistors may be considered to be in the active region at 0.65 V_{BE}.

The emitter of I also follows the collector of A and will yield standard MECL levels. The voltage at point J will then be approximately -1.1 or -1.85 due to the divider action of R_{13} and R_{10}. The $\overline{J}$ inputs on pins 7 and 8 act as emitter followers so that point K will be either -1.5 or -2.3 V. C_1 differentiates the input as it appears at point K. Whenever point K swings negative, nothing will happen, but when point K goes positive, a positive pulse will be coupled to the base of the transistor in parallel with A. If the collectors of the pair were high, they will be brought to a low level as if the flip flop had received a Set pulse. Likewise a positive going level at C_2 will reset the flip flop.

It should be noted that the input rise time must be less than a specified value to transfer enough charge through the capacitor to switch the flip flop. Also the maximum toggle speed of the flip flop is limited by the internal time constants associated with C_1 and C_2. If one of the $\overline{J}$ inputs is high it will inhibit a positive going level on the other $\overline{J}$ input and no pulse will be coupled into the flip flop, unless excessive amplitude, perhaps caused by ringing on the input line, is applied. If differences in the logic levels and ringing both add up to 250 mV for 10 ns or more, it is possible to trigger a flip flop falsely. For worst case design over temperature extremes overshoot should be a maximum of 100 mV. Note the discussion on overshoot for the MC369.

The classical J-K flip flop has its inputs labeled J, K, and C and operates on negative levels. The MECL $\overline{J}$-$\overline{K}$ flip flop is opposite, in that high levels inhibit and positive going clock transitions actually clock the flip flop. The MECL levels generally are preferrable since positive logic is more common than negative logic.

As may be seen from the truth table and the logic diagram for clocked $\overline{J}$-$\overline{K}$ operation, a dynamic "0" or negative going clock does not affect the flip flop when the other $\overline{J}$ and $\overline{K}$ inputs are at a static level. If $\overline{C_D}$ and $\overline{K}$ are low and $\overline{J}$ goes high, the flip flop will be set to a "1" on the Q output. Likewise if $\overline{C_D}$ and $\overline{J}$ are low while $\overline{K}$ goes high, the flip flop will be reset to zero. For normal clocked operation, $\overline{J}$ and $\overline{K}$ are static levels changed only when C_D is high (flip flop inhibited). The symbol in the truth table, ϕ, refers to a static level of either high or low. For state 1 in the truth table, the flip flop output, Q, will be the same level at time t = n + 1 as it was at t = n for a dynamic "0" transition of the clock between t = n and t = n + 1. For state 2 neither $\overline{J}$ or $\overline{K}$ are inhibited, and a dynamic clock will toggle the flip flop, i.e. at t = n + 1 the flip flop will be in the opposite state that it was in at t = n. For state 3, the $\overline{K}$ input is inhibited and a "1" will be shifted into the flip flop. Likewise a "0" will be shifted in for state 4. In state 5, both inputs are inhibited and the flip flop will not change state unless a Set or Reset input is received. Set - Reset inputs take priority over the $\overline{J}$-$\overline{K}$ inputs as may be seen from the schematic. If an uninhibited clock input is received while the Set or Reset level is true (high), a 20 ns pulse of about 400 mV level may appear on the output of the flip flop.

MC308, MC358A Characteristics

As in every $\overline{J}$ $\overline{K}$ flip flop the MC308, MC358A requires a minimum down time of the clock to ensure toggle. Minimum down time of the clock waveform is determined primarily by the discharge time constant of R_9 and C_1 which is nominally 60 ns. After a high level input appears at point K, at least 29 ns under worst case conditions must be allowed for the voltage at point K to decay sufficiently so that the next positive going input will transfer enough charge through C_1 to reliably toggle the flip flop. The maximum guaranteed toggle frequency of the flip flop is 15 MHz with rise and fall times of 9 ns, down time of 29 ns, and 800 mV amplitude. The typical toggle frequency is above 20 MHz when driven from a gate with sharp rise and fall times. Maximum toggle frequency is very dependent upon clock rise time and clock amplitude. This dependence is caused by the variable sensitivity of the flip flop with input rise time changes. Refer to the following section on descriptive curves for MECL flip flops for data showing this relationship.

Typical propagation delay time is 7 ns while nominal rise and fall times are 7 ns and 8 ns respectively. Power dissipation is about 85 mW at V_{EE} = -5.2 V.

DESCRIPTIVE CURVES FOR MECL FLIP-FLOPS

The following data is most helpful to the designer in understanding the characteristics of

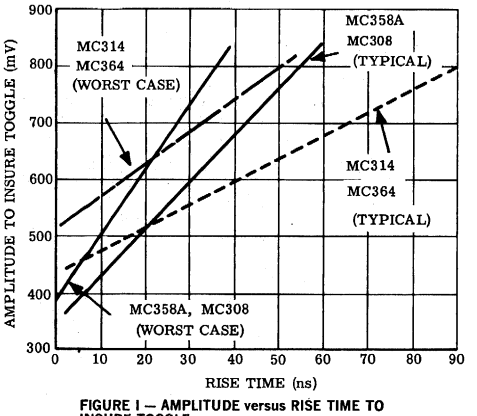


FIGURE I — AMPLITUDE versus RISE TIME TO INSURE TOGGLE

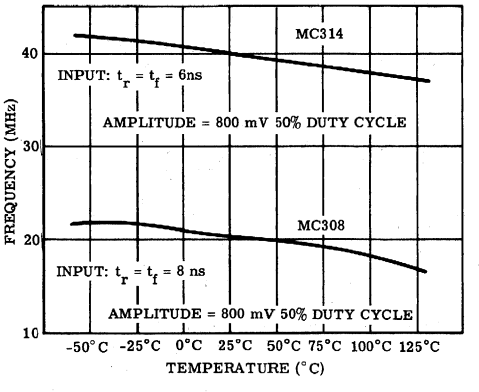
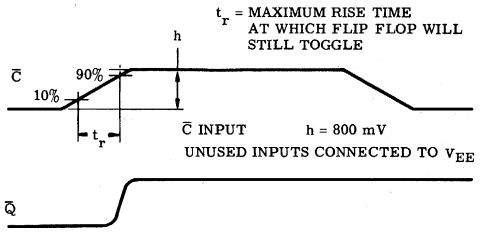


FIGURE II — TYPICAL TOGGLE FREQUENCY versus TEMPERATURE

continued

MECL flip flops. As may be seen from the data, typical characteristics can be much better than those specified for worst case. In fact, typical data usually runs about 30% better than worst case. For example, the distribution of characteristics is wide enough that for fast rise and fall times some of the MC314 flip flops will toggle reliably at 50 MHz. The curves are self-explanatory and include the test conditions for data shown in Figures I, II, III, IV, and V.



90% OF THE DEVICES WILL TOGGLE AT RISE TIMES EQUAL TO OR LESS THAN THAT SHOWN

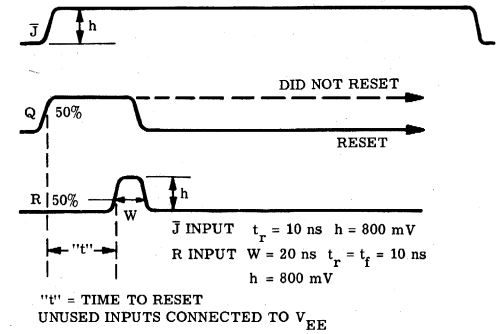
FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	60ns		70ns		90ns
MC364		60ns	70ns	85ns	
MC308	40ns		45ns		70ns
MC358A MC358		40ns	45ns	50ns	

NOTE: FOR WORST CASE DESIGN t_r SHOULD BE:

MC314, MC364: $t_r < 50$ns @ 800mV

MC308, MC358A: $t_r < 35$ns @ 800mV

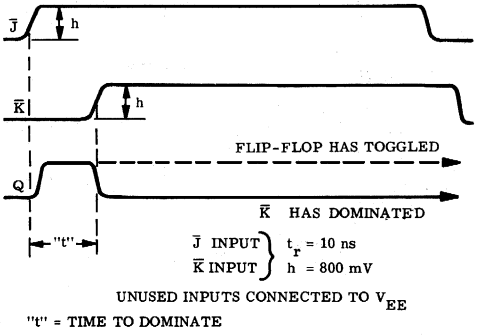
FIGURE III — MAXIMUM RISE TIME TO TOGGLE TEST



THE MAXIMUM VALUES ARE GIVEN BELOW WITH A 90% CONFIDENCE LEVEL

FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	2ns		1ns		1ns
MC364		6ns	3ns	7ns	
MC308	22ns		13ns		33ns
MC358A		18ns	9 ns	22ns	

FIGURE IV — MAXIMUM TIME TO RESET TEST

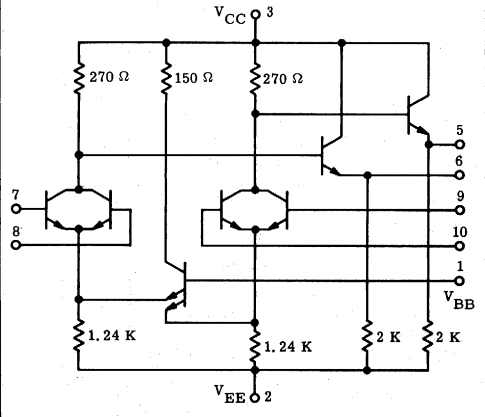


THE MAXIMUM VALUES ARE GIVEN BELOW WITH A 90% CONFIDENCE LEVEL

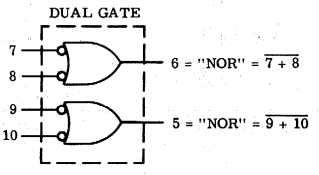
FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	20 ns		21 ns		16 ns
MC364		30 ns	32 ns	35 ns	
MC308	30 ns		33 ns		41 ns
MC358A		20 ns	21 ns	26 ns	

FIGURE V — MAXIMUM TIME TO DOMINATE TEST

DUAL 2 INPUT NOR, BOTH PULL-DOWN RESISTORS: MC309, MC359

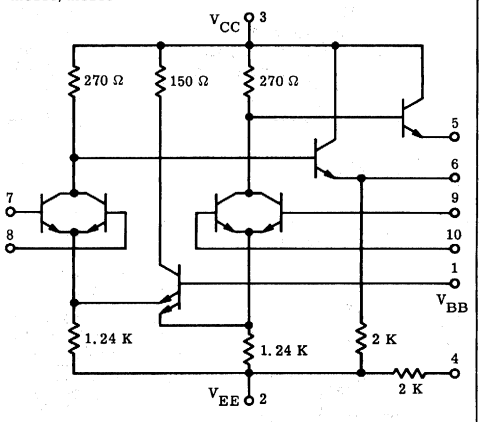


POSITIVE LOGIC
When V_H is defined as a logical "1" and V_L as a logical "0" the "NOR" function is performed:

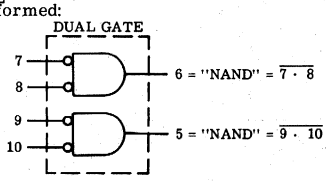


Use of the Dual 2-input NOR gate will usually result in a lower "can count" i.e. the total number of integrated circuits used in a given system. Note that pin 1 the bias driver input is equivalent to two standard loads due to the double emitter output. Typical propagation delay is 7 ns, with a rise time of 6 ns and fall time of 7.5 ns at 25°C. Nominal power dissipation is 55 mW.

DUAL 2 INPUT NOR, ONE PULL-DOWN RESISTOR, ONE OPTIONAL: MC310, MC360

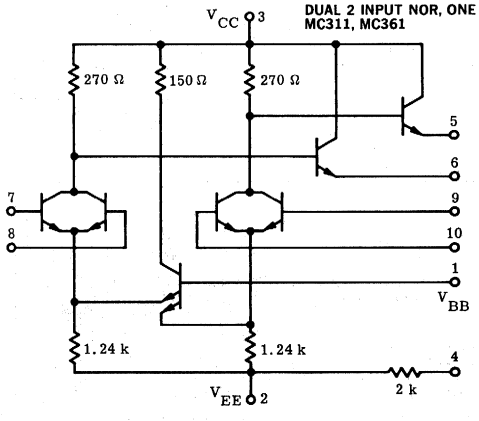


NEGATIVE LOGIC
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "NAND" function is performed:



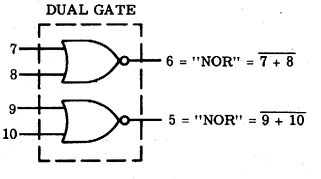
This gate is identical to the MC309, MC359, except that pin 4 allows the option of a pull-down resistor or power savings for the output on pin 5. Typical power dissipation with pin 5 connected to 4 is 55 mW, while it is only 43 mW at V_{EE} = -5.2 V without the pull down resistor. Typical propagation delay is 7 ns. Nominal rise and fall times are 6 ns and 7.5 ns respectively at room temperature.

DUAL 2 INPUT NOR, ONE OPTIONAL PULL-DOWN RESISTOR: MC311, MC361

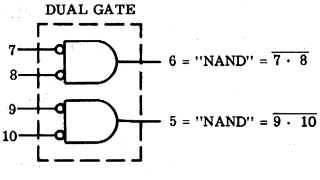


This gate is useful where wire-OR'd outputs are a savings. Both outputs are normally without pull-down resistors which reduces the nominal power dissipation to 31 mW. If the pull-down resistor on pin 4 is used, the nominal dissipation increases to 43 mW. Note the rules governing the wired-OR outputs under General Rules for MECL shown on a previous page. Propagation delay is typically 7 ns with 6 ns rise and 7.5 ns fall times at room temperature.

POSITIVE LOGIC
When V_H is defined as a logical "1" and V_L as a logical "0" the "NOR" function is performed:

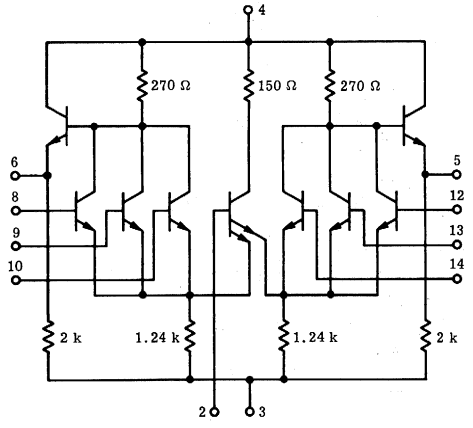


NEGATIVE LOGIC
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "NAND" function is performed:

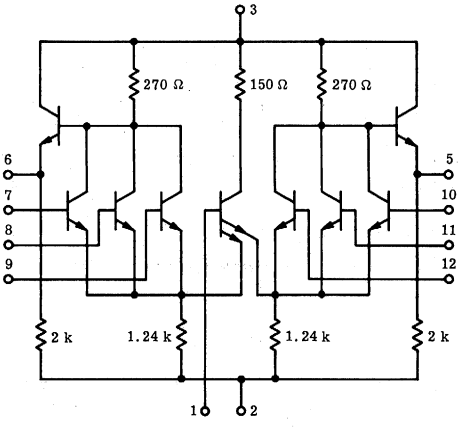


DUAL 3 INPUT NOR: MC312, MC362

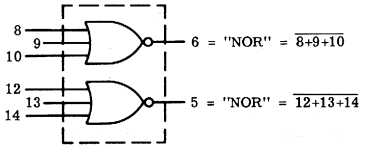
MC312F, MC362F



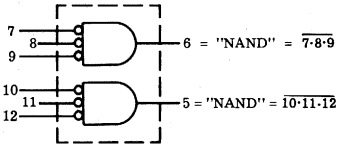
MC312G, MC362G



Positive Logic

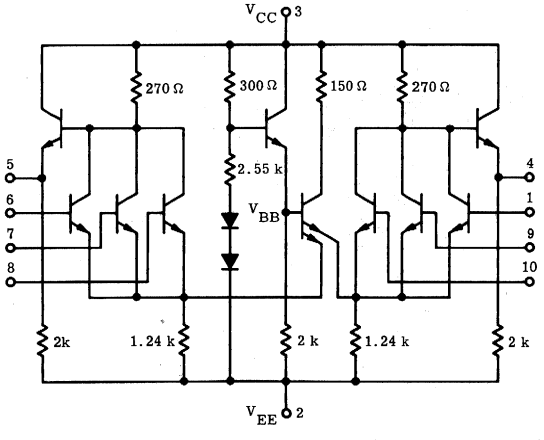


Negative Logic

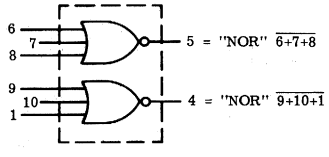


These circuits are preferred wherever three-input gates provide a savings. The F model is available in a 14-pin flat package while the G model number indicates a 12-pin TO-5 package. The typical power dissipation is 55 mW. Nominal delay time is 7 ns with output rise and fall times of about 7 ns.

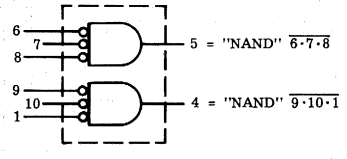
DUAL 3 INPUT NOR WITH BIAS DRIVER: MC312A, MC362A



Positive Logic

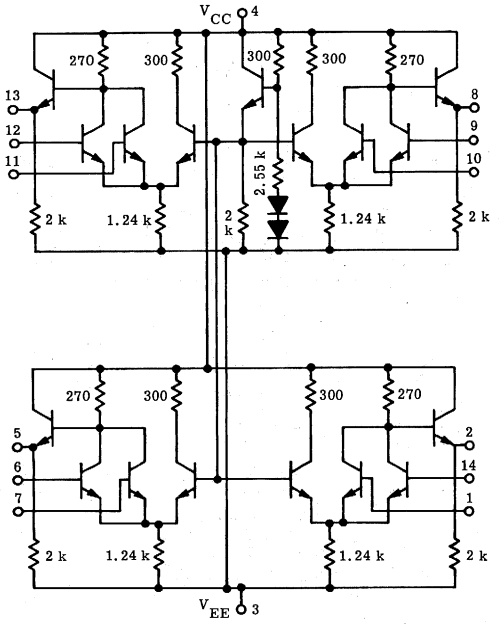


Negative Logic



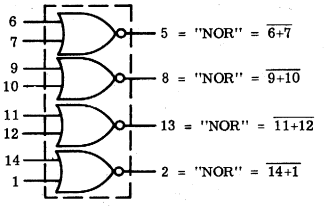
The MC312A, MC362A is essentially the same as the MC312, MC362 except that a bias driver is included on the same monolithic chip, allowing the circuit to be mounted in a 10-pin TO-5 can. Typical characteristics are: power dissipation 72 mW, propagation delay time 8.5 ns and rise and fall times of 9 ns.

QUAD 2 INPUT NOR WITH BIAS DRIVER: MC313F, MC363F



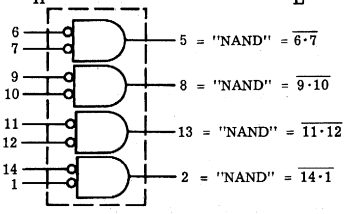
POSITIVE LOGIC

V_H is defined as logical "1", V_L as logical "0"



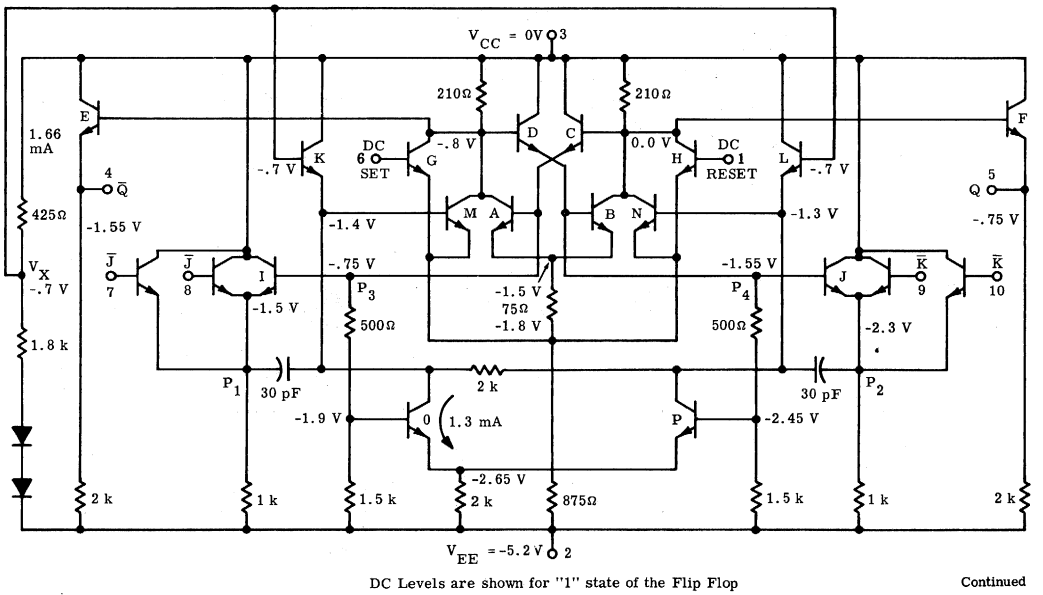
NEGATIVE LOGIC

V_H is defined as logical "0", V_L as logical "1".



The MC313F is available only in the 14-pin flat package due to pin-out limitations of the TO-5 configuration. This multiple function gate may be used to advantage in reducing the can count in a system. Typical power dissipation is 125 mW. Nominal propagation delay time is 7 ns, with a rise time of 6 ns and a fall time of 7.5 ns. The built-in bias driver not only saves a pin but effectively adds to the noise immunity because it sees a fixed load.

J-K FLIP-FLOP, DC R-S; HIGH SPEED, BUFFERED OUTPUTS: MC314, MC364



DC Levels are shown for "1" state of the Flip Flop

Continued

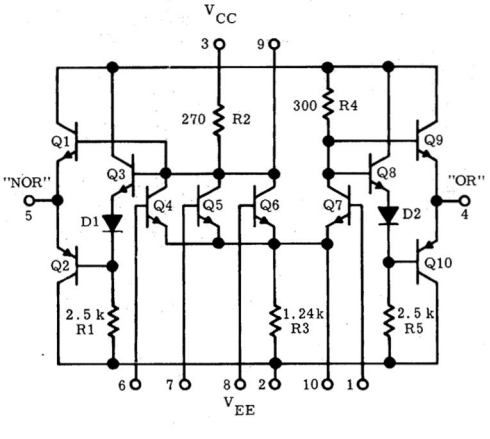
The MC314, MC364 utilizes 20 transistors and two junction capacitors in a high-speed design that guarantees a minimum toggle frequency of 30 MHz at room temperature while typical toggle frequency is 40 MHz at room temperature. Typical characteristics are: power dissipation 115 mW, propagation delay time 12 ns, rise time 13 ns, and fall time 12 ns.

The adjacent schematic shows the nominal D.C. levels for the flip flop in the "1" state, i.e. Q = -0.75 V. Transistors A through H function the same way as in the MC308, MC358A. A and B form the bi-stable element with feedback through D and C. Transistor G sets the flip flop to a "1" while H resets to "0". Transistors E and F buffer the outputs and prevent noise from feeding back into the flip flop from external sources. Transistor I is turned on ensuring that point P_1 is at -1.5 volts. This inhibits a normal MECL $\overline{J}$ input from affecting the state of the flip flop. A high $\overline{J}$ input would have no effect since P_1 is already at -1.5 V.

The K inputs are enabled and a positive going MECL level will couple charge through the 30 pF capacitor and raise the emitter of L to about -0.9 V at which point it is clamped by N which is forward biased and causes the flip flop to change state. As soon as the flip flop changes state, P_4 is raised from -1.55 V to -0.75 V which switches the constant current (1.3 mA) from transistor O to transistor P. This constant current discharges the 30 pF capacitor in about 10 ns. It is seen that the flip flop may be set or reset very soon after a $\overline{J}$ or $\overline{K}$ input has been received due to the rapid discharge of the capacitor. The 30 pF capacitor and the 1 k resistor also form a time constant that requires a minimum down time on a clocking waveform. The 30 ns time constant requires about 8 ns to decay from -1.5 V to -2.3 V with nominal values of R and C. This requires a down time of at least 10 ns at the 10% levels of the clocking waveform. The voltage V_X is internally generated to track with MECL levels over temperature and power supply variations. Transistors K and L are very lightly turned on. One of them, depending upon the state of the flip flop, supplies current for the constant current source employing transistors O and P and the 2 k resistor to V_{EE}. The 2 k resistor between collectors provides a 50 μa pull-down current for either K or L depending upon which is not providing the 1.3 mA discharge current.

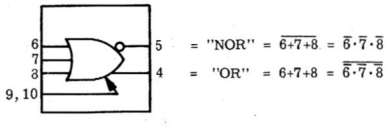
Logically, the MC314, MC364 design is identical with that of the MC308, MC358A. The electrical characteristics have some variations besides maximum toggle frequency. These are illustrated in the section containing MECL flip flop curves.

LINE DRIVER AND CAPACITANCE DRIVER: MC315, MC365

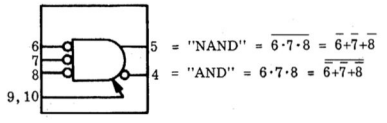


The MC315, MC365 is most useful whenever high speed digital information with little allowed degradation is to be transmitted over long distances without noise pickup. This circuit will drive coax of 50Ω impedance or higher with degradation dependent only upon line losses. Also high values of capacitance may be driven with good rise and fall times.

POSITIVE LOGIC - Simultaneous "OR"/"NOR"; V_H is defined as logical "1", V_L as logical "0".



NEGATIVE LOGIC - Simultaneous "AND"/"NAND"; V_H is defined as logical "0", V_L is logical "1".



The gate is a 3-input OR, NOR with bias voltage normally applied to pin 1. Unused inputs must be returned to -5.2 V. The outputs, pins 4 and 5, have active devices to both pull-up and pull-down the load as necessary. For a "1" level output (-0.75 V), the NPN output transistor is turned on giving the low output impedance of an emitter follower to charge any line capacitance. Very low impedance is also provided by the PNP emitter follower to discharge any line capacitance.

Continued

Maximum power dissipation with both outputs loaded to ground with 50Ω is 240 mW, which for maximum reliability requires a case temperature of 125°C maximum rather than 125°C ambient. With only one output loaded, 50Ω to ground, maximum power dissipation is 170 mW. Reducing the single load to 100Ω further decreases dissipation to 110 mW.

For a load of 50Ω and .001μF to ground, the propagation delay is typically 16 ns at room temperature while rise and fall times are about 20 ns. With 50Ω coax terminated in a 50Ω resistor, rise time is typically 15 ns and fall time 20 ns with propagation through the device of about 14 ns.

If the device is used as a capacitance driver, output rise and fall times and propagation delay times depend upon the value of capacitance. Typical curves showing this dependence are drawn below in figures A, B, C, and D. A 10Ω resistor was put in series with the load capacitor to prevent overshoot and ringing on the output waveform. The 10Ω resistor damps the series L-C circuit formed by lead inductance and the lumped capacitance. Without the resistor, overshoot may be about 300 mV depending upon the size of the capacitor. More information on driving lines from MECL outputs may be found in application note AN-187.

Figure E illustrates graphically definitions for rise, fall, and delay times.

For gate loaded 50Ω to ground with variable capacitance in parallel, figures F and G show output rise, fall, and delay times.

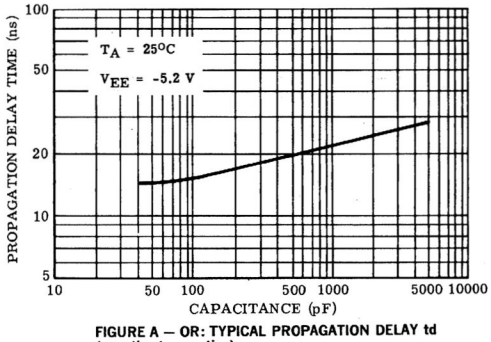


FIGURE A — OR: TYPICAL PROPAGATION DELAY t_d (negative to negative)

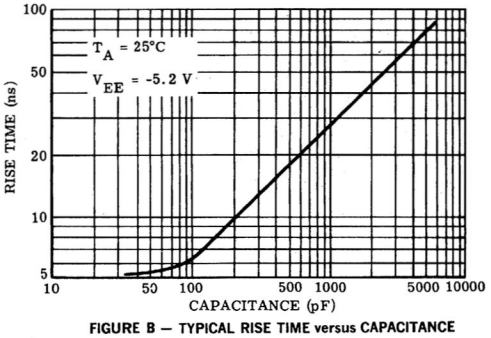


FIGURE B — TYPICAL RISE TIME versus CAPACITANCE

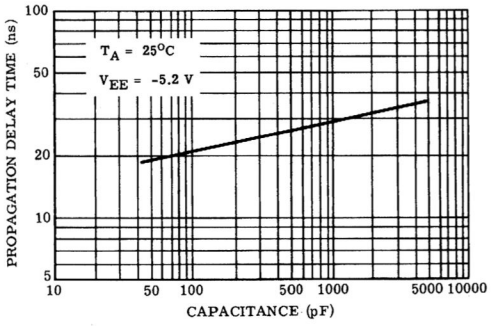


FIGURE C — OR: TYPICAL PROPAGATION DELAY t_{d_2} (positive to positive)

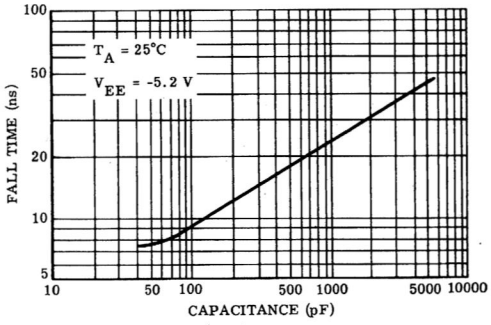


FIGURE D — TYPICAL FALL TIME versus CAPACITANCE

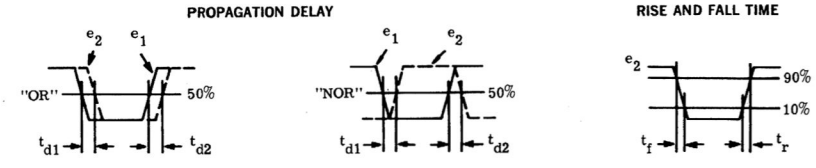


FIGURE E — RISE, FALL AND DELAY INTERVALS

Continued

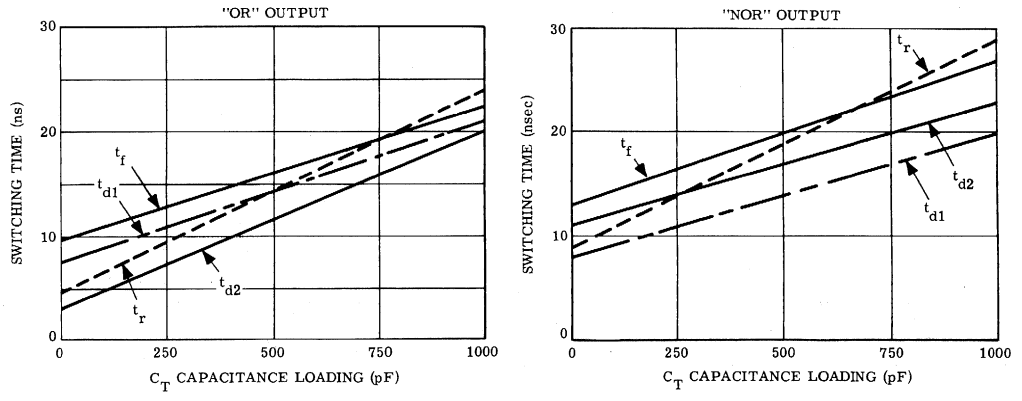


FIGURE F — SWITCHING CHARACTERISTICS OF MC315, MC365

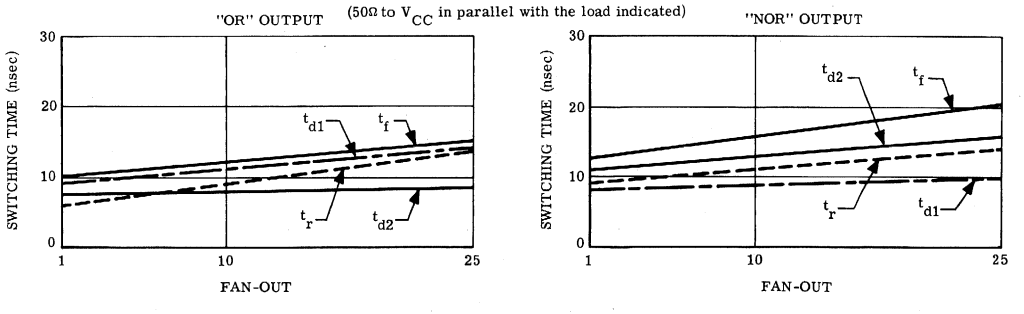
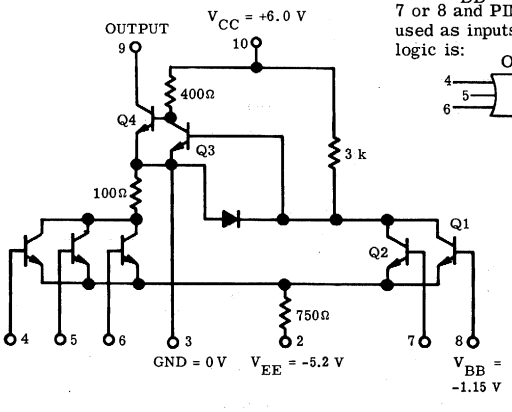
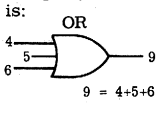


FIGURE G — TYPICAL SWITCHING CHARACTERISTICS OF MC315, MC365

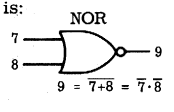
LAMP DRIVER: MC316, MC366



When V_{BB} is applied to PINS 7 or 8 and PINS 4, 5 and 6 are used as inputs; the resultant logic is:



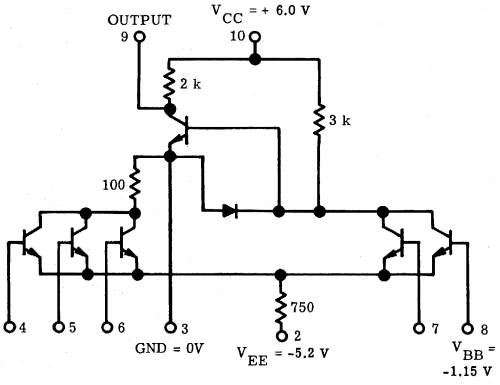
When V_{BB} is applied to PINS 4, 5 or 6, and PINS 7 and 8 are used as inputs; the resultant logic is:



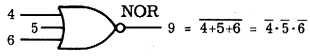
The Lamp Driver operation is the same as that of a regular gate except for the output circuitry which presents saturated logic levels. The current through the 3 k resistor is either switched through the base of Q_3 or transistors Q_1 and Q_2. Q_4, the output transistor, may then be used to turn an indicator light on or off. The diode becomes useful if the gate is to be used as a high speed switch by preventing saturation of Q_1 and Q_2.

Q_4 will sink a maximum of 100 mA at 25°C and 50 mA at 125°C. The maximum V_{sat} is 1.0 V at 100 mA. Typical V_{sat} is 0.75 V at 100 mA with a V_{CC} of 4 V to 6 V. Maximum power dissipation is 235 mW at 6 V and 100 mA sink current.

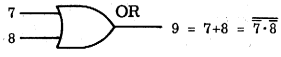
LEVEL TRANSLATOR MECL TO DTL: MC317, MC367



When V_{BB} is applied to PINS 7 or 8, and PINS 4, 5 and 6 are used as inputs; the resultant logic is:



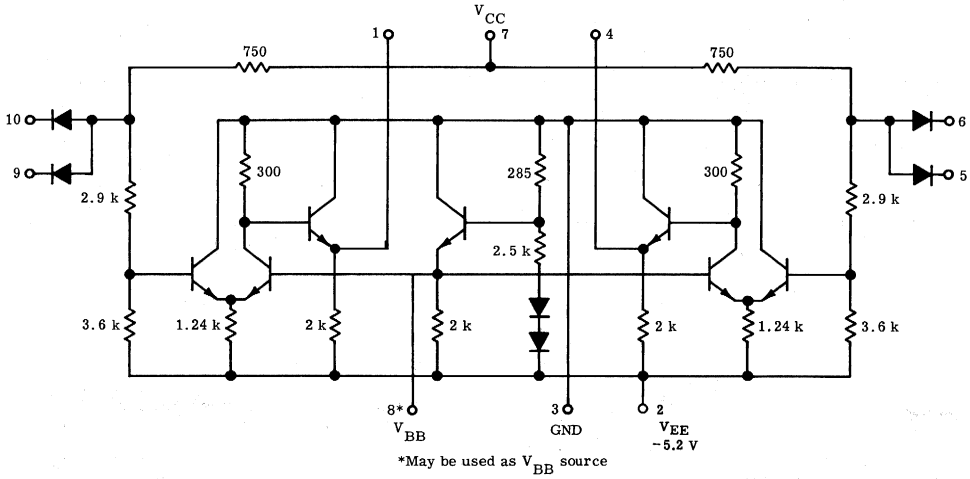
When V_{BB} is applied to PINS 4, 5 or 6, and PINS 7 and 8 are used as inputs; the resultant logic is:



The primary function of this gate is to act as a high speed interface between MECL logic levels and those of saturated logic. Operation is identical to that of the MC316, MC366 Lamp Driver except for the elimination of the output driver transistor.

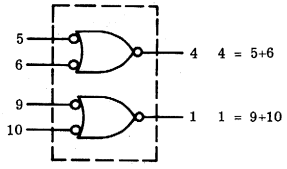
Maximum saturation voltage of 0.45 V at 25°C is specified for a sink current of 10 mA, while typical V_{sat} is 0.25 V. The output voltage at no load is essentially V_{CC}. Turn on and turn off times are a maximum of 30 ns and 35 ns respectively while worst case power dissipation is 75 mW over the full temperature range.

LEVEL TRANSLATOR DTL TO MECL: MC318, MC368



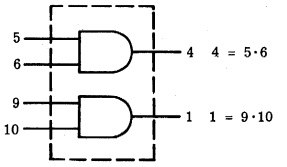
*May be used as V_{BB} source

NEGATIVE LOGIC



LOGIC SPECIFICATION
By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at -1.55 V and logical "1" at -0.75 V.

POSITIVE LOGIC

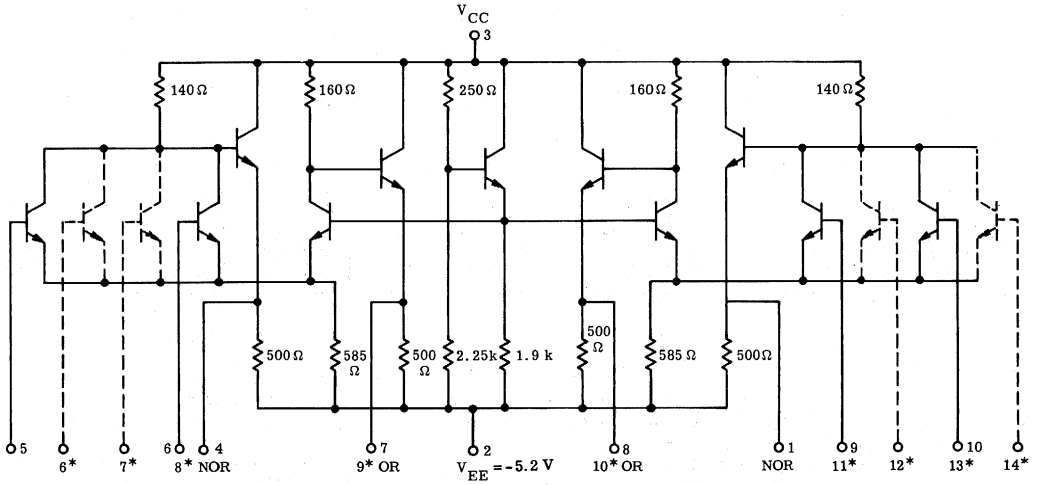


Continued

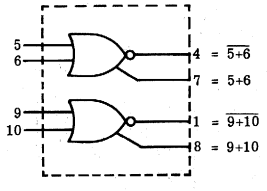
This device is used wherever a high-speed level translator from saturated logic to MECL is required. Turn on and turn off times are about 15 ns with output rise time and fall time nominally 7.5 ns. Maximum power dissipation is 120 mW over the temperature range. The saturated logic input levels should switch from about +0.5 V to + 5.0 or + 6.0 V for the above specifications.

The dual translator operation is as follows: If inputs 5 and 6 are high, the logic input of the respective MECL gate receives a high level through the voltage divider. The OR output of the first MECL gate on pin 4 will then go high. The second translator functions in the same manner for inputs on pins 9 and 10 and an output on pin 1. The device contains a built-in bias driver that compensates for voltage and temperature variations. This reference voltage is available to drive additional gates. A maximum fan-out of 23 is available. Both translators perform the positive AND logic function.

MC369G DUAL-2 OR, NOR CLOCK DRIVER AND HIGH-SPEED GATE
MC369F DUAL-4 OR, NOR CLOCK DRIVER AND HIGH-SPEED GATE

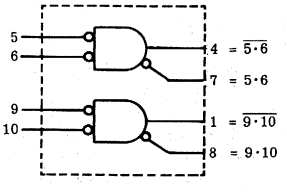


POSITIVE LOGIC
V_H is defined as logical "1", V_L as logical "0".



MD369G

NEGATIVE LOGIC
V_H is defined as logical "0", V_L as logical "1".



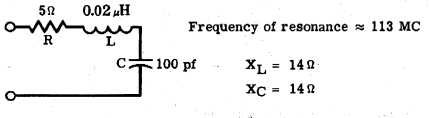
MD369F

The Clock Driver is a very low output impedance device (about 5Ω) and exhibits very fast rise and fall times. Because of its low output impedance and fast rise times, precautions must be taken to reduce ringing in circuits employing the device. The device will fan-out to one or two flip flops ($\overline{J}$ and $\overline{K}$ tied together) with a typical rise time of less than 4 ns. Also, a fan-out to 20 flip flops may be achieved with typical rise times of less than 9 ns.

Operation of the gate is the same as a standard MECL gate with the exception of lower resistance values and higher power dissipation. Typical characteristics at a fan-out of 10 MECL gate loads are: rise time 4.0 ns, fall time 5.0 ns, propagation delay time 5 ns, and power dissipation 240 mW.

Continued

Considering that in a clock driver application, a flip flop may be inhibited with a minimum "1" level and that overshoot may appear on a maximum "1" level clock, worst case allowable overshoot is only 100 mV over the temperature range. For room temperature applications overshoot should be limited to 150 mV. If a lumped capacitance load is added to the clock driver output, overshoot and ringing will be noted. The following is a simplified equivalent circuit for the clock driver output where: R = incremental output impedance of the emitter follower. L = the inductance of 1" of wire. C = the capacitance of 10 flip flop inputs with $\overline{J}$ and $\overline{K}$ tied together.



This represents an underdamped series R-L-C circuit and overshoot will be a problem when a step function is applied to the input of the circuit. The following method has been found satisfactory for reducing overshoot to 100 mV or less: (1) Keep the output lead of the device as short as possible, (2) Tap off from the output lead with a resistor of appropriate value to each input being clocked, (3) Keep all devices being clocked as close as possible to the clock driver, (4) If overshoot is still a problem, it may be reduced by 30% to 50% by paralleling two outputs, i.e. two OR's or two NOR's from the same can. This reduces by half the current flowing through an output lead.

The following data in the table are given as a guideline for selecting the proper resistor to be used in series with each flip flop input. Power supplies were bipassed to ground and all loading flip flops were kept within 3 inches of the clock driver.

TABLE OF OVERSHOOT AND RISE-TIME

VS. RESISTANCE AND FAN-OUT

FO = 1 R = 0Ω

S		P	
OS	t_r	OS	t_r
50 mV	3.4 ns	25 mV	3.4 ns

FO = 2 R = 0Ω

S		P	
OS	t_r	OS	t_r
115 mV	3.4 ns	70 mV	3.4 ns

FO = 3 R = 0Ω

S		P	
OS	t_r	OS	t_r
175 mV	3.5 ns	105 mV	3.4 ns

FO = 5 R = 200Ω

S		P	
OS	t_r	OS	t_r
120 mV	5.5 ns	95 mV	5.5 ns

FO = 10 R = 200Ω

S		P	
OS	t_r	OS	t_r
180 mV	5.9 ns	140 mV	5.6 ns

FO = 10 R = 330Ω

S		P	
OS	t_r	OS	t_r
100 mV	7.1 ns	75 mV	6.9 ns

FO = 15 R = 330Ω

S		P	
OS	t_r	OS	t_r
135 mV	7.3 ns	100 mV	7.1 ns

FO = 10 R = 470Ω

S		P	
OS	t_r	OS	t_r
50 mV	8.4 ns	40 mV	8.4 ns

FO = 20 R = 470Ω

S		P	
OS	t_r	OS	t_r
100 mV	8.6 ns	70 mV	8.3 ns

FO = fan-out of clocked flip-flops

S = single gate output

P = paralleled gate outputs (from same can)

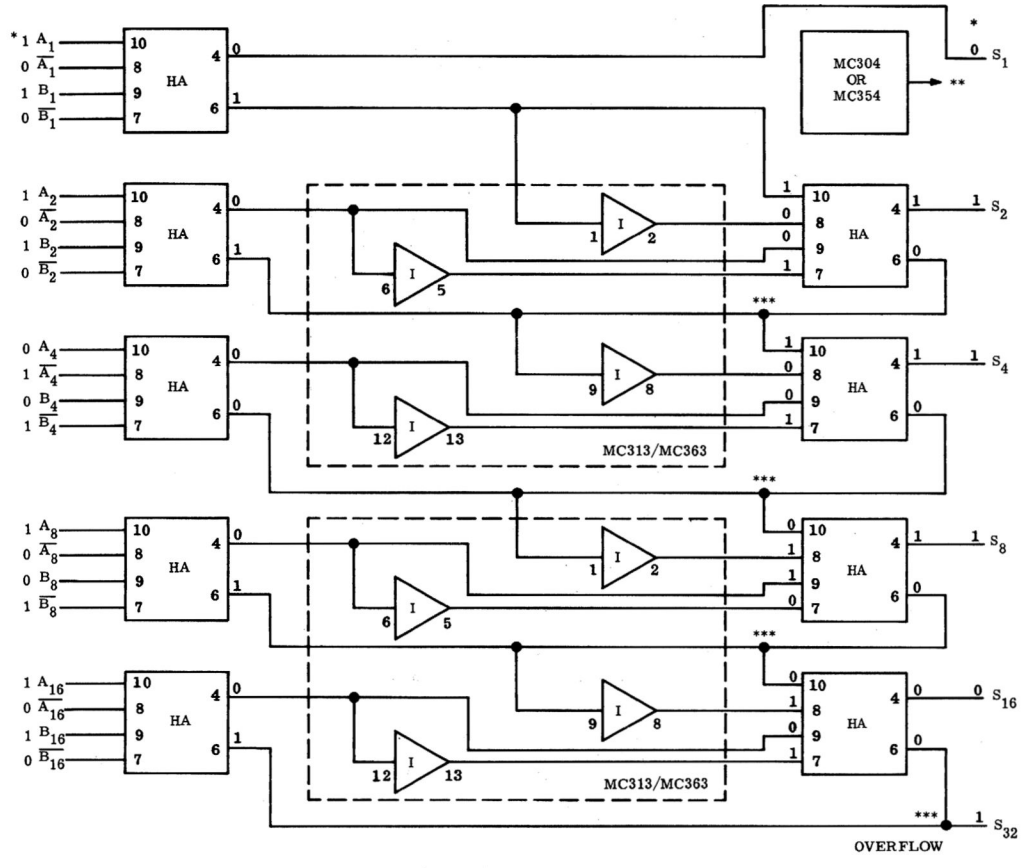
OS = overshoot in millivolts

t_r = rise-time in nanoseconds at input to a flip-flop

MECL SYSTEM APPLICATIONS

This section of sample applications of MECL is included to illustrate the use and versatility of this family. Note the short propagation times obtained. Also additional gates are saved by using the wired-OR feature of MECL.

MECL ASYNCHRONOUS PARALLEL FIVE BIT ADDER



The table illustrates the addition of two 5 bit binary numbers. The subscripts give the decimal equivalent weights of the binary bits. Logic levels for the example are shown in the logic diagram.

TYPICAL EXAMPLE

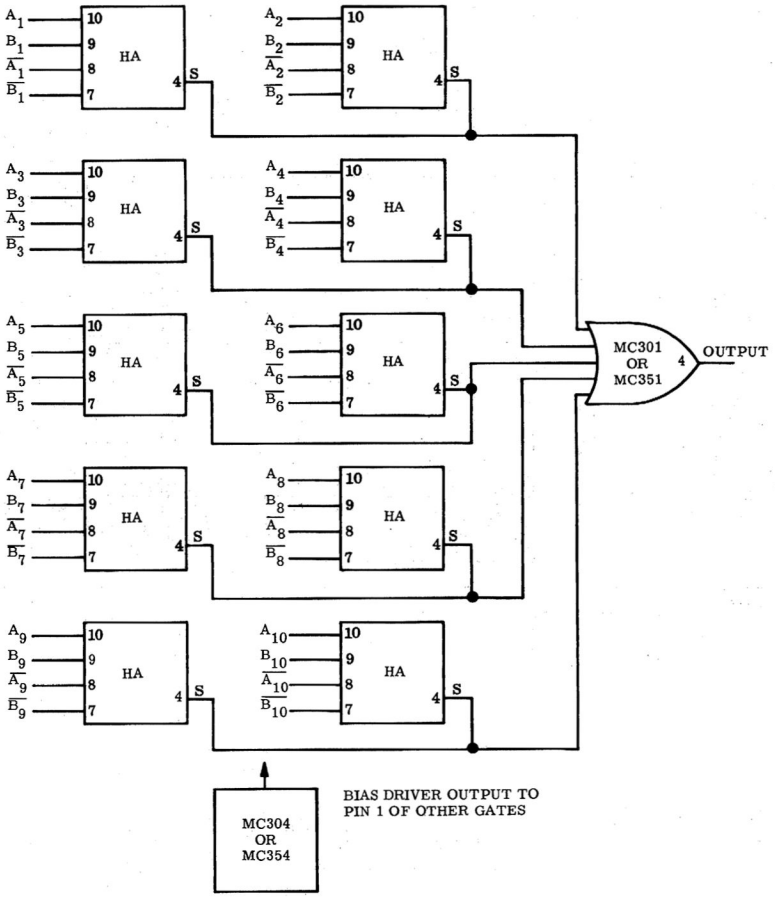
"A" AUGEND		"B" ADDEND		"S" SUM		"C" CARRY	
A_1	1	B_1	1	S_1	0	C_1	1
A_2	1	B_2	1	S_2	1	C_2	1
A_4	0	B_4	0	S_4	1	C_4	0
A_8	1	B_8	0	S_8	1	C_8	0
A_{16}	1	B_{16}	1	S_{16}	0	C_{16}	1

DEFINITIONS:
HA = Half Adder MC303 or MC353. A logical "1" is defined as a relatively high level (-.75 V). A logical "0" is defined as a relatively low level (-1.55 V).

NOTE: The inverters are obtained from 2-quad two-input gates. If desired, 4-dual two-input gates may be used instead of the 14-pin MC313/MC363.
"Can Count" = 9 Half Adders, 2 Quad 2-input gates, 1 Bias Driver = 12 "cans".
The 5-bit adder requires 9 gate delays for a carry to ripple through from the first Half Adder to the overflow output. The total propagation delay time is approximately 60 ns.

*Logic Levels are for the example shown in the table.
**The Bias Driver connects to each gate requiring external bias.
***Outputs are wire OR'd together.

ASYNCHRONOUS 10-BIT MECL COMPARATOR
(Employing the HALF-ADDER as an exclusive OR)



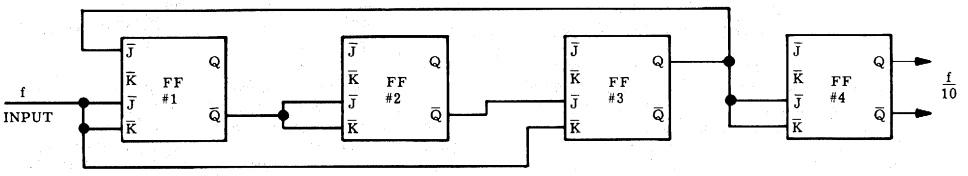
HALF ADDER Truth Table

Pin #	10	9	8	7	4
	A	B	$\overline{A}$	$\overline{B}$	OUT
	Lo	Lo	Hi	Hi	Lo
	Lo	Hi	Hi	Lo	Hi
	Hi	Lo	Lo	Hi	Hi
	Hi	Hi	Lo	Lo	Lo

This circuit employing only 12 devices indicates asynchronously whether or not the data from two sources (A and B) agree. If any one of the Half Adder gates (HA) has a pair of input bits that are different, the gate will have a high level output. The Half Adders are wire-OR'd together two at a time resulting in five outputs which drive a 5-input OR gate. The circuit output will be high if any datum from source A disagrees with the corresponding datum from source B.

The circuit has many uses such as enabling the step counting of a register until its output agrees with a given input. Total propagation delay time from input to output is approximately 15 ns. This high speed is an important asset in fast analog to digital conversion. As many bits as desired may be compared with similar propagation delay time by wire OR'ing the output of another 5-input OR with the one shown or by using an expandable gate instead of an MC301 or MC-351.

MECL ÷ 10 COUNTER

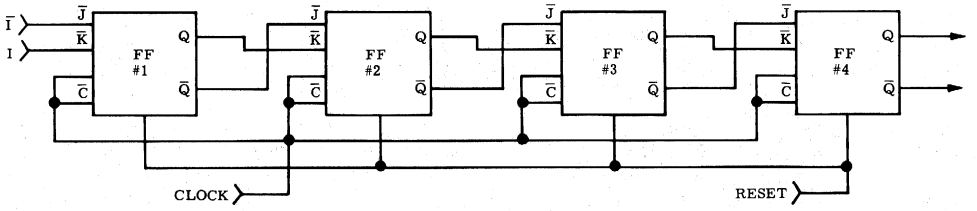


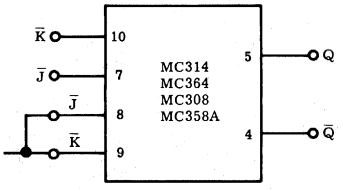
STATE #	FF #1	FF #2	FF #3	FF #4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	1
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	0
10	0	0	0	0

NOTE:
1. A positive going $\overline{J}$, all other inputs to FF low, sets FF to "1".
2. A positive going $\overline{K}$, all other inputs to FF low, sets FF to "0".
3. In going from state 4 to 5, the "1" from FF 3 is fed back to the $\overline{J}$ input of FF 1 while the clock waveform is still high and inhibiting the flip flop. If the up-time of the clock is too short, the $\overline{J}$ input may set FF 1 to the "1" state causing an error.
4. FF 2 and 4 are connected in the toggle mode and simply divide by two.

The main advantage of MECL counters (besides speed), is that any desired count may be obtained without additional gates. The maximum input frequency (f) of the configuration shown is about 15 MHz, without selection of units. If MC314, MC364 flip flops are used and FF 4 is put first in the chain (yielding f/2); inputs of 30 MHz may be employed. The output in the second case is not symmetrical which may be a disadvantage. Further information on counters both clocked and asynchronous may be found in AN-194 and AN-257.

MECL 4-BIT SHIFT REGISTER





CLOCKED JK OPERATION

FLIP FLOP Truth Table

INPUT STATE	$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
	ø	ø	0	Q^n
1	0	0	1	$\overline{Q^n}$
2	0	1	1	1
3	1	0	1	0
4	1	1	1	Q^n

continued

Information received in a shift register will normally be of input state 2 or 3 as shown in the truth table, i.e. inputs of opposite levels. It is seen from the table that the level of the $\overline{K}$ input will be stored in the flip flop, after a dynamic clock, and appear at the Q output. After the first flip flop in the shift register, changes state, the $\overline{J}$ and $\overline{K}$ inputs of the second receive their data. Since the "up time" of a clock waveform is longer than the propagation delay time of a flip flop, a following flip flop is inhibited while the $\overline{J}$ and $\overline{K}$ inputs may be changing levels. Since propagation delay is of no importance, it appears that the maximum shift frequency is the same as the maximum toggle frequency. This is almost true with one exception: If the zero level from the previous flip flop into the $\overline{J}$ or $\overline{K}$ input is more positive than the zero level of the clocking waveform, then a small portion of the clock waveform will be inhibited. This reduces the effective amplitude of the clock. (Note the schematic of one of the flip flops shown previously.) Since maximum toggle frequency depends upon clock amplitude, a reduction in typical operating speed for a given flip flop may be seen. For good clock waveforms and amplitudes, shift frequency is essentially the same as minimum guaranteed toggle frequency.

The Reset input may be used to set every stage to zero if desired, or a combination of Set and Reset inputs may be used to obtain a given count prior to shifting. If the D.C. Set or Reset input is at a high level when the clock also goes high, an undesirable voltage spike will be transmitted to the flip flop output. Therefore, a flip flop should only be Set or Reset at other than clocking time, preferrably when the clock is high.

Another application of the shift register is that of a digital delay. A bit delay of n clock pulses may be obtained between the input and output of a shift register containing n flip flops. Also the output of a shift register may be fed back to the input to form a ring counter. One bit may be inserted in a ring counter and recirculated to form a simple bit time generator for clocking computer decisions.

MECL 70 MHz J-K FLIP-FLOP

INTRODUCTION

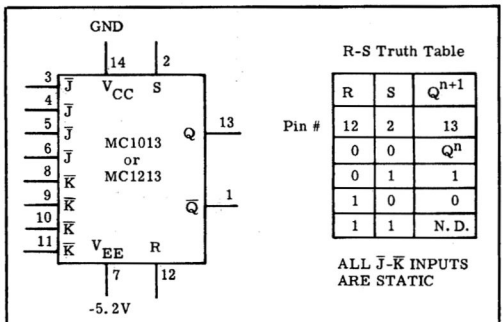
This note presents a thorough characterization of the MC1013/MC1213 $\overline{J}$-$\overline{K}$ flip-flop, which is a member of the new High Speed MECL II family. Both typical and worst case data for system design are given. The flip-flop is versatile in logic designs since four $\overline{J}$ and $\overline{K}$ inputs are provided. The typical operating speed of 85 MHz permits many high speed applications that were only possible with discrete components.

Figure 1 presents the truth tables and pin layouts for the flip-flop. The device is available in the dual in-line 14-pin plastic package (0°C to 75°C) and the 1/4" X 1/4" 14-pin ceramic flat package (-55°C to 125°C). Figure 2 is the device schematic with nominal resistor values. Circuit operation is the same as explained in AN-244 for the MC314/MC364 flip-flop.

The desired input levels are those of a standard MECL gate (see AN-244) i.e., a nominal voltage swing of 800 mV from -.75V to -1.55V at 25°C. Since capacitive coupling is internally employed, the device will accept large variations from the nominal values. In fact, 10 to 20 MHz may be added to the typical toggle frequency at 25°C by "overdriving" the clocked or toggle input with a 1.2V signal between the levels of about -0.4V and -1.6V and keeping the rise and fall times to 2 ns or less.

Figure 3 is the recommended circuit for driving the flip-flop from a pulse generator. For optimum performance, the lead length into and out of the 2N3959 must be kept short to prevent excessive overshoot. The 2N3959 is a 1.8 GHz device and gives good performance down to 1 ns rise and fall times. Output impedance is less than 20 Ω. This circuit closely approximates the output of the MC1023 clock driver which will be available in the first quarter of 1967. The MC1023 exhibits a typical rise time of 2.0 ns and fall time of 3.0 ns at a fanout of 10 (5 $\overline{J}$-$\overline{K}$ pairs) where lead lengths are kept to one inch or less. Each $\overline{J}$-$\overline{K}$ pair should have a separate input lead to the clock driver output if point to point wiring is used.

Other devices in the MECL family will also drive the MC1013/MC1213 satisfactorily at slower risetimes, resulting in slightly lower operating frequencies. The MC369G, MC1050, MC1051, MC1052, all exhibit typical risetimes of 4.0 ns and fall times of 5 ns at a fanout of 5 clocked flip-flops. The flip-flop itself makes a satisfactory driver with a typical output impedance of 15 Ω, risetime of 4 ns, and fall time of 5 ns at a small fanout.



R-S Truth Table

Pin #	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

ALL $\overline{J}$-$\overline{K}$ INPUTS ARE STATIC

Clocked $\overline{J}$-$\overline{K}$ Truth Table

Pin #	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	-	1	1	1
	1	0	1	0
	1	1	1	Q^n

ALL OTHER $\overline{J}$-$\overline{K}$ INPUTS AND THE R-S INPUTS ARE AT A "0" LEVEL

$\overline{J}_D$-$\overline{K}_D$ Truth Table

Pin #	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

ALL OTHER $\overline{J}$-$\overline{K}$ INPUTS AND THE R-S INPUTS ARE AT A "0" LEVEL

NOTES

1. N.D. stands for NOT DEFINED
2. *Any one of the $\overline{J}$ or $\overline{K}$ inputs may be used.
3. **Any $\overline{J}$ and $\overline{K}$ inputs may be tied together to form C_D eg. pins 6 and 8
4. -0.75V nominal is defined as a logic "1" or high level and -1.55V nominal is defined as a logic "0" or low level. $\overline{J}$ and $\overline{K}$ refer to static levels while $\overline{J}_D$, $\overline{K}_D$, C_D refer to dynamic positive-going transitions for a "1".
   A high level on a $\overline{J}$ input inhibits the flip-flop from being set by a $\overline{J}_D$ input. Likewise a "1" level on a $\overline{K}$ inhibits a $\overline{K}_D$ from resetting the flip-flop. The $\overline{J}$ and $\overline{K}$ inputs perform the "OR" function in preventing a $\overline{J}_D$ or $\overline{K}_D$ from setting or resetting the flip-flop.

FIGURE 1 — MECL II J-K FLIP FLOP LOGIC DIAGRAM AND TRUTH TABLES

MC1013/MC1213 CHARACTERISTICS

The following curves are most useful in describing the various parameters of the flip-flop under different operating conditions. The worst case data shown is conservative and may be used for system design purposes. If good system layout techniques are employed, the worst case system data observed will be better than that shown in the graphs. Poor system layout such as long inductive leads, high lumped values of capacitance, and unnecessarily large fanouts can reduce the typical operating speed considerably below 70 MHz.

Figure 4 illustrates the typical and worst case toggle frequency (or divide-by-two parameter) of the flip-flop. The guaranteed minimum toggle frequency of 70 MHz at 25 C is internally guard-banded by the manufacturer to prevent correlation problems with the customer. The toggle test is run with the circuit shown in Figure 3 with 800 mV input amplitude, less than 2.0 ns rise and fall times and a duty cycle of 50%. This test also assures a minimum allowed down and up time of 7.0 ns for the clocking waveform at 25°C (measured at the 50% levels). The worst case down or up time over the full temperature range is 9.0 ns. This corresponds to a worst case toggle frequency of 55 MHz at 125°C. The loading on the flip-flop has a negligible effect upon toggle frequency due to the emitter followers that isolate the flip-flop from the load. With the test input as stated above, a small percentage of the devices will toggle at 100 MHz. Slower rise and fall times will reduce this maximum frequency of operation. It should be noted that

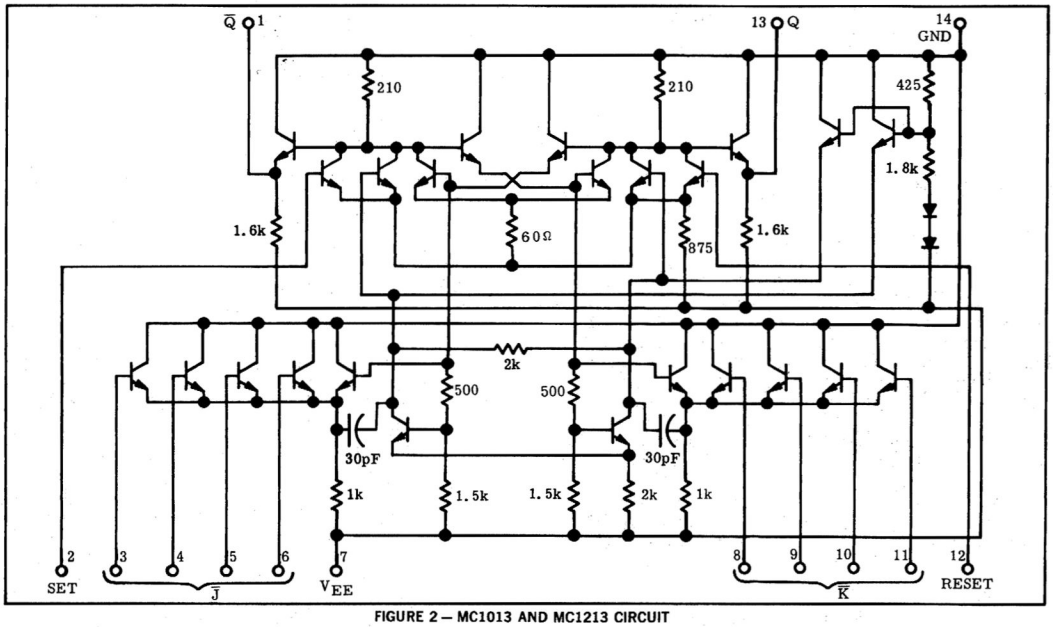


FIGURE 2 — MC1013 AND MC1213 CIRCUIT

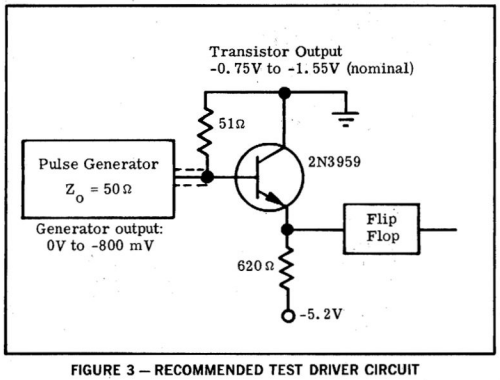


FIGURE 3 — RECOMMENDED TEST DRIVER CIRCUIT

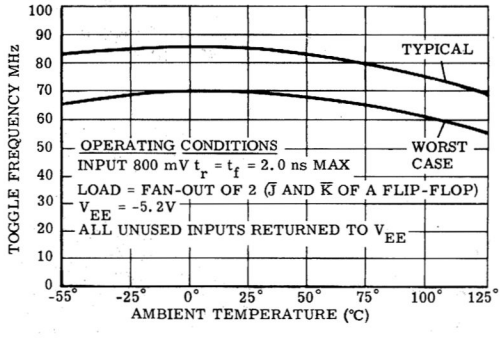


FIGURE 4 — TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

a gate with 4 ns rise and fall times can do no better than a sine wave at 90 MHz.

The typical toggle frequency vs. V_{EE} curve, shown in Figure 5, illustrates the versatility of the MECL design that exhibits common mode rejection of V_{EE} supply variations. Toggle frequency changes very little for ±20% variations in supply voltage. The flip-flop appears as a nominal 215Ω resistive load to the power supply. Therefore, power dissipation is proportional to the square of V_{EE}. At a V_{EE} of -4V, power dissipation drops to a nominal 75 mW. At least 90% of the flip-flops will drive another device with V_{EE} varying from -3.0V to -8V at 25°C.

The minimum input amplitude required to toggle or clock the flip-flop at a given rise time is an important parameter. This measure of sensitivity varies with input rise time as shown in Figure 6. All flip-flops exhibit a slope of about 7.3 mV per ns as is shown for the typical flip-flop. The maximum variation in slope is ±20% which permits worst case design points to be guaranteed by the specification points shown in Figure 6. The worst case limit lines (for least sensitive devices and most sensitive devices) are obtained by changing the slope from that of the nominal flip-flop and leaving a guard-band that insures validity over the full temperature range. (See Figure 13 "Typical Sensitivity Variation VS. Temperature"). The specification points, tested on 100% of the devices, are: the flip-flop must not toggle on 300 mV input at 5.0 ns rise time and the flip-flop must toggle at 600 mV input at 20 ns rise time. These points are guard-banded to prevent any correlation problems. The worst case design points are: An input of 800 mV and greater than 100 ns rise time will not toggle the flip-flop. An input of 800 mV and less than 40 ns rise time will toggle the flip-flop. An input of 250 mV will not toggle the flip-flop, even at 0 ns rise time. These worst case values hold for the full temperature range of -55°C to 125°C.

Figure 7 illustrates typical and worst case propagation delay, rise, and fall times for a fanout of one clocked flip-flop (J and K tied together). The worst case curves are conservative and, therefore, recommended for system design at a fanout of two. t_{pd+-} stands for the propagation delay through the flip-flop from 50% of the positive going clock input to 50% of the negative going output. t_{pd++} is measured from 50% of the positive going clock input to 50% of a positive going output. All clock inputs and outputs are symmetrical and the results are the same regardless of which inputs or outputs are used in the measurements.

The typical and worst case delay, rise, and fall times vs. fanout of MC1000/MC1200 series gates are given in Figure 8. The MECL II gates exhibit less input capacitance than the MC300/MC350 series of MECL. Worst case data for 0°C and -55°C should be taken as the same as that shown for 25°C. Typically these values are slightly better than those shown at 25°C.

The minimum time to toggle after the flip-flop has been set or reset is shown in Figure 9. Worst case data are: width of the set/reset pulse 6 ns minimum, width of the $\overline{K}/\overline{J}$ pulse 8 ns minimum, and the minimum spacing is 8 ns between the falling edge of the set/reset pulse and the rising edge of the $\overline{K}/\overline{J}$ pulse. Times are measured from the 50% portions of all waveforms.

Figure 10 illustrates the minimum required time to reset/set after a $\overline{J}/\overline{K}$ input has been received. This figure indicates the internal time constants of the flip-flop. Under worst case conditions the flip-flop will reset/set with a minimum pulse width of 10 ns, if the pulse is received 11 ns or more after the $\overline{J}/\overline{K}$ input. The worst case times are approximately 1 ns longer than the worst case propagation delay times (Figure 7).

If the $\overline{J}$-$\overline{K}$ inputs to a flip-flop are spaced far enough apart in time, they will act as set-reset inputs (all other inputs at a low level). While if they are brought close enough together, they will act as a toggle input to the flip-flop. Figure 11 illustrates the minimum required time to insure that the $\overline{K}$ input dominates after a $\overline{J}$ input. If the inputs are closer together (time-wise) than that shown for worst case, the flip-flop may toggle. Time to dominate may go as low as 2.0 ns at -55°C for some devices. Therefore, it is recommended that when it is desired to toggle a device, that the particular $\overline{J}$-$\overline{K}$ inputs be wired together rather than be fed through separate gates.

The "Power Dissipation vs. Temperature" curve (Figure 12) is primarily a measure of the device effective resistance over the temperature range. The worst case values are given for a single device, but values for worst case system design may be moved closer to the typical curve if desired. This is due to the averaging effect of multiple devices. Typically power dissipation changes less than 3 mW from D.C. to the maximum operating frequency of a given device. An unloaded flip-flop actually shows a decrease in power dissipation of about 2 mW from D.C. to above 70 MHz.

The sensitivity variation of a flip-flop (minimum input amplitude to toggle) vs. temperature is almost lost in measurement uncertainties. Typically, variations are well within ±10% which is insignificant in a system. Figure 13 illustrates that the typical device is more sensitive at -55°C than at 125°C. The sensitivity tracks very well with typical output amplitude vs. temperature which is shown in Figure 14.

The sensitivity of a flip-flop changes with supply voltage (V_{EE}) as does the output amplitude. Figures 15 and 16 illustrate the tracking capabilities of sensitivity and output amplitude vs. V_{EE}. It is seen that tracking is very good for ±30% variations in V_{EE}. The higher sensitivity at reduced V_{EE} suggests using the device as an RF amplifier, which also divides the input frequency by two. The effective gain through the flip-flop is typically greater than 2.5 at V_{CC} = -4.0 V.

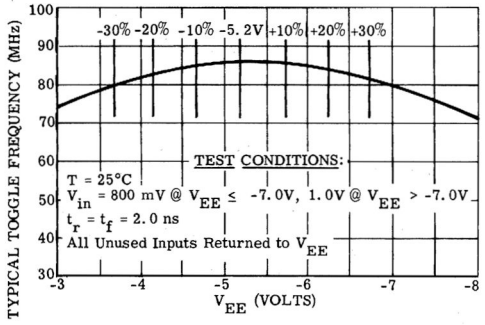


FIGURE 5 — TYPICAL TOGGLE FREQUENCY versus V_{EE}

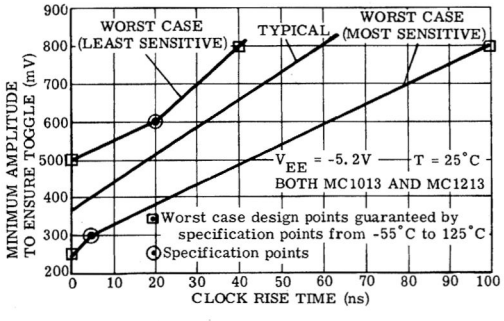
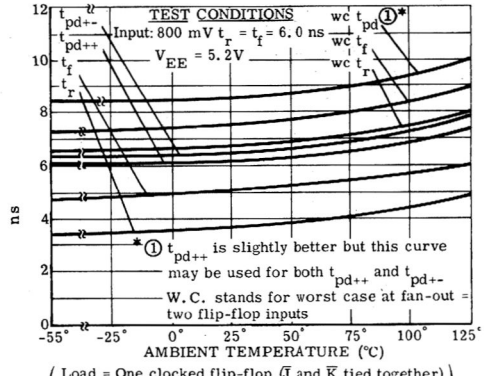


FIGURE 6 — AMPLITUDE versus RISE TIME TO INSURE TOGGLE

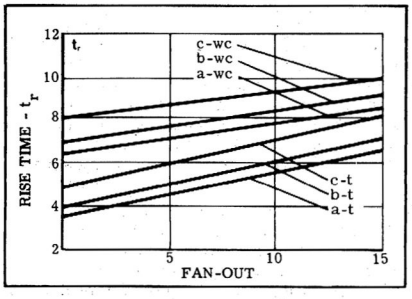
ADDITIONAL FLIP-FLOP CHARACTERISTICS

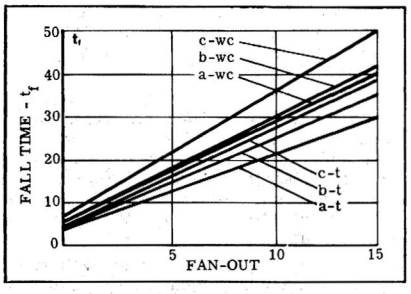
The flip-flop may be set and reset at a rate in excess of 100 MHz. The optimum pulses in this mode of operation are from 4 to 5 ns in width with rise and fall times of less than 2 ns. The MC1013/MC1213 flip-flop exhibits a tighter distribution of parameters than devices in the MC300/MC350 Series. 90% of the devices exhibit less than ±20% variations in propagation delay, rise, and fall times. Also, the maximum toggle frequency varies

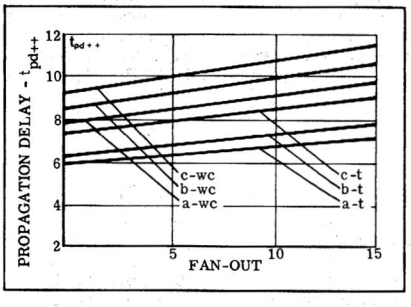


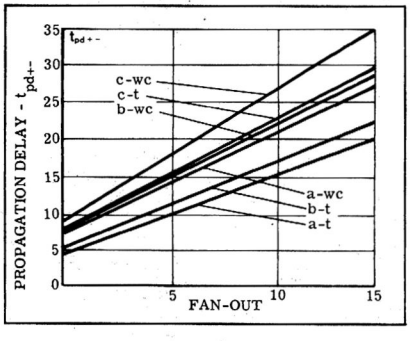
(Load = One clocked flip-flop ($\overline{J}$ and $\overline{K}$ tied together)
All unused inputs are returned to -5.2V)

FIGURE 7 — PROGAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE









INPUT t_r = 5.0 ns — A = 25°C

INPUT AMPLITUDE 800 mV — B = 75°C

V_{EE} = -5.2V — C = 125°C

T = TYPICAL — WC = WORST CASE

FIGURE 8 — PROPAGATION DELAYS, RISE TIME, FALL TIME versus FAN-OUT AND TEMPERATURE

only about ±15% from the nominal value of 85 MHz. Each $\overline{J}$ and $\overline{K}$ input should be considered as a load of one, making a clocked input equivalent to a load of two. The maximum recommended fanout for the flip-flop is 15, above which, fall times become excessive. At low operating frequencies, fanout may be greatly increased if waveform deterioriation is considered in the design. The device has a guaranteed D.C. fanout of 25 which corresponds to a worst case of 2.5 mA load current. The maximum output current that should be drawn from the flip-flop is 10 mA which will decrease the nominal "1" level at no load by about 150 to 200 mV. If the flip-flop is used to drive a gate, the "1" level noise immunity is reduced to about 50 mV under these conditions. At large fanouts, fall time and t_{pd+-} will be decreased if an additional resistor is wired between the output and V_{EE}.

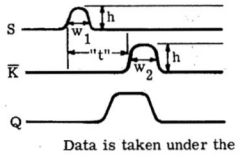
It should be noted that if a DC set or reset input is at a "1" level and the $\overline{J}$-$\overline{K}$ inputs are clocked, that a "glitch" will appear on the outputs. This glitch may be of sufficient amplitude to toggle or clock another flip-flop tied to the Q or $\overline{Q}$ output. This condition is the same as applying both a set and reset input to a current mode R-S flip-flop where both outputs tend to go to a V_{BB} level (half-way between "1" and "0"). This glitch may be minimized by a clock of low amplitude and slow rise time, but good system design eliminates this situation.

The worst case shift frequency depends upon the slowest flip-flop in the shift register. For a shift register without gating, the worst case shift frequency is essentially the same as the worst case toggle frequency of the slowest flip-flop employed in the register. Therefore, the worst case shift frequency is 70 MHz at 25°C and 55 MHz at 125°C.

This flip-flop is most useful in high frequency counters, phase locked loops, frequency synthesizers, special counters, logic designs that require additional $\overline{J}$ and $\overline{K}$ inputs, and high speed registers in the arithmetic portion of digital computers.

SUMMARY

The MC1013/MC1213 flip-flop is a versatile high frequency device that more than doubles the maximum operating frequency of a MECL system. The worst case data given in this note are conservative and, therefore, intended for system design. Due to the high frequencies of operation, performance depends heavily upon system layout. This MECL flip-flop will work best when used with multilayer printed circuit cards where lead lengths have been minimized. This flip-flop is characteristic of MECL II devices which operate in the 5 ns region with typical system loads.



w_1 = 4 ns (optimum)

w_2 = 6 ns (optimum)

h = 800 mV

Data is taken under the following conditions:

S and $\overline{K}$ inputs: $t_r = t_f$ = 1.5 ns

V_{EE} = -5.2V

t = min of 7-10 ns, "t" - w_1 = 3-6 ns min @ 25°C

Worst Case Operation -55°C to 125°C

w_1 = 6 ns min w_2 = 8 ns min "t"-w_1 = 8 ns min

FIGURE 9 — MINIMUM TIME TO TOGGLE AFTER SET OR RESET

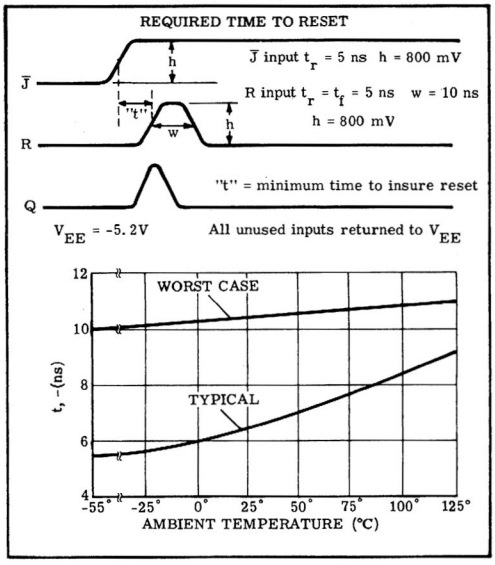


FIGURE 10 — REQUIRED TIME TO RESET

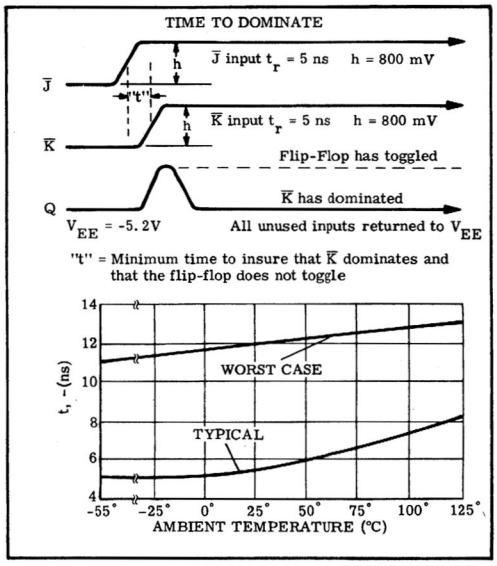


FIGURE 11 — TIME TO DOMINATE

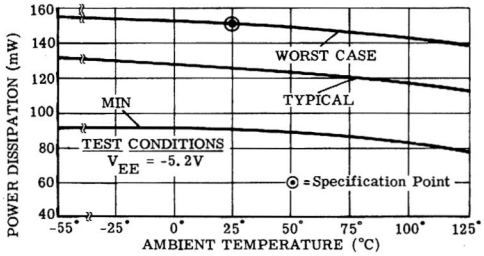


FIGURE 12 — POWER DISSIPATION versus TEMPERATURE

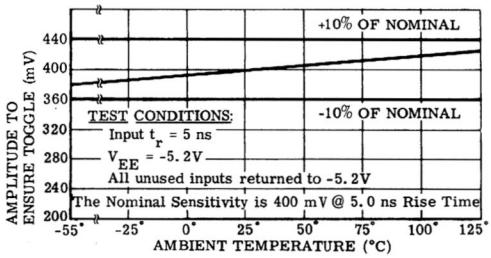


FIGURE 13 — TYPICAL SENSITIVITY VARIATION versus TEMPERATURE

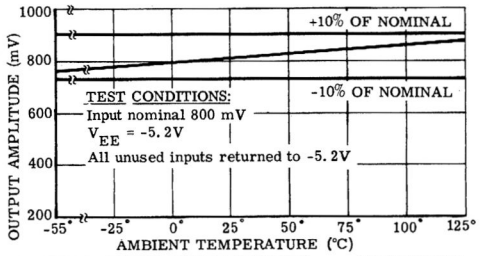


FIGURE 14 — TYPICAL OUTPUT AMPLITUDE versus TEMPERATURE

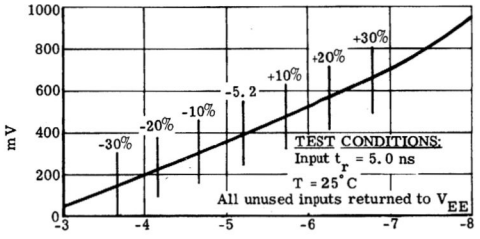


FIGURE 15 — TYPICAL SENSITIVITY TO TOGGLE versus V_{EE}

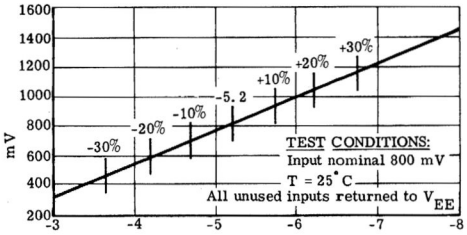


FIGURE 16 — TYPICAL OUTPUT AMPLITUDE versus V_{EE}

USING SHIFT REGISTERS AS PULSE DELAY NETWORKS

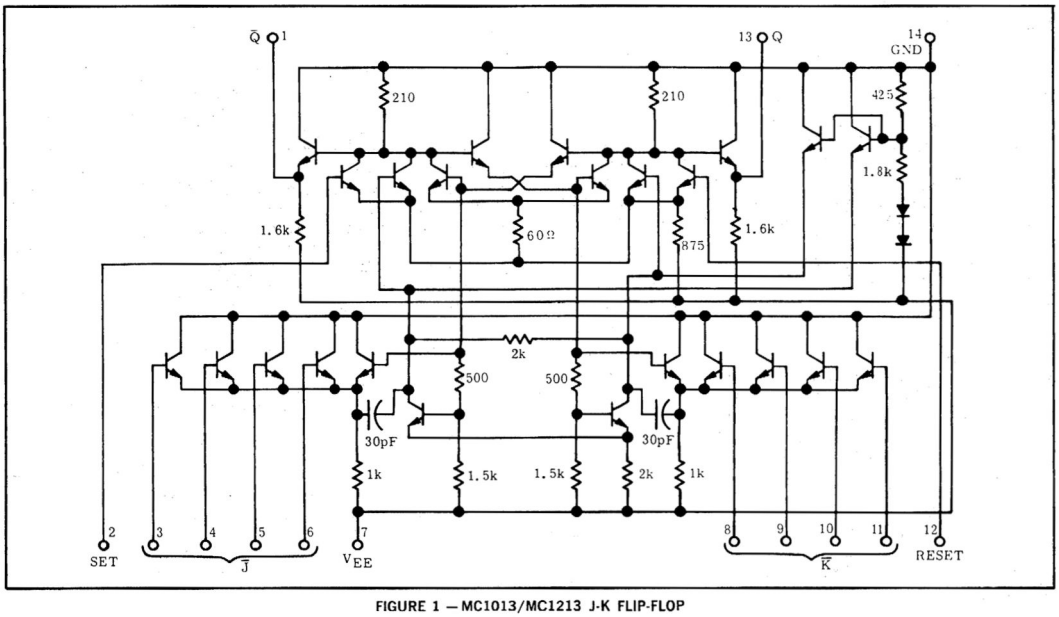
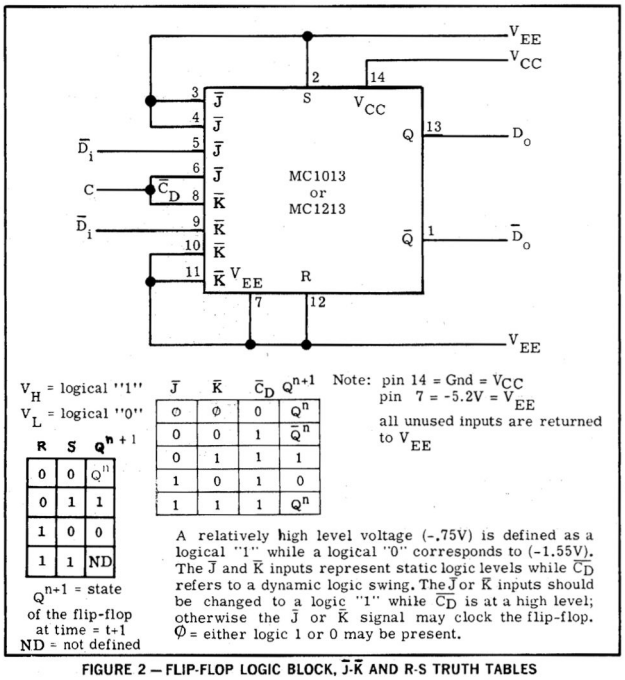


FIGURE 1 — MC1013/MC1213 J-K FLIP-FLOP



V_H = logical "1"
V_L = logical "0"

R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	ND

Q^{n+1} = state of the flip-flop at time = t+1
ND = not defined

$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^{n+1}
Ø	Ø	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

Note: pin 14 = Gnd = V_{CC}
pin 7 = -5.2V = V_{EE}
all unused inputs are returned to V_{EE}

A relatively high level voltage (-.75V) is defined as a logical "1" while a logical "0" corresponds to (-1.55V). The $\overline{J}$ and $\overline{K}$ inputs represent static logic levels while $\overline{C}_D$ refers to a dynamic logic swing. The $\overline{J}$ or $\overline{K}$ inputs should be changed to a logic "1" while $\overline{C}_D$ is at a high level; otherwise the $\overline{J}$ or $\overline{K}$ signal may clock the flip-flop. Ø = either logic 1 or 0 may be present.

FIGURE 2 — FLIP-FLOP LOGIC BLOCK, $\overline{J}$-$\overline{K}$ AND R-S TRUTH TABLES

INTRODUCTION

With the availability of flip-flops that will shift at rates in excess of 70 MHz, high speed shift registers are easily fabricated. These MECL II devices allow a shift register to be employed as a variable digital delay line in many applications. The pulse width degradation and delay errors are shown to amount to uncertainties of a maximum of one clock period for asynchronous inputs. This would amount to 20 ns for a 50 MHz shift register.

The flip-flop used in this application note is the MC1013 (0 to 75°C) or MC1213 (-55 to 125°C). The device is a $\overline{J}$-$\overline{K}$ type flip-flop with four $\overline{J}$ and four $\overline{K}$ logic inputs, one Reset input, one Set input, and Q-$\overline{Q}$ outputs. The 70 MHz flip-flop is a member of the MECL II Multifunction family which is available in the dual in-line, 14 pin plastic package (0 to 75°C) and the 14 lead 1/4"×1/4" ceramic flat pack. Flip-flop specifications are: minimum toggle frequency = 70 MHz at 25°C; typical toggle frequency = 85 MHz. Oversensitivity (adequate noise immunity) — the device will not toggle at 5 ns rise time and less than 300 mV input. Adequate sensitivity — the device will toggle at 20 ns rise time and an input greater than 600 mV. The flip-flop will toggle on rise times of 40 ns or less at the nominal input amplitude of 800 mV. Worst case toggle and shift frequency is 55 MHz or better over the full temperature range, -55°C to +125°C. Operating voltage is -5.2 V with negligible degradations in characteristics for ±20% variations in supply voltage. Typically rise, fall, and propagation times are from 3.0 to 7.0 ns.

Figure 1 gives the schematic of the MC1013/MC1213 with nominal values of resistance. Circuit operation is the same as explained in AN244 for the MC314/MC364. The only differences are the extra $\overline{J}$ and $\overline{K}$ inputs and improved processing that decreases internal time constants.

Figure 2 illustrates a single flip-flop logic block connected as a single stage of a shift register. The $\overline{J}$-$\overline{K}$ and R-S truth tables are also shown in the figure. For shift register operation, the $\overline{J}$ and $\overline{K}$ inputs are always complements.

DELAY REGISTER OPERATION

Figure 3 is the logical schematic for an "n" bit shift register which includes the necessary logic for electronically controlling the delay of the register in powers of two. The incoming data to be delayed is considered to be asynchronous with the internal clock oscillator and random in nature. The input data (D_I) might appear as shown in Figure 4. The figure illustrates typical waveforms that would result from D_I and a 50 MHz clock.

G_1 is used to split the input into Data (D) and Data Not ($\overline{D}$) since the remaining logic requires complementary data (dual rail logic). The OR and NOR outputs of a gate have essentially the same propagation delay so output skew is no problem. G_2 and G_3 form a logic switch that "switches off" the input data whenever C is low ($\overline{C}$ high). This prevents the undesirable transfer of data into the first $\overline{J}$-$\overline{K}$ flip flop while the clock is at a low level. If the clock input to a $\overline{J}$-$\overline{K}$ flip flop is low, a positive going waveform on $\overline{J}$ would SET the flip flop to the "1" level (Q high) or a positive going waveform on $\overline{K}$ would RESET the flip flop (Q low). This feature is undesirable in this application.

Gates G_4 and G_5 form an R-S flip flop that stores the previous input data while $\overline{C}$ is at a high level. On the positive going transition of C, the data stored in G_4-G_5 is shifted into the first $\overline{J}$-$\overline{K}$ flip flop. The J-K is then inhibited by the high level of the clock. On the positive going edge of C, new data may be started through G_2 and G_3 into G_4-G_5. The input data is delayed through gates G_1 through G_5 and then an additional delay of τ (clock period) as it is shifted through each $\overline{J}$-$\overline{K}$ flip flop.

Figure 4 illustrates several of the possible timing conditions that may occur between D_I and the clock waveforms. For example, D_I is low between time 2.3 and 3.3. This is the longest low level on the input that will not be recognized by the shift register. From the timing diagram, it is seen that if an input is present for longer than the clock period, it will be recognized and shifted through the register. The low level data between 4 and 4.5 is present long enough to be recognized, and is stretched to one clock period in length by the input gating and flip flop #1. Also the positive pulse between time 12 and 12.5 is long enough and in the proper position to be recognized.

The input levels f_0-f_8, shown in the lower portion of Figure 3, allow the selection of the clock frequency $\frac{f}{2^m}$

where m is the number of the flip flops used to divide the basic frequency of the clock oscillator. Inputs f_0-f_8 are negative logic inputs, i.e. only one input should be low at a time. The low input will enable the desired clock frequency. If all inputs go high, the register will store the data that was being shifted in the register.

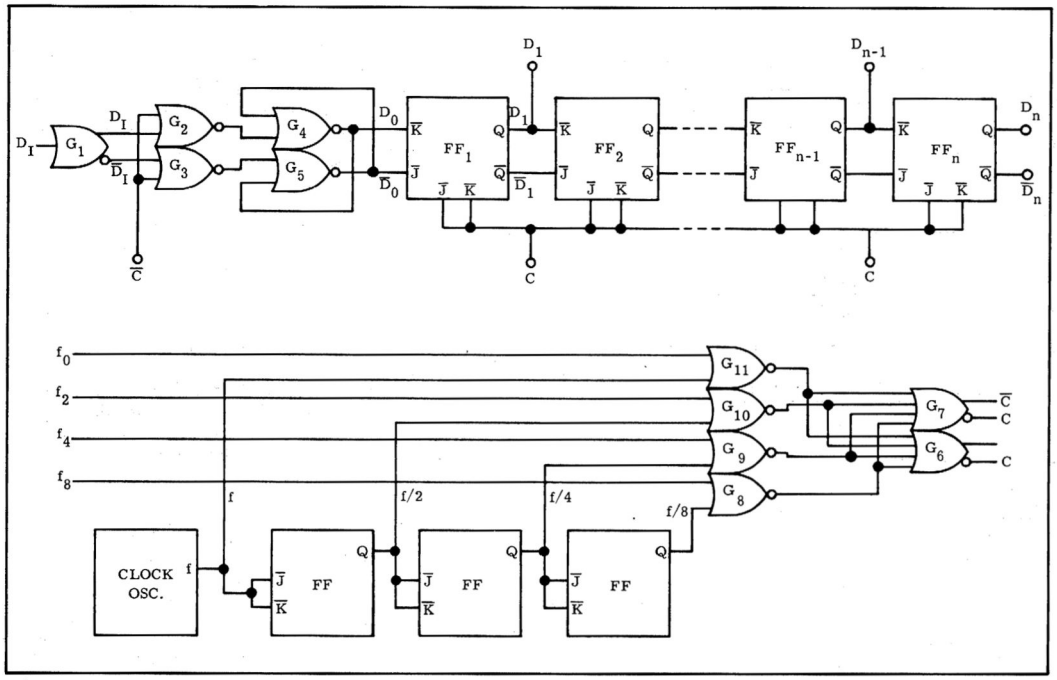


FIGURE 3 — DELAY REGISTER DIAGRAM

The preferred gate for G_1 through G_7 is the MC1023 which is a clock driver and high speed gate. This device exhibits typical propagation delays, rise, and fall times of 2ns. Two clock drivers are shown in Figure 3 where it is assumed that the number of stages in the register is ten or more. The MC1023 is a dual 4-input OR-NOR gate. By using both gates, 10 flip flops may be driven with a typical rise time of 2ns and fall time of 3.0ns. If lead lengths are kept short and low inductance printed circuit wiring employed, the register as shown in Figure 3 will shift at clock rates in excess of 70 MHz at room temperature.

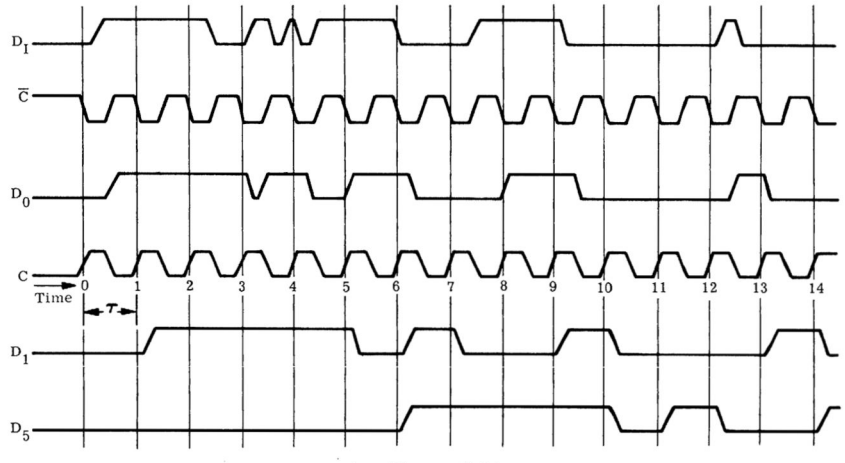
Typically the delay through the input gating using the MC1023 is a minimum of 6ns or a maximum 6ns + $\frac{\tau}{2}$. This amounts to a minimum of 6ns and a maximum of 16ns for a 50 MHz clock, depending upon the relative position of the data and the clock. The delay from D_0 to D_1 is a minimum of $\frac{\tau}{2}$ plus the delay of flip flop 1 or a maximum of τ plus the flip flop delay. For 50 MHz operation, this yields a minimum of 15ns or a maximum of 25ns. The total delay from D_1 to D_1 is then a minimum of 21ns or a maximum of 41ns. The incremental delay from flip flop 1 to flip flop 2 is τ and so forth throughout the delay register.

Assuming a 50% duty cycle clock, delay uncertainty of input information is $\pm \frac{\tau}{2}$ and the maximum length of an input datum that may not be recognized is τ. Also an input datum may be lengthened or shortened by as much as τ. The delay of the register shown, using the recommended devices is approximately 11ns + $n\tau \pm \frac{\tau}{2}$, where n is the number of MC1013/MC1213 J-K flip flops between the input and desired output, and τ is the period of the clock waveform.

Further improvement in delay register characteristics may be obtained by using the MC1022 "D" type flip flop. The input is single rail, eliminating the need for G_1. Since the flip flop operates on the master slave principle, gates G_2 through G_5 may also be eliminated. The data input is then brought directly into the flip flop with no additional gating. The delay through a register using the MC1022 is approximately 5ns + $n\tau \pm \frac{\tau}{2}$ where n is the number of "D" flip flops used including the first stage. Typically the "D" type flip flop will operate at greater than 60 MHz allowing values of τ as small as 16.5 ns.

SUMMARY

The MC1013/MC1213 may be used in shift register applications at speeds greater than 50 MHz over the specified temperature range. Incremental delays of 20ns are easily obtained and continuously variable delays are possible with variable clock frequency.



t ≈ 20ns per division

D_I = Input Data
$\overline{C}$ = Clock to input gating
D_0 = Data into first $\overline{J}$-$\overline{K}$ flip flop
C = Clock to shift register
D_1 = Delayed Data out of first $\overline{J}$-$\overline{K}$ Flip Flop
D_5 = Delayed Data out of fifth $\overline{J}$-$\overline{K}$ Flip Flop

FIGURE 4 — TYPICAL DELAY REGISTER WAVEFORMS FOR A 50 MHz CLOCK FREQUENCY

OVERSHOOT AND RINGING IN HIGH SPEED DIGITAL SYSTEMS

Whenever a switching circuit with low output impedance and fast risetime is used to drive a signal lead that is connected to several gates, overshoot will be present. The term overshoot, as used in this note, is defined as the peak to peak voltage difference between the most positive portion of the rising edge of a waveform and the "1" logic level of the waveform after all transients have decayed. In general, the lower the output impedance of a gate, the faster the risetime, the longer the wiring length, and the larger the fanout, the greater the overshoot caused when switching occurs. This note contains several tables and sets of photographs illustrating the overshoot that can be expected under various worst case configurations and loadings. Methods of overshoot reduction are applied with tabulated results from which general conclusions and guidelines are drawn.

The exact simulation of an integrated circuit load or the loading of several devices is extremely difficult with passive components. This is due to the complex and non-linear input impedance of a MECL device. The input capacitance goes through a peak value of approximately 15pF during a logic transition and averages out to less than 5pF over the entire logic swing. The input resistance will be about 50KΩ (worst case) at a logic "1" level. The input resistance will decrease exponentially if saturation of the MECL input is approached. (A MECL gate may be driven into saturation by sufficient overshoot on the input waveform, especially at high temperatures.) For system design purposes a worst case input capacitance of 5pF per device input and a 50k resistance to V_{EE} may be utilized. If sockets for the gates are used, an additional 1pF should be added per gate input. Wiring capacitance using teflon coated wire is about 1 pF per inch. Inductance per unit length of wire is about 0.02 μH per inch. These values will vary by a large amount depending upon "lead dress" and, therefore, should be considered only as "ball park" figures. When circuit measurements are being made, oscilloscope probe capacitance should be considered. The capacitance of a probe will vary from 1.8pF to about 10pF depending upon the probe design.

Attempts were made to simulate the loading caused by various fan-outs with discrete components. The best simulation was obtained by the following circuit, Figure 1, which will help to explain the parameters affecting overshoot. R_O stands for the output incremental resistance of the gate used as a driver. Values are approximately: MC301--20Ω, MC365--12Ω, MC369--5Ω. L is the series inductance of the signal lead and R_I is the input resistance of the gates used as the load. C is the shunt capacitance caused by the fan-out, wiring capacitance, socket capacitance, and probe capacitance. The value of C is 8-10pF per fan-out. R_D is necessary to damp out excessive overshoot which is caused by the lumped value of C. C is chosen to give rise time equivalent to the measured value for the given fan-out. R_D is on the order of 20Ω with higher values for small fan-out and smaller values for large fan-outs.

This load only simulates overshoot and rise time as can be seen by comparing photographs 2, 8, and 14 with 5, 11, and 17 respectively. The period of oscillation is longer for the simulated load, indicating that the value of C is higher than with the actual load. The effective capacitance of the actual load may be shown to be about 6-7pF per fan-out, i.e. 2-3pF less than in the simulated load. The difference in period of oscillation and damping indicates just how approximate the simulated load is.

How much overshoot can occur under worst case conditions in a MECL system? This question is answered by the data which are shown in the following tables. These data were obtained by using the MC301, MC365, and MC369 gates as drivers. MC356's and MC364's were used as fan-out devices. Lead lengths of 3", 6" and 12" were used with the loads constructed on printed circuit boards and plugged into a single socket which terminated the particular lead. This simulates a worst case situation since fan-out is not usually lumped at the end of a single lead. The devices used as drivers were picked at random and other devices may give somewhat different results due to output impedance and output risetime.

How much overshoot can be tolerated in a MECL system? This question is relatively easy to answer in the case of driving flip-flops, but becomes more difficult when referring to gates. When driving flip-flops, one $\bar{J}$ input may be clocked and the other inhibited at a worst case "1" level. If the level of the clocked J input exceeds the inhibiting level on the other J input by more than the required amplitude to toggle a sensitive flip-flop, then false information may be passed into the flip-flop. For room temperature operation, overshoot should

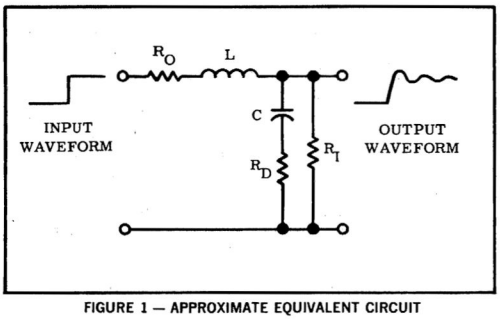


FIGURE 1 — APPROXIMATE EQUIVALENT CIRCUIT

DRIVER GATE	FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	2-MC356	5mV	8.9ns	10mV	7.7ns	50mV	6.8ns
MC301	5-MC356	40mV	9.2ns	60mV	8.5ns	110mV	8.0ns
MC301	10-MC356	90mV	10.9ns	115mV	10.9ns	175mV	11.1ns
MC301	15-MC356	95mV	12.1ns	135mV	12.0ns	200mV	12.3ns
MC365	2-MC356	40mV	6.7ns	70mV	6.2ns	145mV	5.4ns
MC365	5-MC356	80mV	6.9ns	140mV	6.6ns	215mV	6.6ns
MC365	10-MC356	150mV	8.2ns	205mV	8.2ns	270mV	8.4ns
MC365	15-MC356	180mV	9.0ns	220mV	10.0ns	300mV	10.3ns
MC369	2-MC356	80mV	4.2ns	200mV	4.5ns	300mV	4.4ns
MC369	5-MC356	120mV	5.2ns	220mV	5.5ns	330mV	6.3ns
MC369	10-MC356	180mV	7.4ns	220mV	7.7ns	350mV	9.1ns
MC369	15-MC356	200mV	8.9ns	270mV	9.0ns	370mV	9.9ns

TABLE 1 — MEASURED OVERSHOOT AND RISE TIME MC356 AS LOAD

DRIVER GATE	J-K COMMON FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	1-MC364	0mV	7.5ns	0mV	7.8ns	0mV	6.0ns
MC301	2-MC364	45mV	7.5ns	70mV	7.3ns	135mV	7.2ns
MC301	5-MC364	85mV	8.6ns	130mV	8.8ns	200mV	8.8ns
MC301	10-MC364	160mV	12.9ns	190mV	13.0ns	270mV	13.5ns
MC365	1-MC364	0mV	6.7ns	0mV	4.7ns	55mV	4.8ns
MC365	2-MC364	100mV	5.9ns	165mV	5.8ns	250mV	6.0ns
MC365	5-MC364	160mV	6.7ns	210mV	6.9ns	340mV	7.3ns
MC365	10-MC364	180mV	9.9ns	230mV	11.3ns	370mV	11.5ns
MC369	1-MC364	0mV	4.5ns	50mV	4.1ns	280mV	4.1ns
MC369	2-MC364	180mV	4.9ns	280mV	5.0ns	350mV	5.4ns
MC369	5-MC364	250mV	6.0ns	340mV	6.4ns	420mV	6.4ns
MC369	10-MC364	250mV	8.8ns	340mV	9.3ns	440mV	10.1ns

TABLE 2 — MEASURED OVERSHOOT AND RISE TIME MC364 (CLOCKED) AS LOAD

LOADING		MAXIMUM SERIES RESISTANCE (R_S)		
DC FAN-OUT	MAXIMUM EQUIVALENT LOAD CURRENT	STANDARD GATE DRIVER R_O=22	LINE DRIVER MC315/MC365 R_O=15	CLOCK DRIVER MC369 R_O=5
25	2.5mA	0	7	17
15	1.5mA	14	21	31
10	1.0mA	33	40	50
5	0.5mA	88	95	105
3	0.3mA	160	170	180
2	0.2mA	250	260	270
1	0.1mA	530	535	545

NOTE: Worst Case values are calculated from $R_O + R_S = \frac{\Delta V}{\Delta I}$

ΔV = 55mV maximum allowed "1" level voltage change (no load to full load)

ΔI = change in load current (no load to full load) for given fan-out

R_O = incremental output resistance of driver gate

R_S = series resistance added in lead between driver and fan-out

TABLE 3 — MAXIMUM ALLOWED VALUES OF SERIES RESISTANCE VS. FAN-OUT

be less than 150 mV. For worst case design over the full temperature range (-55°C to +125°C), overshoot should be limited to 100 mV or less. Although a regular gate will tolerate far more overshoot than the above-mentioned values, the worst case value of 100 mV should be used in system design. If high overshoot levels occur in a system, problems caused by the cross-coupling of noise from one signal lead to another will be compounded. For example, if 200 mV of overshoot is allowed, a normal transition of 800 mV would be changed to a 1V transition, therefore increasing cross-coupling of noise by 25%.

It is obvious that the worst case values of overshoot shown in Tables 1 and 2 are excessive. How then can overshoot be reduced? It can be seen from the approximate equivalent circuit, Figure 1, that overshoot and the associated ringing is caused primarily by the values of L and C which dominate the other parameters for large fan-outs. Overshoot may be reduced by decreasing L and C and/or adding to the damping by increasing R_O or R_D. The value of L may be decreased by running the lead close to a ground plane or using a flat conductor that has less inductance per unit length. Figures 3, 9, and 15 compared with 4, 10, and 16 respectively, show the striking difference in overshoot for 12" of teflon coated wire driving a fan-out of 15 gates when the wire is touching the ground plane and when it is an average of 3" above the ground plane. The value of C is difficult to reduce. The equivalent capacitance per gate input may be varied by perhaps 2pF depending upon the use of sockets or the direct wiring of the integrated circuits, and the method of wiring used.

The most effective method of reducing overshoot is the reduction of $L\frac{di}{dt}$, the voltage drop across L due to the rate of change of current. One way to accomplish this is by decreasing lead length or running multiple wires between the driver and load. This method is often not practical. The insertion of a resistor in series with the lead, thus increasing the series damping resistance, is the most effective method of overshoot reduction. The time constant of the transmission path is then increased, therefore causing a trade-off with risetime. The addition of a resistor causes a DC voltage drop and large values must be avoided to prevent "1" level degradation. Table 3 gives the maximum value of series resistance that may be inserted for worst case design for a given fan-out and driver.

Since capacitively coupled flip-flops toggle on peak-to-peak amplitude and are relatively unaffected by voltage input levels, higher values of series resistance may be employed. The limit on the values of resistance is determined by the worst case amplitude vs. risetime curves which may be found in AN244. The added resistance, if relatively large in value, forms an R-C integration network which determines the risetime. This may be observed in Table 4.

It is seen from Table 4 that the values of required series resistance become marginal for high fan-outs with 12" signal leads when compared to the allowed values shown in Table 3. Therefore, when driving a high fan-out with fast risetime it may be more desirable to use the following method: A separate signal lead and series resistor from the driver to each fan-out is utilized. This method may be used for a fan-out of 20 clocked flip-flops using the MC369 as a driver. The risetime to each flip-flop or gate is appreciably less for this method than when driving the devices with a single signal lead and resistor.

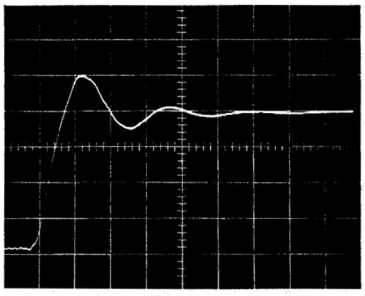
Another method of reducing overshoot is the addition of a ferrite bead around the signal lead between the driver and the load. This is another method of trading overshoot for risetime. Advantages of the ferrite bead are low cost and no shift produced in DC levels. Disadvantages are that it is effective for only small fan-outs, fast risetimes, and long lead lengths. The ferrite bead adds inductance to the signal lead at low frequencies, but this is an inductance of very low Q at high frequencies. Therefore, attenuation is produced for the high frequency components of the risetime, resulting in a slower risetime as seen by the load. Once the risetime is reduced to about 12ns, the addition of further ferrite beads to the signal line will not appreciably reduce overshoot and may actually increase overshoot for slower risetimes.

The following photographs will serve to illustrate the data shown previously. All photographs are taken with the following constants: Horizontal deflection rate 1cm per 20ns, Vertical deflection 1cm per 200mV, and signal lead lengths of 12 inches. The following notation is used for the photographs. OS = overshoot, tr = risetime, and W = 1/8", W = 0", W = 3" which stand for wire 1/8" above ground plane, 0" above ground plane and 3" above ground plane respectively. L stands for load with "A" being the actual integrated load and "S" being the simulated load. R_S is the value of series resistance inserted in the signal lead. The simulated load used in Figures 5, 7, 11, 13 was C = 150pF, R_D = 15Ω, R_I = 3K (refer to Figure 1), while the simulated load in Figures 17, 19 was C = 160pF, R_D = 8 , R_I = 3K.

DRIVER GATE	FAN-OUT	R	3" LEAD LENGTH OVERSHOOT	3" LEAD LENGTH RISETIME	R	6" LEAD LENGTH OVERSHOOT	6" LEAD LENGTH RISETIME	R	12" LEAD LENGTH OVERSHOOT	12" LEAD LENGTH RISETIME
MC301	10-MC356	0	90mV	10.9ns	5	100mV	11.7ns	18	95mV	12.8ns
MC301	15-MC356	0	95mV	12.1ns	12	90mV	14.3ns	12	95mV	14.4ns
MC301	5-MC364	0	85mV	8.6ns	13	90mV	9.9ns	27	100mV	10.2ns
MC301	10-MC364	10	95mV	14.2ns	13	100mV	14.6ns	24	95mV	15.9ns
MC365	10-MC356	10	90mV	9.4ns	15	95mV	9.8ns	25	95mV	10.3ns
MC365	15-MC356	10	100mV	10.3ns	15	100mV	10.9ns	24	95mV	11.8ns
MC365	5-MC364	20	95mV	8.5ns	27	100mV	8.7ns	51	90mV	9.8ns
MC365	10-MC364	13	95mV	11.9ns	18	95mV	12.6ns	27	95mV	13.8ns
MC369	2-MC356	0	80mV	5.1ns	24	90mV	5.4ns	62	100mV	6.0ns
MC369	5-MC356	5	100mV	5.9ns	24	100mV	6.8ns	43	100mV	7.6ns
MC369	10-MC356	10	100mV	8.7ns	24	90mV	10.5ns	33	90mV	11.4ns
MC369	15-MC356	10	95mV	10.2ns	18	95mV	11.4ns	27	95mV	12.7ns
MC369	1-MC364	0	0	4.8ns	0	50mV	3.9ns	68	90mV	4.0ns
MC369	2-MC364	27	100mV	5.9ns	62	95mV	6.7ns	75	100mV	6.8ns
MC369	5-MC364	22	90mV	7.5ns	39	100mV	8.2ns	47	100mV	8.6ns
MC369	10-MC364	15	90mV	10.9ns	22	100mV	11.9ns	33	100mV	13.4ns

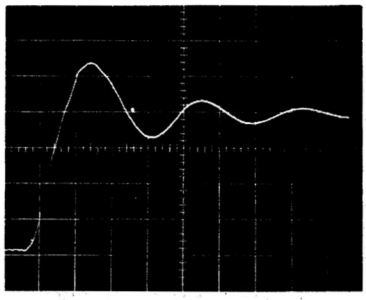
TABLE 4 — REQUIRED SERIES RESISTANCE TO REDUCE OVERSHOOT TO AN ACCEPTABLE LEVEL

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC301 FAN-OUT = 15 MC356'S



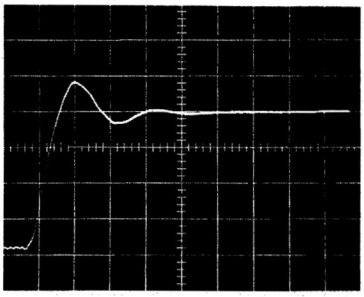
t_r = 12.3ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = A

FIGURE 2



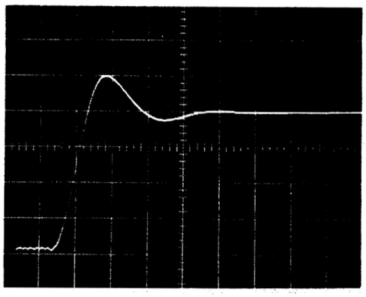
t_r = 14.2ns
w = 3"
R_S = 0Ω
OS = 280mV
L = A

FIGURE 3



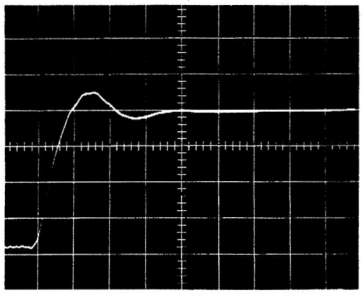
t_r = 12.3ns
w = 0"
R_S = 0Ω
OS = 175mV
L = A

FIGURE 4



t_r = 12.8ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = S

FIGURE 5



t_r = 14.7ns
w = 1/8"
R_S = 15Ω
OS = 95mV
L = A

FIGURE 6

t_r = 15.3ns
w = 1/8"
R_S = 15Ω
OS = 100mV
L = S

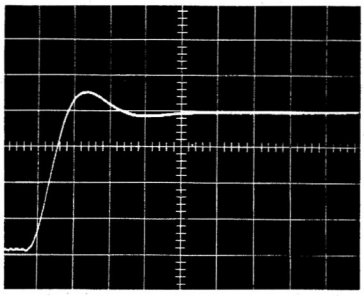
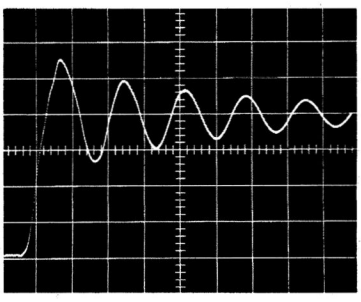


FIGURE 7

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC365
FAN-OUT = 15 MC356'S



t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = A

FIGURE 8

t_r = 12.9ns
w = 3"
R_S = 0
OS = 360mV
L = A

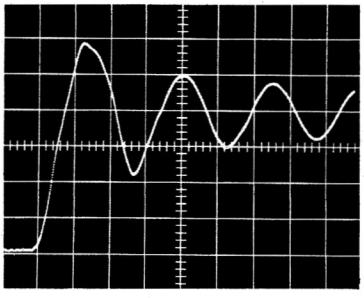
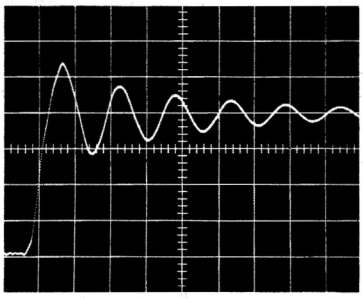


FIGURE 9



t_r = 9.5ns
w = 0"
R_S = 0
OS = 280mV
L = A

FIGURE 10

t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = S

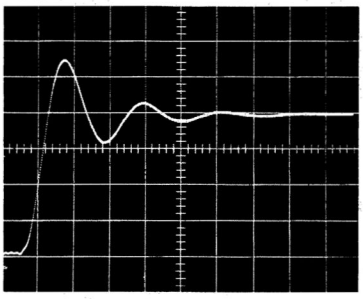
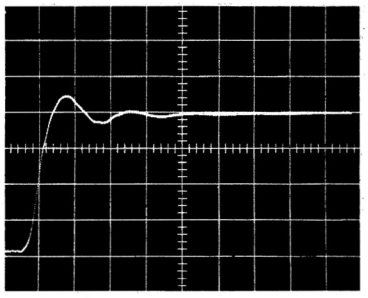


FIGURE 11



t_r = 11.8ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = A

FIGURE 12

t_r = 13.0ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = S

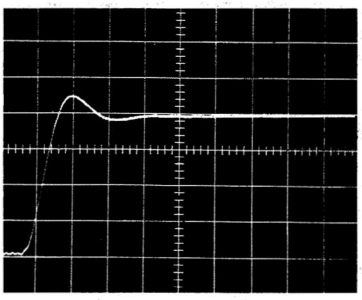
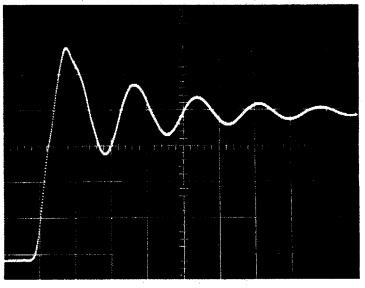


FIGURE 13

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC369
FAN-OUT = 15 MC356'S



t_r = 8.8ns
w = 1/8"
R_S = 0
OS = 370mV
L = A

FIGURE 14

t_r = 12.0ns
w = 3"
R_S = 0
OS = 390mV
L = A

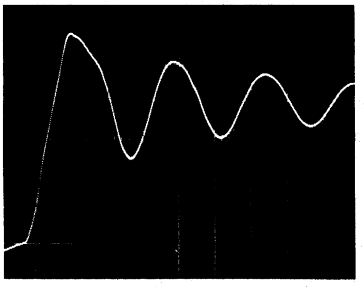
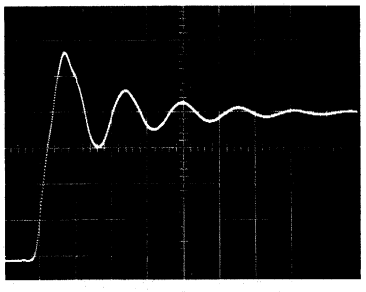


FIGURE 15



t_r = 8.3ns
w = 0"
R_S = 0
OS = 360mV
L = A

FIGURE 16

t_r = 9.2ns
w = 1/8"
R_S = 0
OS = 380mV
L = S

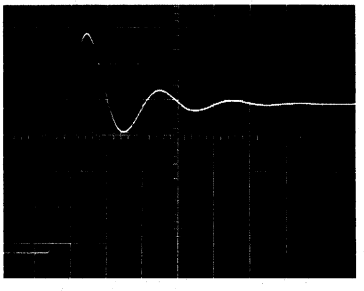
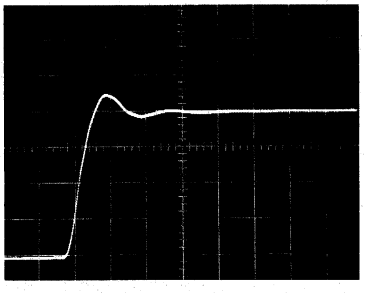


FIGURE 17



t_r = 11.6ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = A

FIGURE 18

t_r = 13.4ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = S

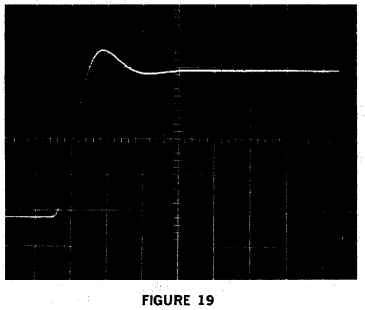


FIGURE 19

CONCLUSIONS

It has been shown that overshoot can be a system problem for long lead lengths and "lumped" fan-outs and that the amount of overshoot is primarily determined by system layout and geometries. Overshoot to typical fan-outs may be reduced to acceptable levels by inserting resistance of the proper value in series with the driver output lead. Higher fan-outs may be driven with fast risetimes by inserting a resistor of appropriate value in series with the input to each integrated circuit load, and running a separate lead from the driver to each resistor. Also, ferrite beads may be used to advantage for certain configurations of long leads and relatively low fan-outs.

As system speeds increase and MECL gates with risetimes of 2ns or less are utilized, these methods will not be useful for reducing overshoot. Strip line techniques utilizing multi-layer printed circuit boards, controlled line impedance, and terminated transmission lines will solve overshoot problems for logic into the sub-nanosecond region.