AN-467
USING HIGH THRESHOLD LOGIC

The introduction of integrated circuits has triggered an expansion in usage of electronic circuits. In the digital field, initial devices available consisted of families which generally exhibited reasonably fast operating times and operated from power supplies of 3 to 6 volts (e.g., resistor-transistor, diode-transistor, transistor-transistor and emitter-coupled logic families). The inherent advantages of integrated circuits made these families particularly attractive to the computer market and other similar fields. The industrial community, however, normally does not require high-speed operation; and it is more concerned with the electrical noise that is usually present in industrial environments. For these reasons, early digital integrated circuits did not possess the characteristics that would provide the maximum appeal to the industrial market.

Now, however, a new family of digital integrated circuits exhibits characteristics that are attractive to industrial and similar users. It is Motorola High Threshold Logic (MHTL) in the MC660 series. A summary of typical characteristics of this family are given in Table I.

This note describes members of the family, operating characteristics, and application information to help the designer to more fully utilize the logic family.

TABLE I – TYPICAL CHARACTERISTICS

V_{CC} = 15 ± 1 V
7.5-Volt Threshold
6.0-Volt Noise Margin
100 ns Propagation Delay
Fanout Capability of 10
-30°C to +75°C Operation

DEVICE OPERATION

The basic MHTL gate is shown in Figure 1A. It may be noted that this gate is very similar in configuration and operation to the Motorola Diode-Transistor Logic (MDTL) gate shown in Figure 1B. The basic difference is in diode D1, resistor values, and the collector supply voltage (V_{CC}). In MDTL, D1 is a base-emitter diode operated in its forward direction and having a drop of approximately 0.75 volt. The input threshold level of MDTL is seen to be a net of two forward diode drops (the input diode offsets a diode drop in the other direction) or about 1.5 volts. In MHTL, D1 is a base-emitter junction that is operated in its reverse direction; this is commonly called zener operation. Conduction occurs, in this case, when the junction has approximately 6.7 volts across it. Thus the threshold voltage for MHTL is one forward diode drop plus one reverse diode drop or about 7.5 volts. The normal supply voltage for this family is 15 volts ± 1 volt and in order to keep the power dissipation down, the gates have higher resistance values than comparable resistors in MDTL devices.

The MHTL gate provides the same positive-logic NAND function as the MDTL gate. It can be noted that if either of the A or B inputs is below the threshold level, possible base current to the transistor Q1 is routed to the low input. If both inputs are above the threshold level, Q1, D1 and output transistor Q2 all turn on and the output goes low. Thus the output is true or high if A or B is not true, i.e., $F = \overline{A \cdot B} = \overline{A} + \overline{B}$.

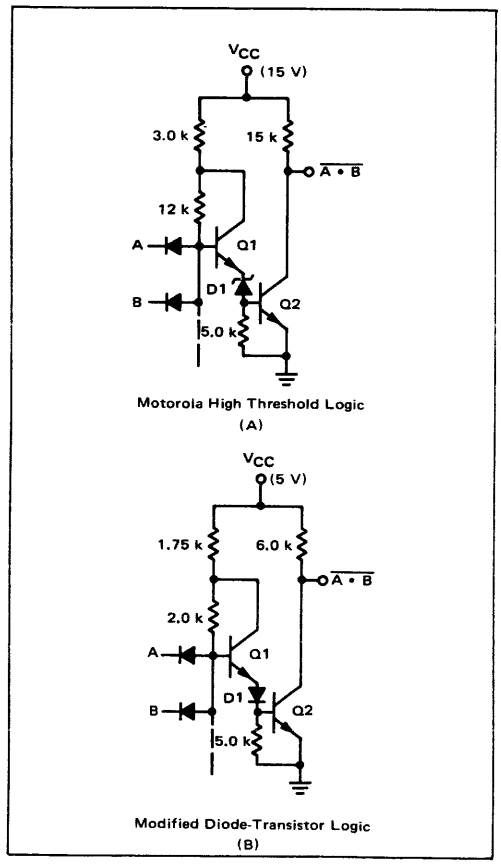


FIGURE 1 – Circuit Comparison Between the Input of High-Threshold Logic Gate (A) and Modified Diode-Transistor Logic Gate (B).

A typical MHTL transfer curve is shown in Figure 2. For normal input low voltages, less than 1.5 volts, it can be noted that the output exceeds V_{CC} minus 1.5 volts and will continue to do so for any input up to 6.5 volts, a tested point. A transition width is specified from 6.5 volts to 8.5 volts and once the input exceeds 8.5 volts, the output is guaranteed to be below 1.5 volts. This will remain true for any further increase in the input voltage. It can be noted that with a 15 volt supply, worst-case noise margin in either the high or low state is 5.0 volts. Normally, the low input voltage is 1 volt, the transition region is between 7 and 8 volts, and the high output voltage is better than 14 volts, thus typical noise margins of 6 volts are obtained in either state. As a comparison, the transfer region for other forms of integrated circuit logic generally lies within the unshaded area shown in the lower left-hand portion of the figure. From this it can be seen that MHTL could be considered as a "big brother" to other families of integrated circuits.

Although the basic gate was shown and is available with a nominal 15-kilohm pullup resistor, the devices are normally supplied with the active pullup configuration shown in Figure 3. In this circuit when Q2 is off, base current is supplied to Q3 from the 15-kilohm resistor and load current is effectively supplied through the 1.5-kilohm resistor. When Q2 is on, load current flows through D2 and Q2. Base current is also shunted from Q3 and this transistor is off in this state. The diode drop across D2 accounts for the somewhat higher low state voltage of MHTL as compared to other forms of logic families.

Each form of output has its advantages and disadvantages and the particular application would determine which device to use. The active pullup configuration has a lower output impedance in the high state and consequently will provide a higher degree of noise immunity from an energy point of view. This lower impedance can also better drive a load when in the high state, thus it is a superior interface for discrete components such as NPN transistors. The outputs of the functions with active pullup should not be connected together unless all inputs are also paralleled, to insure simultaneous operation of all devices. If one device were turned on while another device were off, the device in the low state would be required to sink current from the active pullup configuration of the high state unit. This will not damage the devices, but it leaves very little margin for providing load capacity to other devices.

The main advantage of the passive pullup configuration is its ability to have outputs of separate devices connected together. For each additional gate connected to the output of a gate, the original output loading factor of that gate must be reduced 1.25 because of the additional current that will be handled when a device is in the low state. When passive outputs are connected together, the impedance in the high state is reduced, and correspondingly the noise immunity from an energy standpoint is increased as compared to that for a single gate. The passive gate also normally has a lower V_{OL} than the active pullup configuration since only a $V_{CE(sat)}$ is involved although V_{OL} is still tested at 1.5 V with an I_{OL} of 12 mA.

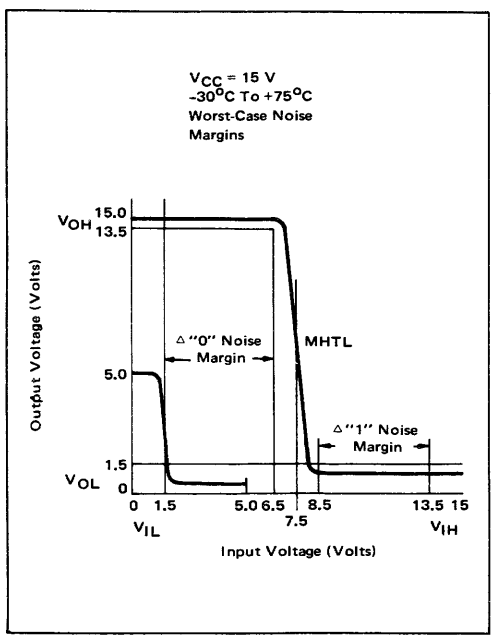


FIGURE 2 – High-Threshold Logic Transfer Curves.

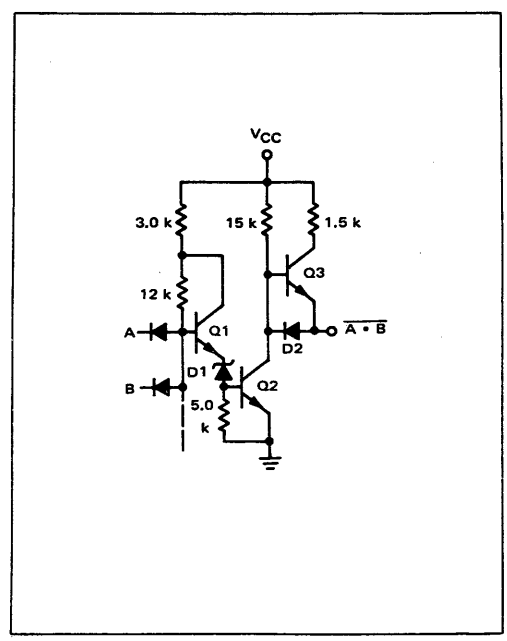


FIGURE 3 – MHTL Gate with Active Pullup

MHTL FAMILY

The MHTL family contains a sufficient variety of devices that the system designer can build complete systems with high-threshold characteristics. Gate devices providing the positive-logic NAND function are available as duals, triples and quads, as illustrated in Figure 4. Each basic configuration is available with active or passive pullup. Special logic functions are provided by the AND-OR-INVERT gates. For each gate, fanout capability is ten with a loading factor of one on each input. In addition, a dual, 4-input line driver (MC662) is available; it has a fanout capability of 30 loads while maintaining an input loading factor of one. This unit has a lower pullup impedance (1 kΩ) than the basic gate and is better suited for driving capacitive loads of discrete devices.

Two types of flip-flops are available in the MHTL family. The first is a dual J-K flip-flop that operates on a stored-charge principle and consequently is dependent on fast rise and fall times (less than 500 nanoseconds through the transition region of 6.5 to 8.5 volts) for proper operation. It is the MC663 shown in block form in Figure 5A. The second type (MC664, Figure 5B) is a single master-slave flip-flop which has a built-in diode offset between the master and slave sections. This feature makes transfer of data into the device virtually insensitive to clock rise and fall times. Both devices typically have maximum toggle frequencies of approximately 4 MHz. A detailed explanation of these two flip-flops is given in Motorola Application Note AN414, "Operation and Application of MHTL IC Flip-Flops."

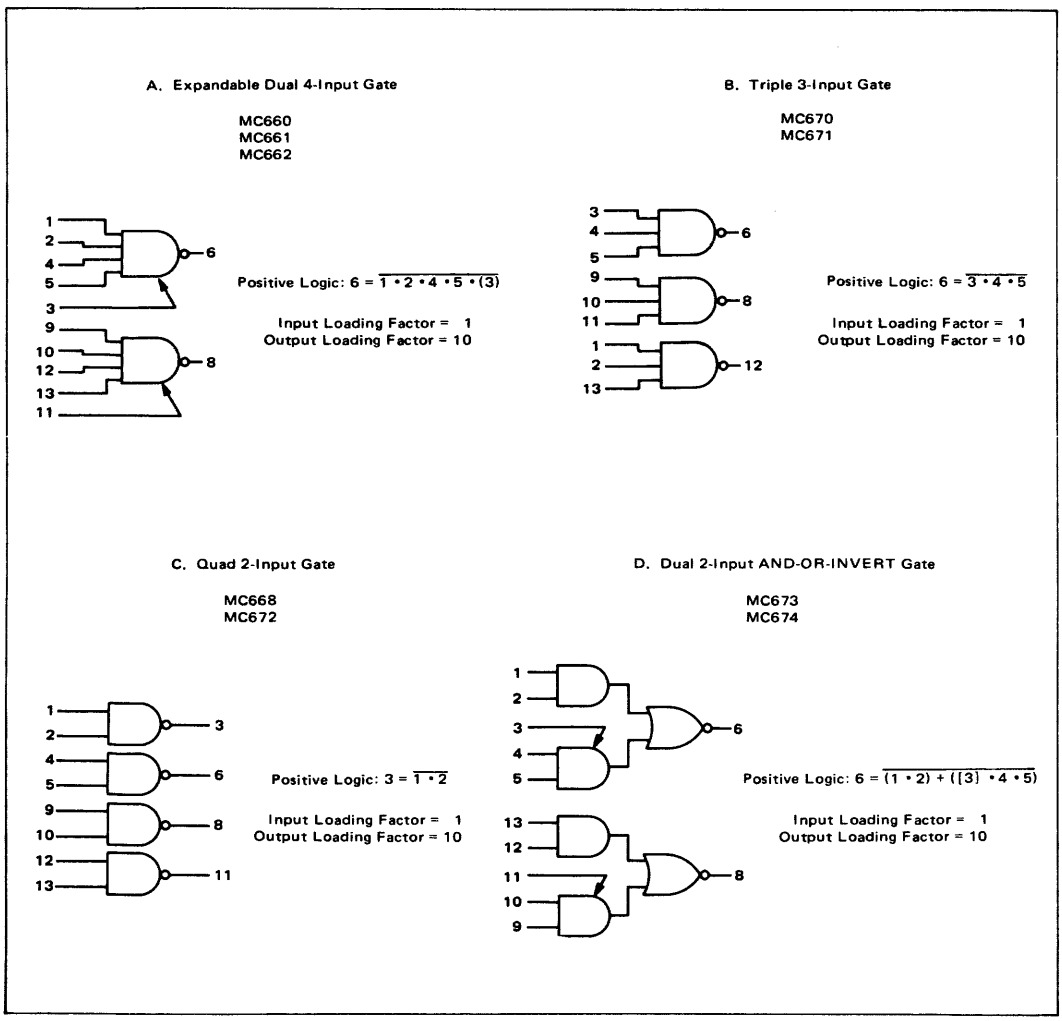
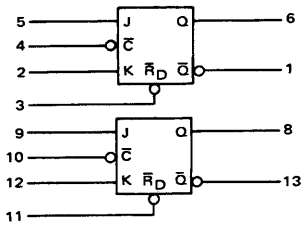


FIGURE 4 – Motorola High-Threshold Logic Gates

MC663



Truth Table

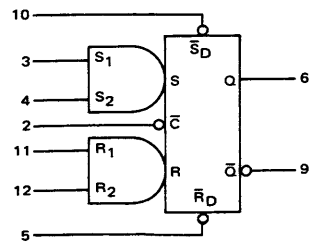
t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Input Loading Factor:
$\bar{R}_D$ Input = 2
$\bar{C}$ Input = 1.5
Other Inputs = 1
Output Loading Factor = 9
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc
f_{Tog} = 4.0 MHz typ
Total Power Dissipation = 200 mW typ

Direct input ($\bar{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n
NOTE: A low state "0" at the direct reset $\bar{R}_D$ causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

FIGURE 5A – MHTL J-K Flip-Flops.

MC664



Direct Input Operation

$\bar{R}_D$	$\bar{S}_D$	Q	$\bar{Q}$
1	1	NC	NC
1	0	0	1
0	0	NA	NA

NC = No Change
NA = Not allowed
$\bar{C}$ must be low

Clocked Operation

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Input Loading Factor:
$\bar{C}$ Input = 3
Other Inputs = 1
Output Loading Factor = 8
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc
f_{Tog} = 4.0 MHz typ
Total Power Dissipation = 160 mW typ

Notes for Clocked Operation Truth Table:

Direct inputs ($\bar{R}_D$, $\bar{S}_D$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

FIGURE 5B – MHTL Clocked R-S Master-Slave Flip-Flop.

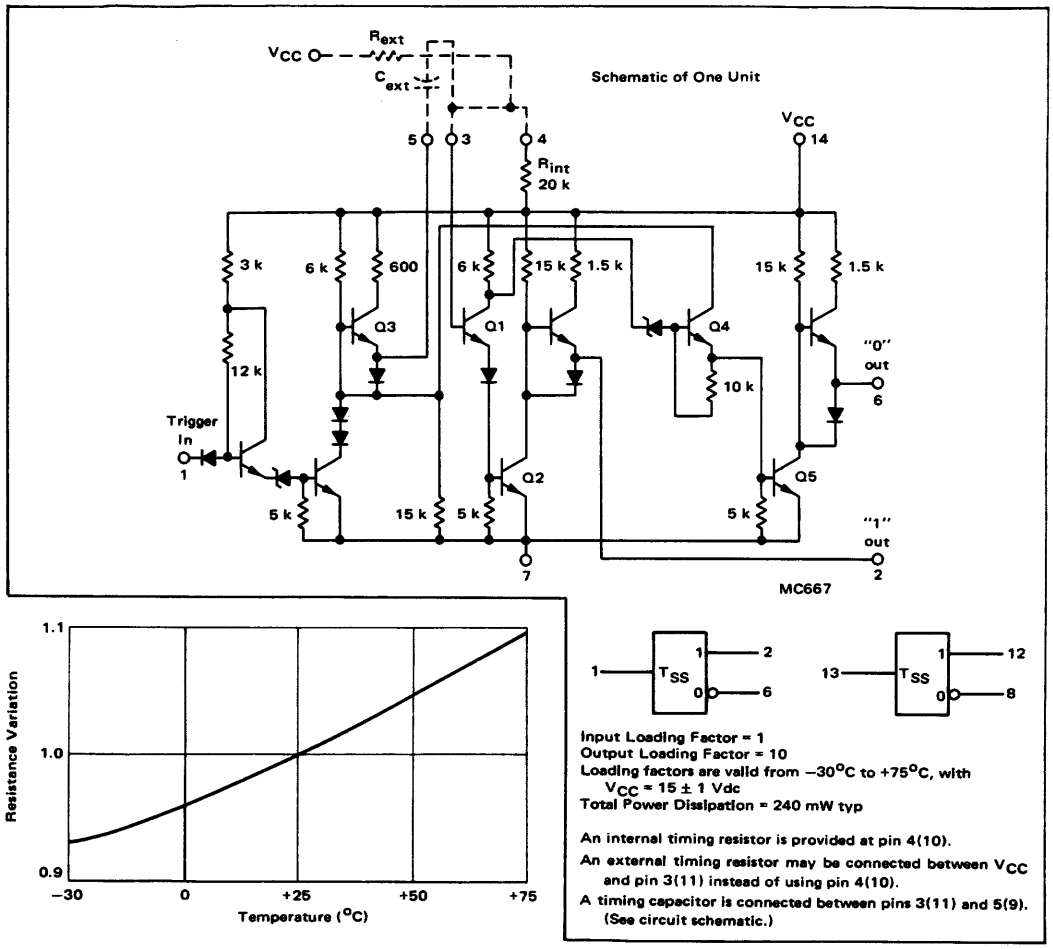


FIGURE 6B – Typical Resistance Variations with Temperature Change.

FIGURE 6A – Dual Monostable Multivibrator.

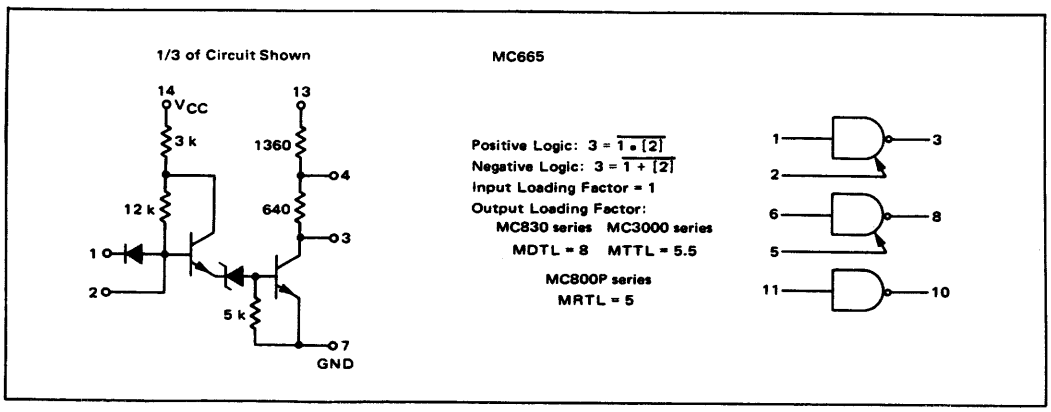


FIGURE 7 – Translator from MHTL to MRTL, MDTL or MTTL.

A dual monostable multivibrator (MC667) available in the family is illustrated in Figure 6. Each section provides both a positive-going and a negative-going pulse upon triggering by a positive-going signal that passes through the MHTL transition region of 6.5 to 8.5 volts. This is a direct-coupled circuit and will not be triggered by sharp noise pulses that do not exceed the threshold level. The width of the pulse may be adjusted with an external capacitor. The duration is approximately determined by the equation, $PW = 0.7\ R_T C_T$. An internal 20 kilohm resistor is provided for each multivibrator, but external resistors may be used for the timing function. The initial tolerances of the internal resistance may approach ± 20% with a typical temperature variation characteristic for the resistor as illustrated in Figure 6B.

Termination of the generated pulse occurs when the timing capacitor is discharged to the point where Q1 and Q2 conduct and the potential of pin three is clamped at three V_{BE} drops. However, because of this type of operation, the device is susceptible to negative noise spikes at the timing capacitor terminals. These spikes could cause Q1 and Q2 to turn off, triggering the device by turning on Q4 and Q5. Impedance at these points is kept down to approximately 600 ohms in the quiescent state by keeping Q3 on through the 15-kilohm resistor in the emitter circuit, thus aiding in noise rejection. Additionally a negative-going spike on the ground line may cause false triggering. Typical noise margins on these two leads exceed 1.5 volts. For these reasons, however, it is desirable to bypass the power supply and ground terminals at the device if noise is present on these leads and to shield the timing capacitor from noise if it exists at this point.

The design of this monostable multivibrator allows the generation of output pulses with widths virtually independent of trigger pulsewidths. However, the device does require a recovery time that begins at the end of the generated output pulse or when the trigger input returns to the "0" state, whichever is later. Allowable duty cycle may be determined from the equation, $\text{Duty cycle} = \frac{R_T \times 100}{R_T + 4.5}\%$ where R_T is in kilohms.

Two translators are available in the MHTL family and both are triple devices. The first (MC665) will convert high-threshold logic to RTL, DTL or TTL. It is shown in Figure 7. For conversion to DTL and TTL, a 5-volt supply is connected to a 2-kilohm pullup resistor through pin 13. For translation to RTL levels, pins 4, 9 and 12 are connected to the RTL supply voltage (nominally 3.6 volts). Output test conditions closely match those given for the popular Motorola MC800P series of MRTL devices and for the MC830 series of MDTL integrated circuits. Expander points without diodes are present at the inputs of two of the units, but not on the third unit. This is because of the need for additional leads for the RTL power supply and the pin limitation of the 14-lead package.

The second translator (MC666, Figure 8) is also a

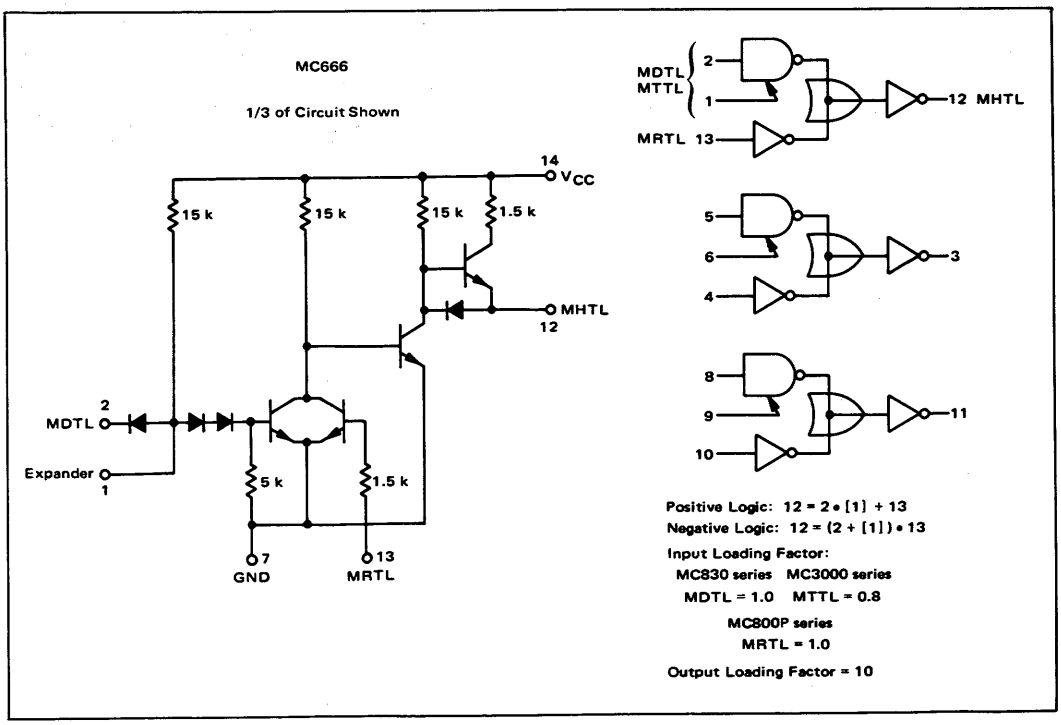


FIGURE 8 – Translator from MRTL, MDTL or MTTL to MHTL.

triple unit, but converts from DTL, TTL or RTL levels up to HTL levels. Signals from DTL/TTL sources are applied to one set of input terminals while signals from RTL sources are applied to another terminal. The different inputs provide threshold levels and characteristics compatible with MDTL/MTTL and MRTL families. Each DTL/TTL section also has an input expander terminal without diodes. These terminals may be used to expand input logic capability or to utilize high-voltage diodes to readily interface high-voltage relay or switch circuits to HTL levels. Both types of inputs may be applied simultaneously, with the output going high if the logic function of either input goes high. If the RTL input is used by itself, the DTL/TTL input must be grounded for proper operation. This is not necessary if the DTL/TTL input is being used by itself, but it is advisable under this condition to ground the RTL input to reduce any possible noise pickup.

A dual 4-input expander unit is also available in the MHTL family. It may be used to expand the input logic power of devices that have an expander node brought out for this purpose: the dual 4-input gates (MC660, 661), dual 2-input AND-OR-INVERT gates (MC673, 674), dual 4-input line driver (MC662) and the MC665 translator. The expander devices may also be connected directly to a normal diode input terminal. Operation in this manner reduces the threshold by a forward V_{BE} drop on those inputs associated with the expander units. Nominal threshold in this case is approximately 6.7 volts which is still adequate for normal operation.

The devices that have been listed in this section have been formally introduced. Expansion of the family, including complex functions, is continuing, thus providing a versatile logic family with high-noise-immunity throughout.

Propagation Delay Times

The MHTL family of devices exhibits a slower propagation time than that normally provided by other integrated circuit logic families. This is an additional aid in rejecting electrical noise because of the inability of the circuits to respond to narrow spikes of noise. Maximum propagation delays for each device are given on the appropriate data sheets. For these measurements, loading composed of a discrete RC network simulates full fanout for the device.

When actual devices are used as a load to measure propagation delay, a shoulder on the positive-going waveform may be observed at the threshold level as shown in Figure 9. This is caused by the decoupling of the actual gate loads from the driving gate. Since this point is very near the 50% level of the waveshape, a variation of approximately 50 nanoseconds may result in propagation time depending on whether the 50% point is above or below the threshold levels of the devices being used in the test. For this reason, discrete loads are used to insure repeatibility of the test conditions and yet provide an indication of the actual propagation delay.

Typical values of the propagation delays for the NAND gates with active pullup outputs are shown as a function of temperature in Figure 10.

Supply Voltage Variations

MHTL devices are tested to ensure proper operation with full fanout capability over the -30°C to +75°C temperature range and with supply voltages between 14 and 16 volts. Normally the devices will provide proper operation if the voltage varies from the specified range, but they are not tested for this operation. When the 16-volt limit is exceeded, devices may exhibit a higher leakage current on the off transistors, although typical units will endure 20 volts collector supply before this becomes evident.

Another drawback to using higher power supply values is the increased power dissipation of the circuits. Thus to keep junction temperatures within acceptable limits on

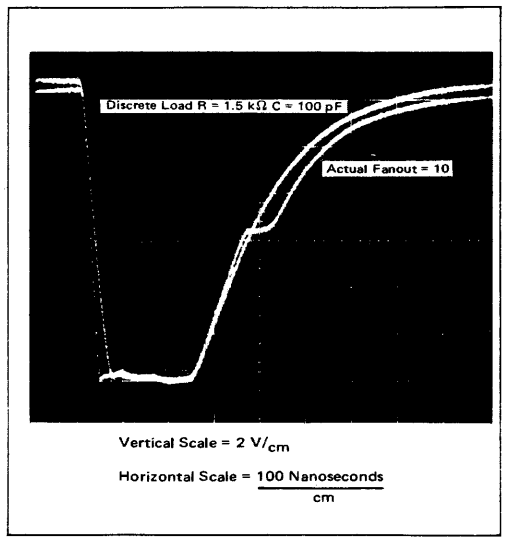


FIGURE 9 – Propagation Delay Waveforms

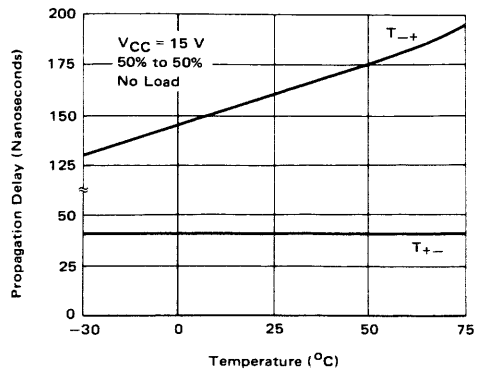


FIGURE 10 – Typical NAND-Gate Propagation Delay Times.

some devices, the ambient temperature limits must be reduced. Because of these two conditions, it is not advisable to exceed the 16-volt supply rating unless the devices have been tested to insure proper operation.

When a V_{CC} below 14 volts is used, the base drive to the output transistor is reduced and is not capable of handling the rated fanout. Figure 11 illustrates the V_{OL} values of typical units as a function of temperature with a V_{CC} of 14 volts and an I_{OL} of 12 mA. However, since the devices are not tested to operate below 14 volts, operation of the devices at these levels cannot be guaranteed. A second disadvantage of operating the units at a lower V_{CC} voltage is the reduction of the noise margin in the high state. This may be seen from Figure 2 by realizing that V_{OH} decreases while the device threshold remains constant.

LINE DRIVING

Applications exist where it is desirable to transmit data over an appreciable distance. The large logic swing of MHTL provides the means of transmitting data while minimizing the effects of noise. Unfortunately, most transmission lines have impedances below 150 ohms. The output impedance of MHTL devices is not an ideal match for these impedances, and consequently reflections may be observed on the transmission line waveforms. The line driver (MC662) has the lowest output impedance but it is still not down in the 150 ohm region. An improvement can be made in the impedance level by connecting an external resistor at the output of the line driver to V_{CC}. The additional current from a 510-ohm resistor can be handled by the MC662 when in the low state and is used to help charge the transmission line when going to the high state. Figure 12A illustrates a test set-up with 500 ft. of #22

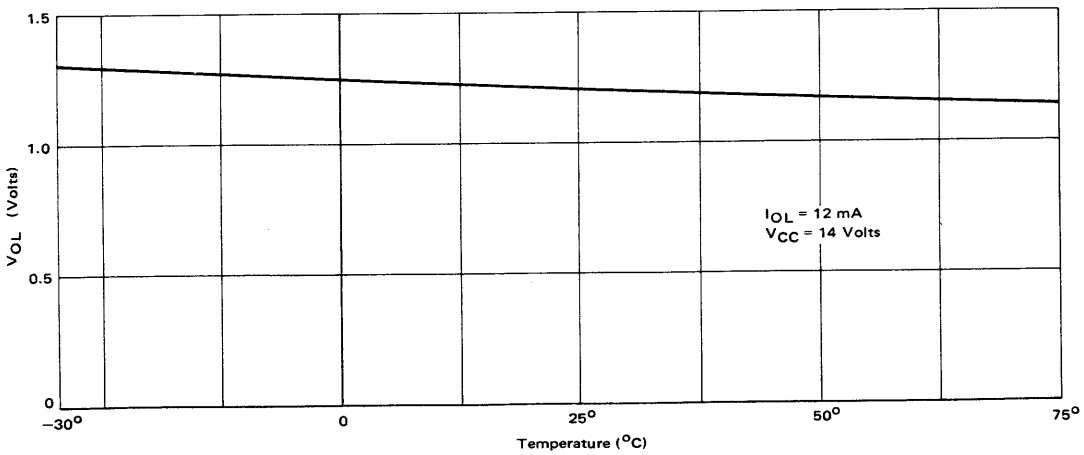


FIGURE 11 – Typical Variation in V_{OL} with Temperature.

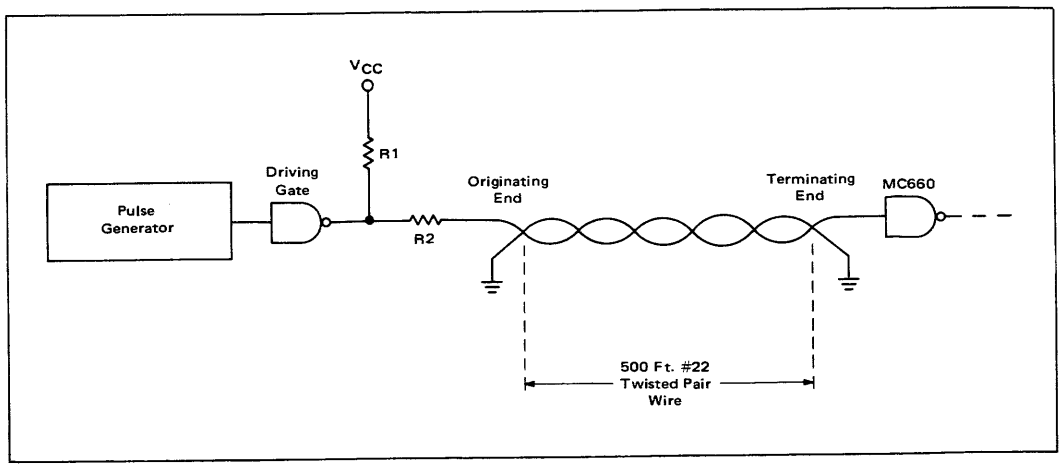


FIGURE 12A – Line-Driving Test Configuration

twisted-pair wire. Waveshapes of this connection are shown in Figures 12B, C, and D where the driving device is a standard gate output, a line-driver output, and a line driver with an external 510-ohm resistor to V_{CC} plus a 100-ohm series terminating resistor.

Special Gate Applications

Two MHTL gates may be connected with two additional resistors as shown in Figure 13A to form a Schmitt trigger. With the input originally low, gate one will be off, which turns gate two on and the output will be low. As the input rises, a point is reached where gate one turns on sufficiently to cause gate two to begin to turn off. Turn off of gate two feeds back to the input of gate one causing a regenerative action and a sharp waveshape at the output. The feedback through R2 and its action on R1 provides hysteresis for the circuit as well as sharp waveshapes. Typical values of turn-on and turn-off voltages are given in Figure 13B as a function of values of resistors R1 and R2.

In this connection, the active pullup devices should be used to minimize the effects of the feedback resistor and input voltage level when the output is in the high state. This configuration is ideal for receiving information transmitted over long lines as described previously.

Additional current sourcing may be obtained from the devices when in the high state by connecting an external resistor from the output to V_{CC} in the manner mentioned for driving transmission lines. The current from the extra resistor must be handled by the device when in the low state, which reduces fanout capability. The resistor used should not allow current to exceed the tested I_{OL} value to maintain V_{OL} values within their specified range. When using this scheme to drive an NPN device, however, an additional silicon diode is required in the base or emitter lead of the driven device to offset the normal V_{OL} value present for this type of operation.

Because of the typical V_{OL} level of 1 volt for the active

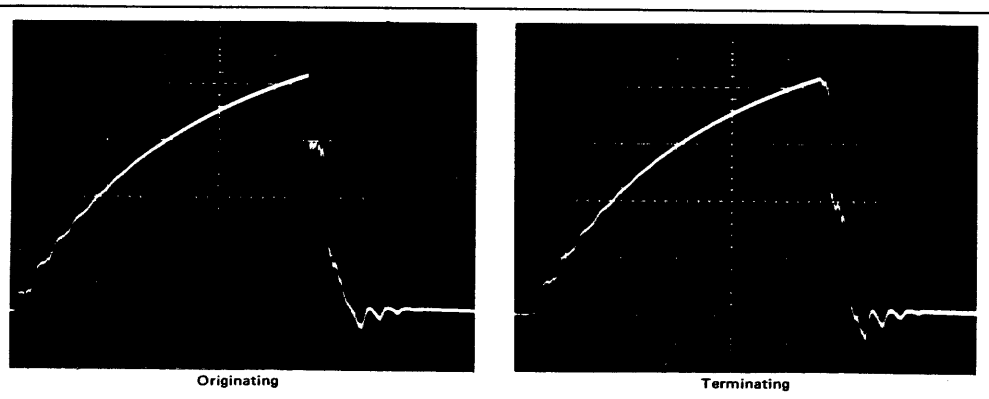


FIGURE 12B – Driving Gate – MC660 $R_1 = \infty$; $R_2 = 0$ Vert. –2 V/cm; Horiz – 5 μs/cm

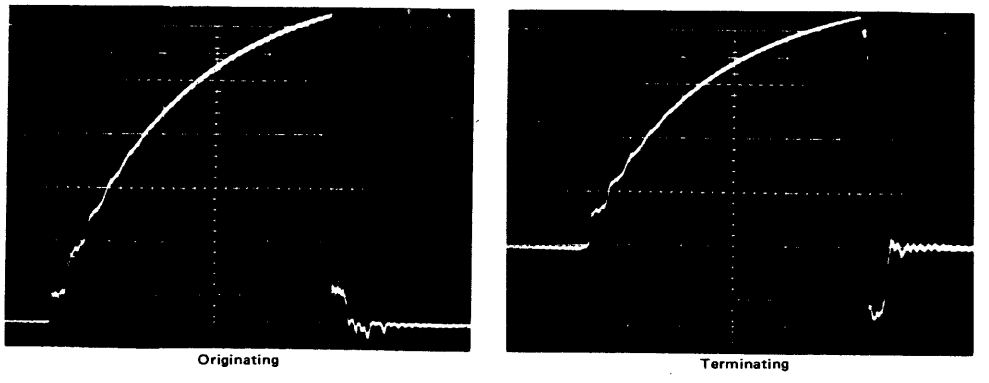


FIGURE 12C – Driving Gate – MC662 $R_1 = \infty$; $R_2 = 0$ Vert –2 V/cm; Horiz – 5 μs/cm

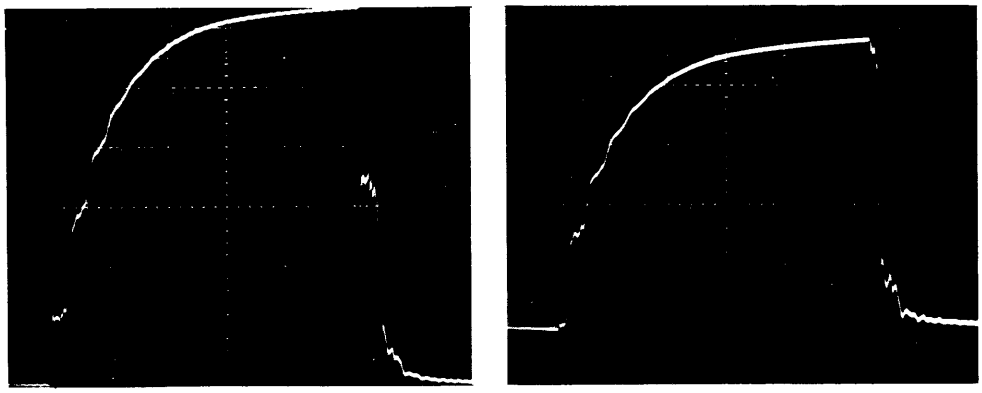


FIGURE 12D – Driving Gate – MC662 R_1 = 510 Ω; R_2 = 100 Ω Vert – 2 V/cm; Horiz – 5 μs/cm

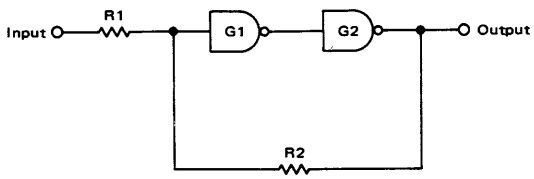


FIGURE 13A – Schmitt Trigger Connection

	R_1 = 1 kΩ		R_1 = 2 kΩ		R_1 = 5.1 kΩ	
R_2	V_{OFF}	V_{ON}	V_{OFF}	V_{ON}	V_{OFF}	V_{ON}
18 k	7.2	6.5	7.1	5.6	6.8	2.9
27 k	7.1	6.6	6.9	5.9	6.0	3.5
39 k	7.0	6.7	6.7	6.0	5.8	4.0
51 k	7.0	6.7	6.7	6.1	5.5	4.2
75 k	7.0	6.8	6.6	6.2	5.3	4.4
100 k	6.9	6.8	6.5	6.2	5.2	4.6

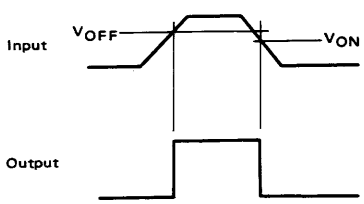


FIGURE 13B – Typical Schmitt Trigger Characteristics

pullup devices, they would not normally be considered suitable for driving NPN transistors directly because of the turn-off voltage. The active pullup devices can be used for driving NPN transistors, however, if that is the only load on the output, as shown in Figure 14. The higher V_{OL} voltage is partially due to the extra diode on the output, but if the gate is not required to sink current, then the voltage on the base of the NPN transistor will be very close to ground. It is equal to the resistance value of R1 times the leakage current of the collector-base junction of the transistor.

Cross connection of the gates as shown in Figure 15 forms a simple storage element. A momentary logic "0" on the S terminal causes the Q output to go high and the Q output to go low. A momentary low on the R terminal reverses the output state. Thus two flip-flops may be obtained from a single quad 2-input gate package.

SUMMARY

The Motorola High Threshold Logic family provides the system designer with devices that can be used to construct a complete system with noise immunity that is not available with the more familiar forms of integrated-circuit logic families. Operating from a nominal 15-volt power supply, which results in large logic swings, the family allows simple interfacing with discrete devices: MHTL devices can be used in peripheral equipment operating in noisy environments, with translators feeding into low-level, higher-speed systems in quieter locations. The unique characteristics of high-threshold logic make it ideal for many applications where integrated circuits have not previously been considered practical.

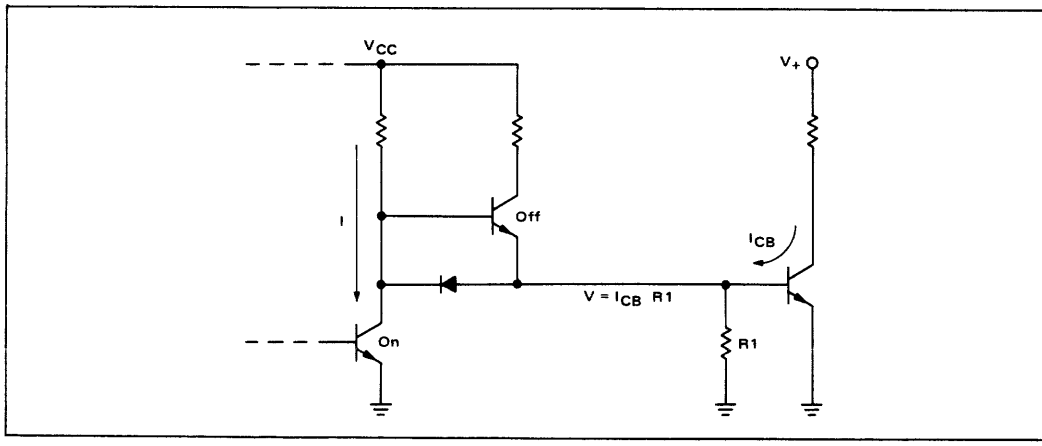
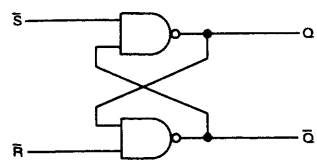


FIGURE 14 – Driving Discrete Transistors



Truth Table

S̄	R̄	Q
0	0	*
0	1	1
1	0	0
1	1	No Change

* This condition provides a high level on both outputs. The output state is indeterminable, however, if both inputs simultaneously go to a logic "1".

FIGURE 15 – Gate Memory Unit