NOISE IMMUNITY WITH HIGH THRESHOLD LOGIC

INTRODUCTION

The following material discusses general noise considerations and compares the noise immunity of the new high threshold devices with standard saturated logic devices. Some basic illustrations are provided which indicate the flexibility of usage that may be achieved with the MHTL family.

Typical characteristics of the MHTL family are:

Single 15-volt power supply
7.5V switching threshold
6 volt signal line noise margins
13 volt logic swing
30 mW gate power dissipation
85 ns gate propagation delay
4 MHz flip flop toggle frequency
-30^{O} to $+75^{O}$C operating temperature range

NOISE INJECTION

Electrical noise has always been a source of trouble for electronic systems whether they are composed of discrete components or integrated circuits. Origination of electrical noise can be from many sources both external to the electronic system under consideration and self-induced noise by the circuitry itself. Examples of external sources would be switching of inductive circuits, rotating machinery, and various electronic control circuits as depicted in Figure 1.

Internal noise may be caused by the switching of one circuit affecting the state of another circuit (Figure 2). The amount of noise induced into the passive circuit is a function of the voltage swing, current change, and the switching speed of the active circuit and the inductive and capacitive coupling between the two circuits. Coupling may also take place by the use of a common path for the active and passive devices such as a power supply or ground lead. Noise from external sources is induced into the system under similar conditions. Generally, noise is a random combination of many sources and as such is extremely hard to analyze. The net result, however, is that induced positive and negative spikes relative to the quiescent condition of a line may cause erroneous information to be absorbed into the system. This condition must be avoided if proper operation is to be achieved by the unit.

NOISE REDUCTION TECHNIQUES

Several schemes have commonly been employed to reduce the effect of electrical noise on a system composed of integrated circuits. Physical shielding of the integrated circuits and its associated wiring prevents external electromagnetic radiation from inducing noise into the circuitry. Special buffering circuits may be employed between the electronic circuits and signal leads dependent on external sources. These signal leads in many cases require special routing considerations and special shielding. Extra filtering of the power supply leads may be required to reduce the noise introduced by this route. Internal noise generation may require special spacing and routing considerations as well as maintaining short lead lengths. In some cases the power supply may need to be by-passed at several points on a board.

The amount of additional components and equipment necessary to protect integrated circuits from electrical noise can increase to a point where it is economically desirable to seek other methods of operation to obtain the desired results. It would be advantageous to have an integrated circuit family with a high degree of inherent noise immunity for economical construction of an electronic system. This will minimize the amount of special care needed for proper circuit operation in areas with a high electrical noise environment.

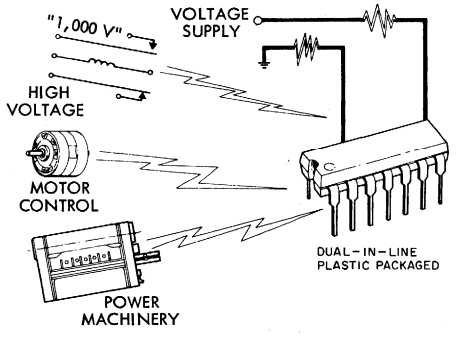


FIGURE 1 - EXTERNAL NOISE GENERATOR

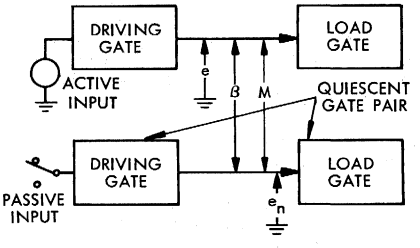


FIGURE 2 - INTERNAL NOISE GENERATOR

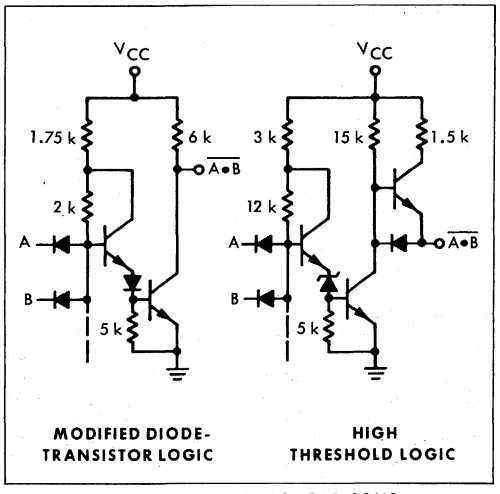


FIGURE 3 - GATE COMPARISONS

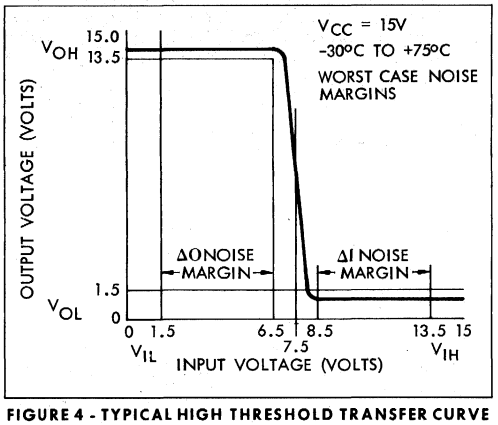


FIGURE 4 - TYPICAL HIGH THRESHOLD TRANSFER CURVE

devices demands a higher power supply and a nominal 15 volts is used. The transfer curve for the basic gate operating with a 15 volt supply is shown in Figure 4. It can be seen that for any input signal up to 6.5 volts, the output will remain in the high state or above 13.5 volts. A 2-volt margin, from 6.5 volts to 8.5 volts, is used for the transition region and guards against variations between manufacturing lots and temperature effects from -30°C to +75°C. At 8.5 volts on the input, the output is in the low state or less than 1.5 volts and remains there for any further increase of the input voltage. This diagram indicates worst case noise margins of 5 volts in both the high and low states for a V_{CC} of 15 volts while typical values are about 6 volts.

LOGIC FAMILY COMPARISONS

BASIC OPERATING CHARACTERISTICS

A comparison of basic operating characteristics for high threshold logic with the standard forms of logic is provided in the table shown in Figure 5. The values given are typical for an ambient temperature of 25°C and indicate relative characteristics between the different families. One difference that should be noted is that the high threshold logic is slower than the other families. This characteristic aids in the rejection of noise and will be illustrated in following figures.

	V_{CC} (VOLTS)	GATE POWER DISSIPATION (mW)	PROPAGATION DELAY (ns)	DC NOISE IMMUNITY (VOLTS)	LOGIC SWING (VOLTS)
RESISTOR TRANSISTOR LOGIC	3.6	12	25	0.5	1.0
MODIFIED DIODE TRANSISTOR LOGIC	5.0	8	30	1.2	4.5
TRANSISTOR – TRANSISTOR LOGIC	5.0	15	10	1.2	3.5
HIGH THRESHOLD LOGIC	15	30	85	6	13

FIGURE 5 - BASIC OPERATING CHARACTERISTICS

A HIGH THRESHOLD LOGIC

The most popular families of integrated circuits in use today exhibit a comparatively high speed of operation and have typical threshold values between 0.7 and 1.5 volts. A new type of logic family, High Threshold Logic (MHTL), has been developed that closely resembles the modified diode-transistor logic family (Figure 3). The basic difference is that the high threshold logic uses a reverse biased base-emitter junction operating in the avalanche breakdown mode as a threshold element. As can be seen in the figure, the logical NAND function is provided by each gate. The inputs of the modified diode-transistor gate must exceed two forward base emitter drops or typically 1.5 volts before base current is applied to the output inverting transistor providing the "0" state. In the high threshold device, however, the inputs must exceed the reverse biased base-emitter breakdown plus one forward V_{BE} drop or typically 7.5 volts before the output inverting transistor turns on. Since the other logic families exhibit a threshold level similar to or less than the modified diode-transistor device, a considerable increase in threshold level has been obtained with the new configuration. The higher threshold incorporated in the

SIGNAL LINE NOISE IMMUNITY

Measurements were made on the different logic families to determine the signal line noise immunity not only from a voltage margin consideration, but also from a pulse width and energy point of view as well. Figure 6-A illustrates a test set-up to measure immunity of the gate to noise on the signal lead. Positive going noise was injected on the signal lead for this set-up with the output of gate #1 in the low state. When sufficient noise was injected, the flip-flop driven by the second gate would begin to toggle indicating the effect of the injected noise. This type of test not only measures the power needed for disturbance, but also the pulse width of noise necessary to propagate through and cause faulty operation of a driven device. A series of values of voltage level and injected current to cause disturbance were taken versus the pulse width at each corresponding point. Current readings were obtained as a voltage drop across the pulse generator resistor. The pulse generator offset voltage was adjusted to eliminate the effect of its quiescent condition on gate levels. Voltage threshold as a function of pulse width is plotted in Figure 6-B. The energy of each logic family is plotted in bar graph form at the knee of each respect-

ive curve in Figure 6-C. For narrower pulse widths, the energy necessary to cause a disturbance increases. The high energy value obtained for MHTL is a result of the high threshold voltage and low gate impedance in this state.

Figure 7-A illustrates a similar test except that gate #1 is in the high state and negative going noise is injected on the signal lead. Similar results are shown in Figure 7-B and C.

GROUND LINE IMMUNITY

Tests were made on the devices to provide information on the immunity to noise injected on the ground terminal. The test configuration is shown in the first part of Figure 8. A plot of voltage threshold versus pulse width is given in Figure 8-B for the worst case condition found for the particular family dependent on the input state. The energy relationships are provided in Figure 8-C.

POWER SUPPLY IMMUNITY

A similar test was made for noise injected on the power supply lead. In this case, the flip flop will only be affected by negative going noise and the results indicate worst case conditions for the particular family dependent on the state of the first gate. The test configuration and results are given in Figure 9.

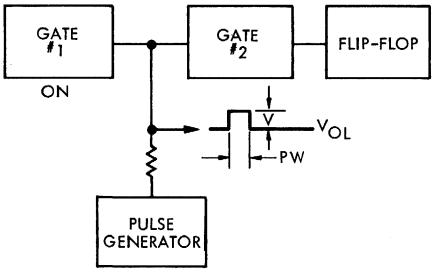


FIGURE 6A

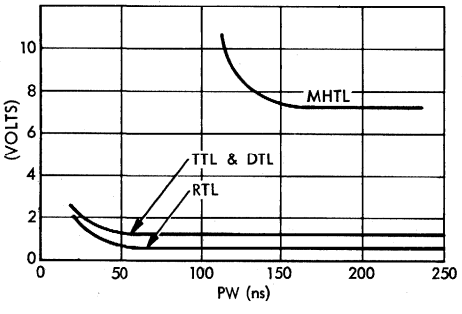


FIGURE 6B

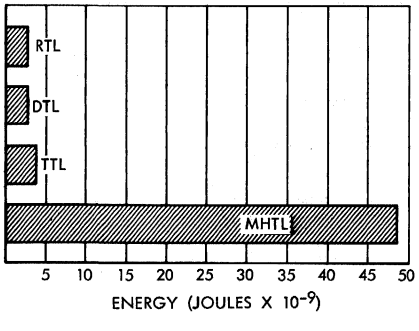


FIGURE 6C

SIGNAL LINE NOISE IMMUNITY

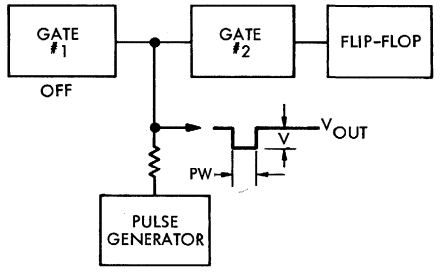


FIGURE 7A

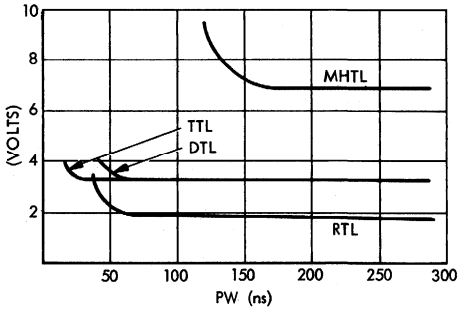


FIGURE 7B

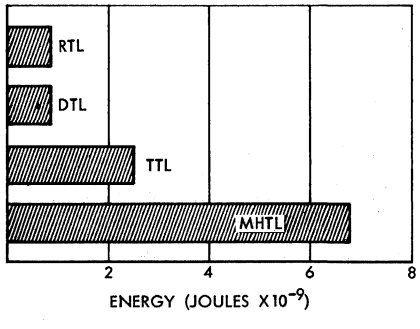


FIGURE 7C

SIGNAL LINE NOISE IMMUNITY

The preceding tests were taken with a fanout of one on the first gate and a fanout of the flip flop only on the second gate. This condition tends to be an advantage for the RTL family and the results are somewhat optimistic in this case.

These comparisons indicate that the high threshold logic has an appreciable inherent advantage over the standard families of integrated circuits. In addition, the higher threshold level present in these devices provides a considerable margin that may be used in conjunction with simplified buffering networks to filter out excessive noise spikes under very extreme conditions.

USAGE

The preceding discussion has generally referred to the basic high threshold gate circuit. Additional components are available, however, which exhibit the same noise immunity characteristics obtained by reverse biased base-emitter breakdown action. The availability of other units such as line drivers, J-K flip flops, R-S flip flops, and monostables will allow the designer to construct a complete logic system with a high degree of noise immunity throughout.

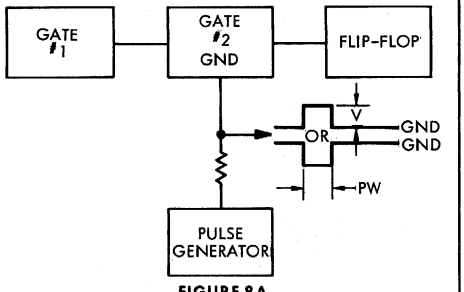


FIGURE 8A

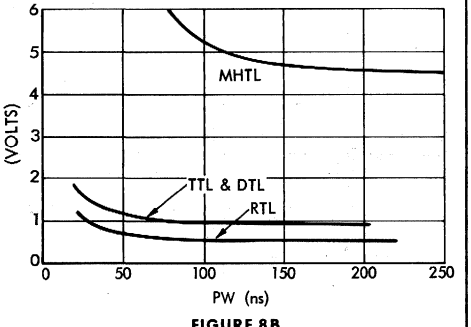


FIGURE 8B

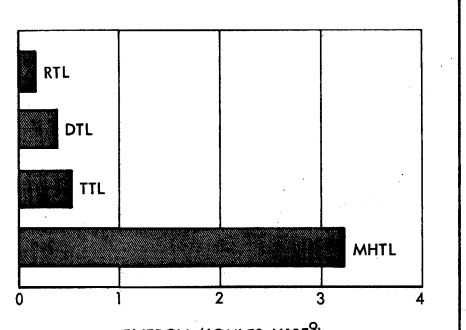


FIGURE 8C

GROUND LINE NOISE IMMUNITY

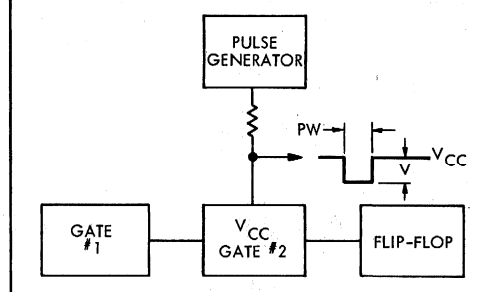


FIGURE 9A

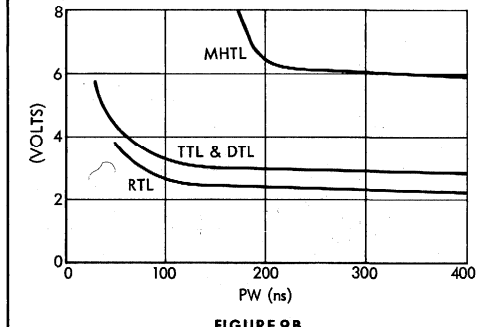


FIGURE 9B

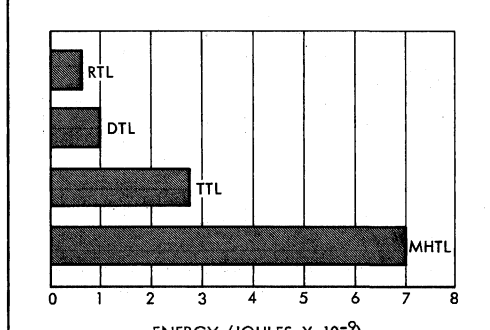


FIGURE 9C

POWER SUPPLY NOISE IMMUNITY

Situations arise where it would be advantageous to work into a system that operates at a higher speed than is obtainable by the high threshold devices. Translation between high threshold logic and standard logic families can be accomplished to allow the usage of high threshold devices as peripheral circuitry to a higher speed logic system. Thus, the high threshold devices may be operated in the noise environments and translation may take place into the lower threshold and higher speed system at the appropriate locations as indicated in Figure 10.

The higher supply voltage used in this logic family provides for the convenient interfacing with many discrete components. For example (Figure 11), the input may be controlled by a photo transistor so that illumination will cause the gate output to be high and darkness will provide a low output state. The output of the gate might feed into a logic system such that after a specific count would operate a relay. If a line driver unit were used as the output element, a 35mA, 15-volt relay could be employed. Other components such as lamps, SCRs, or transistors may also be driven directly at the output. As can be seen, the uses of the high threshold devices are many and varied.

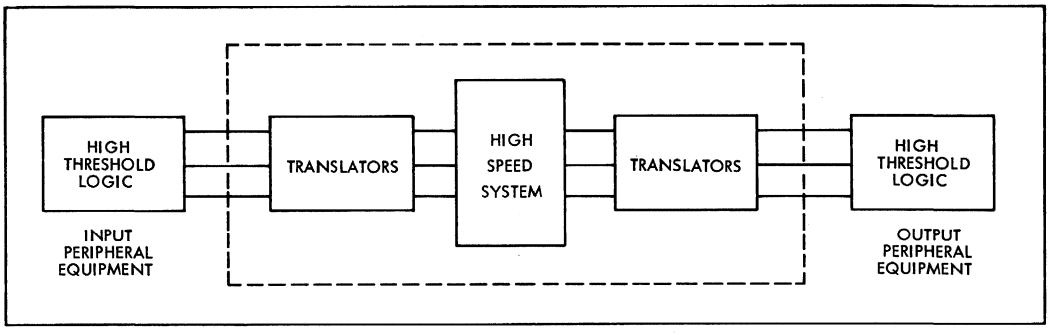


FIGURE 10 - OPERATING AS PERIPHERAL COMPONENTS

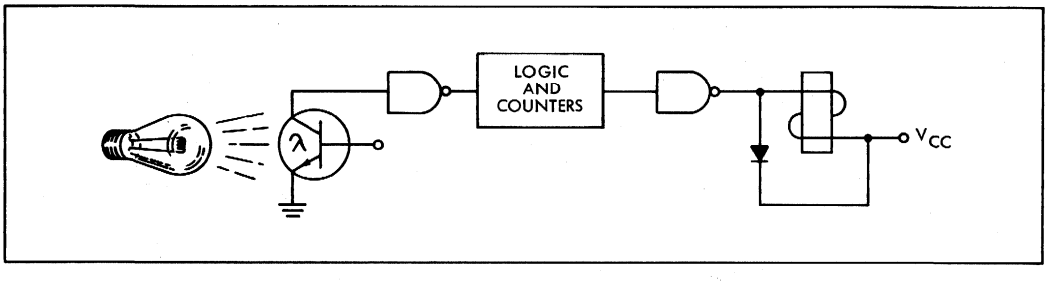


FIGURE 11 - OPERATING WITH DISCRETE COMPONENTS

SUMMARY

The new high threshold logic provides an integrated circuit logic family with a greater inherent immunity to electrical noise than is available with standard logic families. This logic family is ideal for situations where a large degree of electrical noise exists and where it is desirable to minimize the additional precautions necessary to reduce the effects of electrical noise. Input and output compatibility of the units with discrete components opens the door for a wide range of device employment.

OPERATION AND APPLICATION OF MHTL I/C FLIP-FLOPS

INTRODUCTION

The new High Threshold Logic (MHTL) line is designed to satisfy the requirements for systems that will operate in high electrical noise environments. The basic gate circuit of the family is essentially the same as the MDTL gate circuit with the coupling diode replaced by a reverse biased base-emitter junction which operates in the avalanche breakdown mode thus achieving a high input threshold. This family provides a positive logic NAND function or a negative logic NOR function.

Some typical characteristics of the family are:

- Single 15-volt power supply
- 7.5 V switching threshold
- 6-volt signal line noise margins
- 13-volt logic swing
- 30 mW gate power dissipation
- 100 ns gate propagation delay
- -30^{o} to $+75^{o}$C operating temperature range

Two flip-flops are currently available in the MHTL family, a dual J-K, the MC663P and a master-slave R-S, the MC664P. This application note describes the mode of operation of each flip-flop circuit in detail and will illustrate some typical uses of the devices.

MC663P DUAL J-K FLIP-FLOP

The MC663P unit contains two independent J-K flip-flops each with its own clock ($\overline{C}$) and direct reset ($\overline{R_D}$) terminals as shown in the block diagram of Figure 1A. Operation of the flip-flop in the synchronous or clocked mode follows the conditions shown in the Synchronous Truth Table in Figure 1B. The information on the J and K leads is effectively applied to the flip-flop when the clock lead is high and the output corresponds to the (n+1) truth table conditions upon the negative transition of the clock potential with commutation of the flip-flop occuring as the clock potential passes through the transition region (from 8.5 volts to 6.5 volts). The rise and fall times through these levels should not exceed 1 microsecond for proper operation. Clock pulse width at the 8.5 volt level should be greater than 200 nanoseconds, although typical units will operate with a 100 nanosecond pulse width. Operation in the synchronous mode requires that the direct reset inputs be terminated to V_{CC} if they are not used.

The direct reset terminal may be used to place the Q output in the 0 state independent of the steady state conditions on the J, K and $\overline{C}$ inputs. This is accomplished by

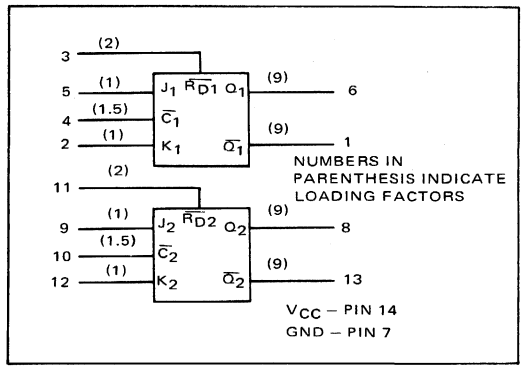


FIGURE 1A – MC663P BLOCK DIAGRAM

SYNCHRONOUS TRUTH TABLE

t_n		t_{n+1}	
J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Q_n	$\overline{Q_n}$
1	0	1	0
0	1	0	1
1	1	$\overline{Q_n}$	Q_n

a. Direct input ($\overline{R_D}$) must be high.
b. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
c. 0 denotes low state, 1 denotes high state.
d. Q_n is the state of the Q output in the time period t_n.

DYNAMIC J-K TRUTH TABLE

J_n	K_n	J_{n+1}	K_{n+1}	Q_{n+1}
1	*	0	K_n	1
*	1	J_n	0	0
1	1	0	0	$\overline{Q_n}$
*	*	1	1	Q_n

* – Don't care.
n – Condition before change.
n+1 – Condition after change.
Clock and direct reset must be high.

FIGURE 1B – MC663P TRUTH TABLES

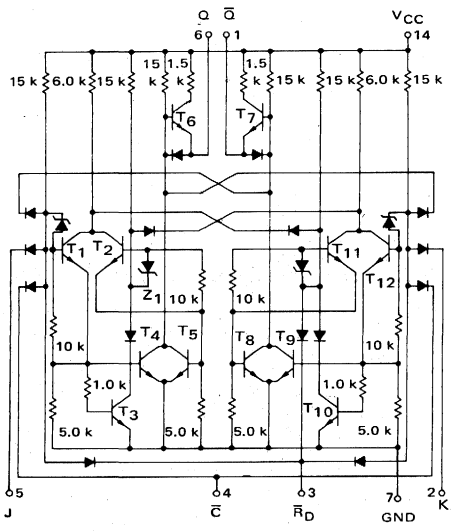


FIGURE 1C – CIRCUIT SCHEMATIC 1/2 MC663P

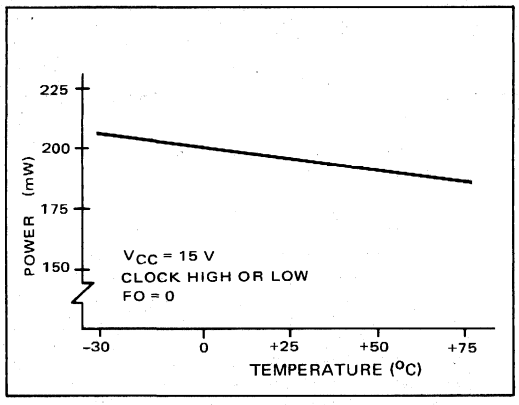


FIGURE 2A – TYPICAL MC663P POWER DISSIPATION versus TEMPERATURE

applying a logic zero to $\overline{R_D}$ for a period not less than 150 nanoseconds.

A third mode of operation may be achieved with these flip-flops as indicated in the Dynamic J-K Truth Table in Figure 1B. Operation in this mode requires the clock input as well as the direct reset input to be in the logic 1 state. Applying a logic 0 to the J and K inputs for a period greater than 150 nanoseconds will give the results indicated in the truth table. The rise time following an independent J or K negative excursion is not critical if the flip-flop remains in the given state; however, it should be less than 1 microsecond if both inputs are connected together when a logic 0 is applied or if the state of the flip-flop is changed by a negative transition on the other input. This characteristic will allow negative going signals to be capacitively coupled into the flip-flop when the J and K inputs are normally held high by external resistors.

Operation of the circuit will be explained using the schematic in Figure 1C. Initially, consider the following conditions: Q output in the low state and correspondingly the $\bar{Q}$ output in the high state, the clock input in the low state, and the direct reset input in the high state. Under these conditions, transistor T_6 will be off, transistor T_7 is on supplying current to any load connected to the $\bar{Q}$ output and T_5 is on, as will be explained later, sinking any load current on the Q output. Transistor T_2 is on with base current supplied through zener Z_1. Transistor T_2 being on supplies base current to T_5. All other transistors are off and this is the quiescent state for these conditions. If the clock input goes high and the J input is high or open, transistor T_1 turns on which also turns on T_3 and T_4. Transistor T_3 turning on will turn off T_2 which correspondingly turns off T_5. It should be noted that the output conditions have not changed due to the logical 1 on the clock input. The flip-flop will remain in this condition as long as the clock and J inputs remain high, but if either input goes low, the flip-flop will change state. If either the J or clock inputs go low, transistor T_1 turns off and its collector potential will rise causing T_{11} to turn on. T_{11} turning on supplies base current to T_8 and the $\bar{Q}$ out-

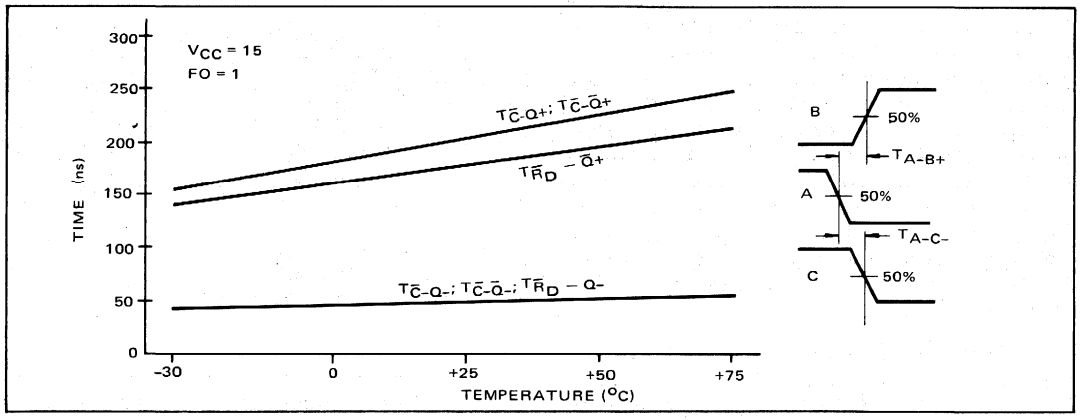


FIGURE 2B – TYPICAL MC663P PROPAGATION DELAY TIMES versus TEMPERATURE

put goes low. Transistors T_3 and T_4 are delayed in turning off after T_1 shuts off due to the charge stored in the base of T_4. Transistor T_3 being on prevents T_2 from turning on and T_2 will be held off once T_{11} turns on. Finally, when T_4 turns off, T_5 is also inhibited and the Q output goes high completing the flip-flop transition. A similar action will occur from this state to cause transition back to the original state if the clock and K input terminals are considered. It can be noted that commutation of the flip-flop may be inhibited by a logic 0 on the J and K inputs. This will prevent transistors T_1 or T_{12} from turning on when the clock is high and thus prevents commutation.

The flip-flop may be set to the Q = 0 state by use of the direct reset terminal $\overline{R_D}$ when the flip-flop is in the Q = 1 state. A logic 0 on $\overline{R_D}$ inhibits the J, K, and $\overline{C}$ inputs and will turn off T_{11} causing T_2 and T_5 to turn on placing the flip-flop in the Q = 0 state. T_{11} turning off removes the base current from T_8 and the $\overline{Q}$ output will go to the logic 1 level.

The load applied to the output terminals must be limited such that the output voltage will not be less than 8.5 volts when in the high state. This is necessary for proper cross-coupling between the two outputs of the flip-flop and the input circuitry.

Typical characteristics of the MC663P over the operating temperature range are provided in Figures 2A and B.

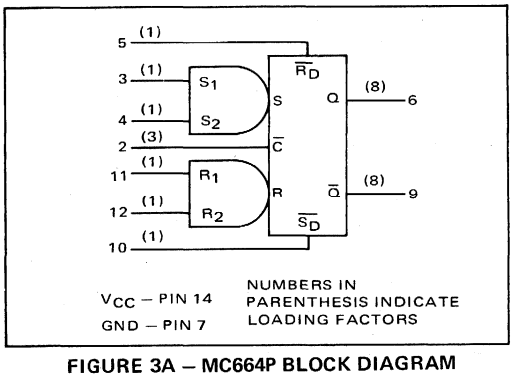


FIGURE 3A – MC664P BLOCK DIAGRAM

MC664P R-S FLIP-FLOP

The MC664P is a dc-coupled R-S flip-flop of the master-slave or two-phase type. Since it is an R-S type, simultaneous high inputs are not allowed because the output cannot be predicted after a negative clock transition. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.

The block diagram shown in Figure 3A indicates the logic function of the flip-flop as well as providing the loading factors for the device. The loading factor of 3 for the clock terminal is tested with the clock input at 1.5 volts. The output loading factors of 8 are reduced from the standard MHTL gate loading factor of 10 because of internal flip-flop cross connections.

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:
Direct inputs ($\overline{R_D}$, $\overline{S_D}$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

DIRECT INPUT OPERATION

$\overline{R_D}$	$\overline{S_D}$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock ($\overline{C}$) input must be low
NC = No change
NA = Not allowed

FIGURE 3B – MC664P TRUTH TABLES

The truth tables for the circuit are provided in Figure 3B for both clocked operation and for the direct input terminals. It should be noted that the $\overline{R_D}$ and $\overline{S_D}$ terminals are high for clocked operation while direct set and reset requires the clock to be low.

The schematic for the MC664P is shown in Figure 3C. Operation of the circuit will be described by making the initial assumptions that the flip-flop is in the Q = 0, $\overline{Q}$ = 1 state, that the clock ($\overline{C}$) is low, and that the direct set and reset ($\overline{S_D}$, $\overline{R_D}$) terminals are high or open. Under these conditions, T_{10} and T_{13} would be off while T_8 and T_{11} would be on. Transistor T_9 is on and supplies base current to T_8 through the zener diode. For this situation to exist T_4 and T_5 would also be on, while the remaining transistors in the circuit are off. This indicates the quiescent condition for the flip-flop under the initial conditions.

To illustrate commutation of the flip-flop, assume that inputs S_1 and S_2 are open or high and that either R_1 and/or R_2 are low. Now, as the clock potential rises to approximately 7 volts, the first change to occur will be the conduction of T_7 which provides a second base current source to T_8 which is already on. A further increase in the clock potential of one forward V_{BE} magnitude will cause T_1 to turn on which turns on T_2. (It is noted that there is a V_{BE}

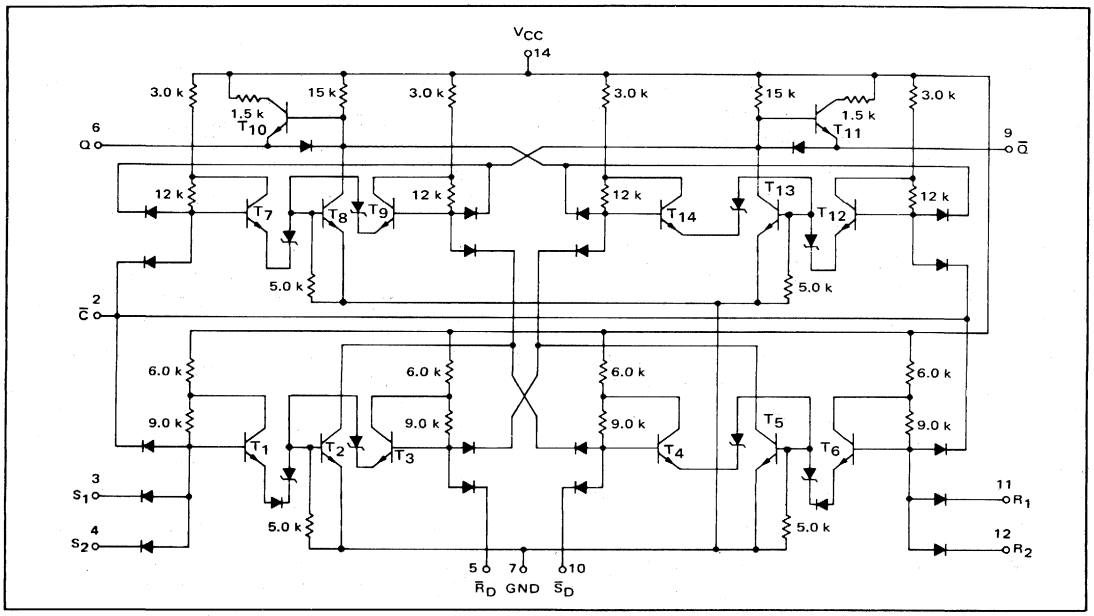


FIGURE 3C – CIRCUIT SCHEMATIC MC664P

diode offset between the master and slave sections of the flip-flop and it is essentially a dc rise time circuit.) Transistor T_2 turning on causes T_9, T_4 and T_5 to turn off. Transistor T_8 remains on, however, due to the second source of base current from T_7. Transistor T_5 being off causes T_3 to turn on and now T_2 is provided with base current from two sources. A continuing increase of the clock input will not cause any further changes in the flip-flop. As the clock potential starts to decrease, T_1 will turn off first although T_2 remains on due to the second base current source. When the clock potential falls an additional V_{BE} drop, T_7 and T_8 turn off and the Q output goes high. This high potential coupled with T_5 being off turns on T_{14} and T_{13} and the $\overline{Q}$ output goes low generating the changed flip-flop state. The conditions of the flip-flop will now remain the same for any further decrease in the clock potential. A similar action would return the flip-flop to the original state if R_1 and R_2 were high or open with S_1 and/or S_2 at the low level and a clocking waveform applied. Although information may be reliably applied to the flip-flop with essentially dc-risetime clock-waveforms, there is a point where the output rise and fall times are beta dependent on the clock level. This will increase the output transition times when excessively slow clock-waveforms are present.

The flip-flop state may be changed by use of the $\overline{R_D}$ and $\overline{S_D}$ terminals. If the condition is considered where Q = 0, $\overline{Q}$ = 1, $\overline{C}$ is low, and both $\overline{R_D}$ and $\overline{S_D}$ are high as in the preceding example, it can be observed that a momentary low on $\overline{S_D}$ will set the flip-flop to Q = 1, $\overline{Q}$ = 0. In this instance when $\overline{S_D}$ goes low, T_4 and T_5 turn off which causes T_3 and T_2 to turn on. With T_2 on, T_9 and T_8 turn off and the Q output goes high. This high potential coupled with T_5 being off, turns on T_{14} and T_{13} causing $\overline{Q}$ to go low completing the transition. Similar action results if the flip-flop were in the Q = 1, $\overline{Q}$ = 0 state and a momentary logical zero were placed on the $\overline{R_D}$ terminal.

A toggle mode of operation may be achieved with the flip-flop by connecting the Q output to one of the R inputs and the $\overline{Q}$ output to one of the S inputs. Under this condition, the truth table for synchronous operation of the MC663P would also apply to the MC664P by redefining the S input as the J and the R input as a K.

Power dissipation for this unit is typically 140 mW with V_{CC} = 15 V. Typical characteristics of parameters as a function of temperature are given in Figure 4A and 4B.

APPLICATIONS

Operation of the MC664P master-slave flip-flop is very similar to the MC931/831 flip-flop operation in the MDTL family. This fact, coupled with similar gate operation between the two families, allow construction of MHTL shift registers, counters and decoders in much the manner described in application notes covering the MDTL family (e.g., AN-235, 262, 283 and 284). The MC663P may be employed to take advantage of the dual function in many shift register and counter circuits, but with only the direct reset function available, parallel input operation is not as flexible as with the MC664P. Since the MC663P operates on a stored charge principle and different modes of operation may be obtained, the devices may be easily interconnected to form gateless ripple counters. Figure 5 illustrates several counters that may be constructed with a maximum

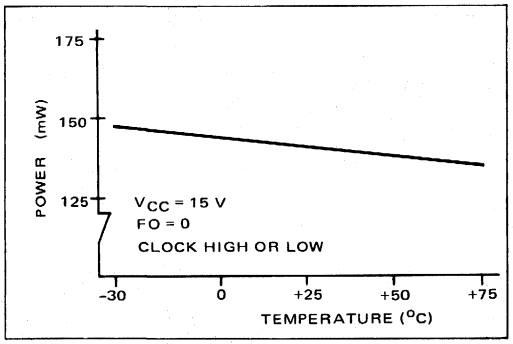


FIGURE 4A – TYPICAL MC664P POWER DISSIPATION versus TEMPERATURE

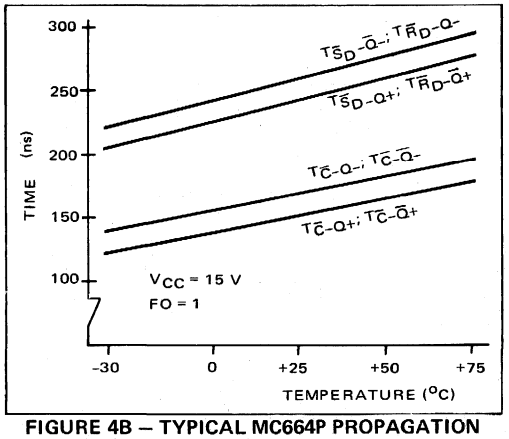
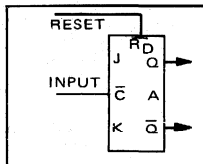


FIGURE 4B – TYPICAL MC664P PROPAGATION DELAY TIMES versus TEMPERATURE

of 2 MC663P Packages. It should be noted that direct resetting of these counters is independent of the clock level, consequently the reset time of any counter equals the reset time of a single flip-flop. The logic sequence and maximum signal ripple for each circuit is also provided in the figure.

In Figure 6, a decade shift counter is constructed using 2 MC663P units and an MC664P for proper input gating. Typical waveshapes are illustrated for this connection and the necessary decoding logic is provided.



MAX RIPPLE–1

÷2

STATE	Q_A
1	0
2	1

MAX RIPPLE–2

÷3

STATE	Q_A	Q_B
1	0	0
2	1	0
3	0	1

MAX RIPPLE–2

÷4

STATE	Q_A	Q_B
1	0	0
2	1	0
3	0	1
4	1	1

MAX RIPPLE–3

÷5

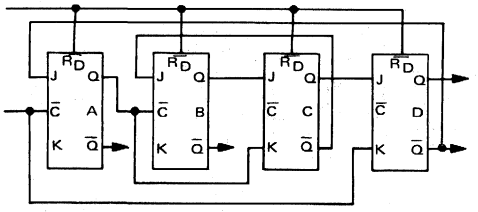
STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1

MAX RIPPLE–3

÷6

STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1

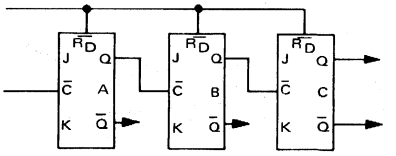
FIGURE 5 – GATELESS RIPPLE COUNTERS FROM MC663P DEVICES



MAX RIPPLE–3

÷7

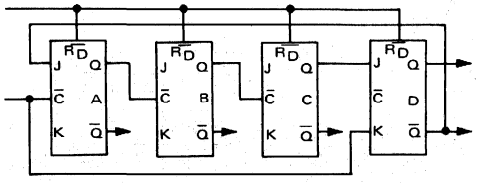
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	0	0	1



MAX RIPPLE–3

÷8

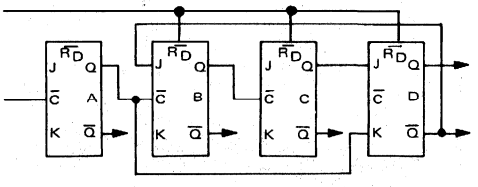
STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1



MAX RIPPLE–4

÷9

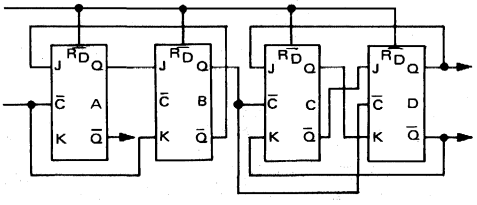
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1



MAX RIPPLE–4

÷10

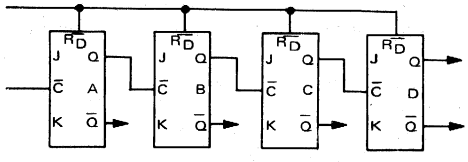
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1



MAX RIPPLE–2

÷12

STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	0	0	0	1
5	1	0	0	1
6	0	1	0	1
7	0	0	1	1
8	1	0	1	1
9	0	1	1	1
10	0	0	1	0
11	1	0	1	0
12	0	1	1	0



MAX RIPPLE–4

÷16

STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

FIGURE 5 – (continued)

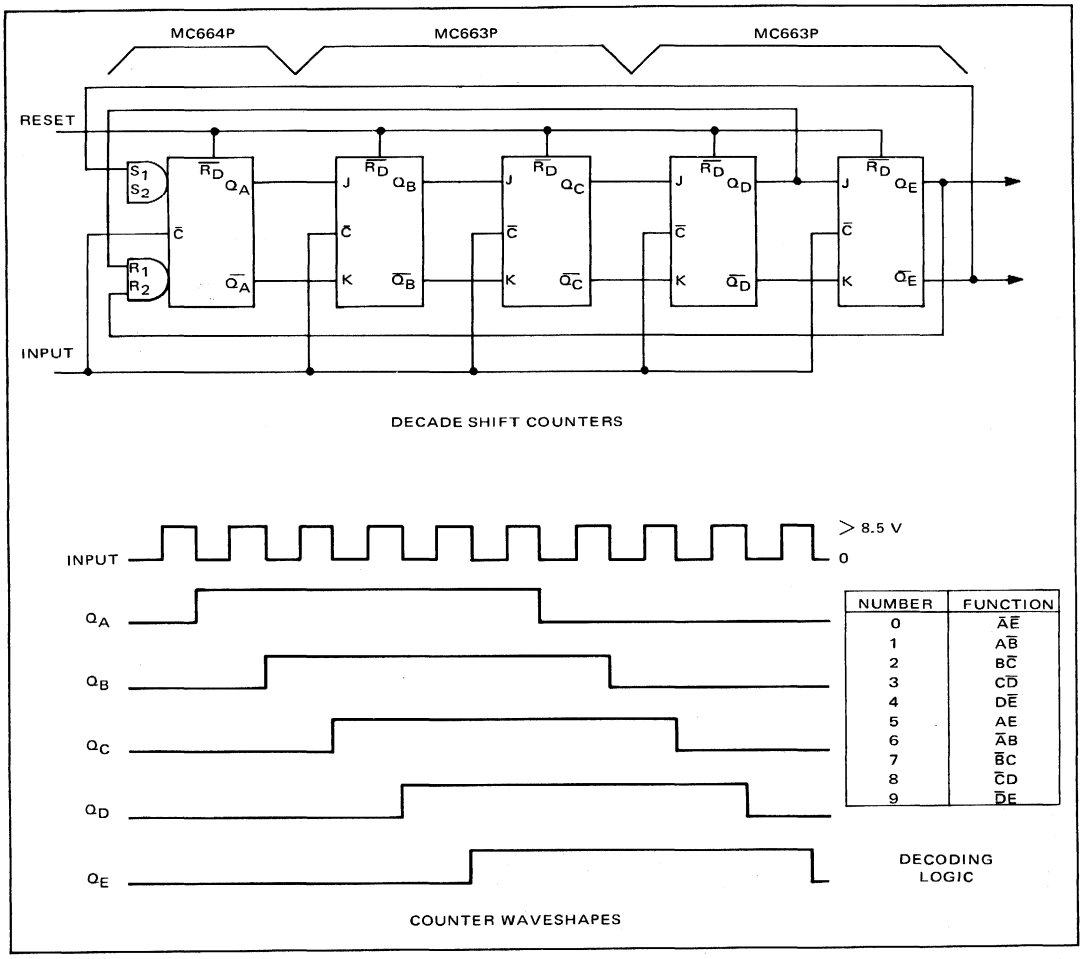


FIGURE 6 – DECADE SHIFT COUNTER AND COUNTER WAVESHAPES

CONCLUSIONS

The initial flip-flops in the MHTL family provide considerable flexibility for the design of digital electronic equipment to operate in environments subject to electrical noise. Some typical applications have been illustrated for usage of these MHTL flip-flops. In addition, a detailed explanation of operation of the devices has been given to help design the units into special applications.