# Direct-Coupled Transistor Logic Circuitry*

J. R. HARRIS†

*Summary*—**Direct-coupled transistor logic circuitry lends itself to systematic design methods and performs remarkably well. Logical design rules are given for use with transistors which meet specifications treated in a companion paper. The implications of the use of silicon transistors are discussed.**

## Introduction

THE CONCEPT of direct-coupled transistor circuitry as a sufficient system for digital computers was introduced by Beter, *et al.*,[1] in March, 1955. The present paper touches on several aspects of direct-coupled transistor logic circuitry (dctl) as follows: what it is, why it works so well, a method of approach for the design of dctl systems, and how a system works when designed this way.

## What It Is

At the top of Fig. 1 is a flip-flop, quite conventional, shown for reference. Below it is a direct-coupled flip-flop; it has no voltage dividers made from resistors, and there is only a single voltage supply. Still, it acts like the conventional flip-flop with one transistor off and one on. The right-hand transistor is on because its base gets nearly all the current from the left resistor. Because it is on, its collector voltage is low, something like 50 mv. This 50 mv is applied to the left base. It is a positive voltage[2] (as are all static voltages in the system) and so is of the opposite polarity to what one would desire to turn off completely, the left transistor. Even so, it is sufficiently near ground, or one might say sufficiently negative, to keep the left transistor effectively off.

The current that flows in a resistor is very nearly constant, regardless of whether the dctl flip-flop is in one state or the other state or changing state. This comes about because of the extremely small range of voltage on a node. In the state shown, the left-hand resistor supplies current to the right base plus some leakage current in the left collector. If the flip-flop were in the other state, the left-hand resistor would furnish collector current for the left stage; the base current of the right transistor, now off, would be negligible.

## Why It Works

In order to show why the system works well, several points deserve mention.

1) A transistor can be an excellent (though not perfect) closed switch. Ideally, the right collector in Fig. 1 should go to zero volts, or, even better, to a slight negative voltage in order to shut off the left transistor. Actually, a transistor collector cannot provide zero volts, but it can provide 50 mv or so of positive voltage, which is adequately near zero.
2) When a transistor in a dctl circuit is nominally off, it is actually in the edge of the active region. Its collector current (desirably very low) can be thought of as the collector diode reverse current $I_{co}$ multiplied by a factor involving alpha, the current gain. Transistors are designed to have a high alpha in the active region. This might be expected to result in excessively large collector currents in the nominally off condition. Fortunately, it is generally found that alpha drops to a low value at the low-current edge of the active region. For a typical germanium-alloy transistor, the collector current is reduced by a factor of five to ten because of the reduced alpha at low currents.
3) Nature is favorable in permitting a rapid switch-off. A reverse base current is desirable for fast switch-off.[3,4] With a power supply of only one polarity, it might seem that reverse base current is not possible. However, if the circuit is examined carefully, the emitter diode within the transistor being turned off is found to have voltage across it; this voltage has the proper polarity to drive reverse base current. It may be noted that the reverse base current cannot exceed the value set by the diode voltage (some 200 mv for germanium), and the internal base resistance of the transistor is turned off. Early in the process of switch-off, the voltage on the emitter diode arises from the flow of collector current. Even after this current ceases to flow in the emitter diode, the diode can maintain voltage of the proper sign because of a "memory" of the flow of forward current.
4) Collector leakage current in germanium transistors becomes undesirably high at high temperature, especially with the forward base bias voltage of a dctl system. However, it is found that this

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[1] R. H. Beter, W. E. Bradley, R. B. Brown, and M. Rubinoff, "Surface-barrier transistor switching circuits," 1955 IRE Convention Record, pt. 4, pp. 139–145.

[2] All voltages would be negative in a system using *p-n-p* transistors.

[3] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," Proc. IRE, vol. 42, pp. 1761–1772; December, 1954.

[4] J. L. Moll, "Large-signal transient response of junction transistors," Proc. IRE, vol. 42, pp. 1773–1784; December, 1954.

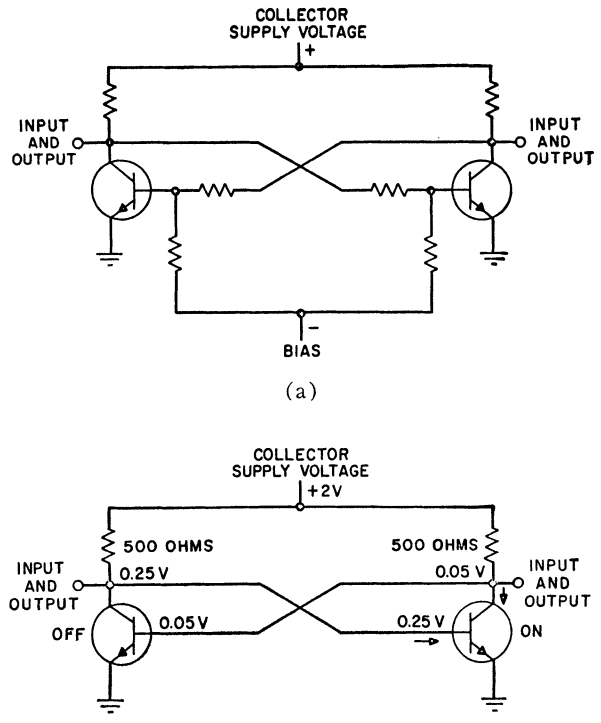


Fig. 1—(a) Simple Eccles-Jordan flip-flop, (b) dctl flip-flop.

effect is less severe in dctl than might be expected. The reason for this is that the forward base bias voltage (which is the collector voltage of an ON transistor) tends to be reduced at high temperature. It appears that the ON collector voltage of germanium-alloy transistors goes down at high temperature because of an increase in alpha.

5) A prime problem of reliability is the fact that some transistors show an increase of collector leakage current with age. In cases where this current has become quite high, it is usually found that the collector current has become strongly dependent on collector voltage. A transistor which has intolerable leakage current at ordinary voltages (*e.g.*, 4.5 volts) is likely to work the same as its well-behaved brothers in a dctl circuit with its inherently low collector voltage. This fact is considered added insurance; the drive toward wholly reliable transistors must not be relaxed.

## An Approach to the Design of a DCTL System

A more complete system is shown in Fig. 2. Note the flip-flop, two circuits (one a two-level series circuit) which drive it, and three circuits which might be considered to be driven by it. This system works as follows: suppose the left transistor of the flip-flop is OFF and the right ON. Now, if the single level driver, or both the upper and lower series drivers, become ON, then point $X$ will approach ground, the right transistor of the flip-flop will go OFF, and finally, the left transistor will go ON.

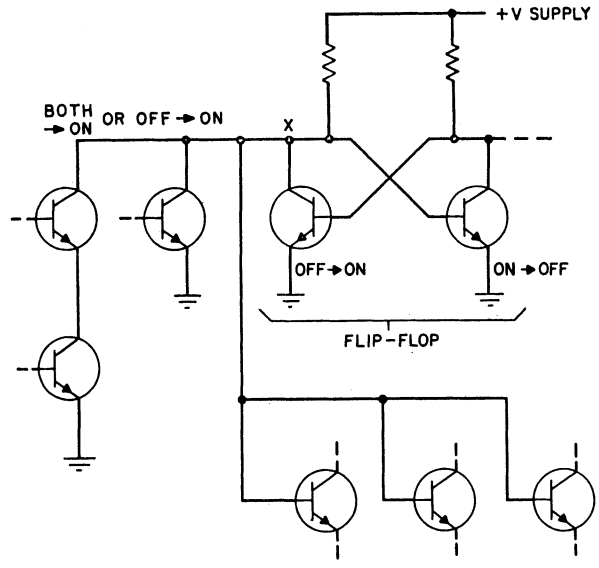


Fig. 2—A typical dctl circuit.

## Logical Design Rules and Transistor Requirements

In a configuration like this, the questions arise, "How many transistors can a flip-flop drive?" "How many transistors can be used to drive a flip-flop?" and so on. For convenience the questions will be put in a different form. Note that the transistors in the flip-flop seem to be connected very nearly like the other transistors of the system. In our experience, no good reason has been found for associating a current supply resistor with a flip-flop any more than with the other transistors. It is to be noted that a resistor feeds only collectors and bases. Accordingly, the question to be answered is just this: "How many collectors and bases can be connected to a resistor?" The answer can be thought of as rules for logical design.

To pursue an answer, consider Fig. 3. Here are what may be thought of as successive stages of transistors, which may or may not be a part of a flip-flop. For simplicity, assume that *all* the current-supply resistors are of the same nominal value and depart from this policy only for good reason. (It appears that a single value is practical.)

The currents in Fig. 3 are intended to represent a worst combination of resistor tolerances. The aim is to assure that a transistor will stay OFF when it should be OFF and ON when it should be ON, with a very *worst* pileup of all conditions. This will be referred to as "stability." How can this be assured? Referring to Fig. 3, one can say in general that the current needed by the bases on a node, plus the leakage current of the collectors on that node, must not exceed the current the resistor supplies (in this case 3.5 ma).

Something can be said now about what kind of transistor is desired. It is one with low collector leakage current; one that gives low $V_{CE}$ with a minimum of current feeding an array of bases in parallel and, of course, one

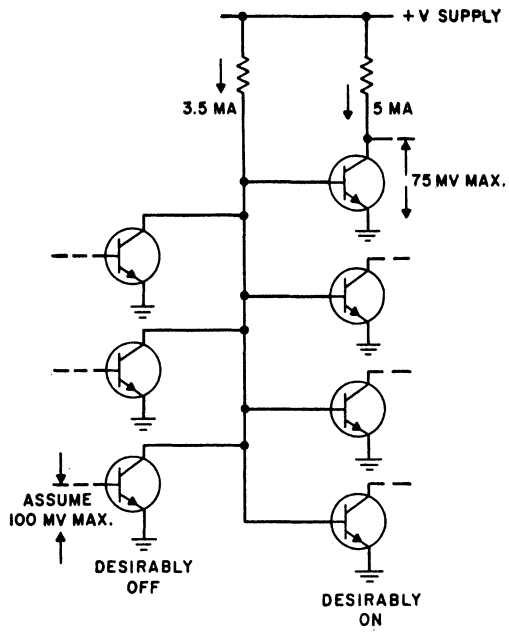


Fig. 3—The problem of static stability.

that is fast enough. Easley[5] describes a set of transistor specifications which, in combination with a proper set of logical design rules, are necessary and sufficient for stability.

### An Example of Logical Design Rules

The basic logical design rule we have used for germanium-alloy transistors states merely that the total number of collectors and bases on a node shall not exceed seven. (This applies to all collectors and to bases of transistors in single-level circuits.) Derivation of this rule will now be outlined with the help of Fig. 3. It is the intention that no collector leakage current on the left exceed 0.5 ma at 40°C. (One would like to put a lower value on the current, thus broadening the logical design possibilities, and a higher value on the temperature, but to do either would demand unreasonably tight specifications on the transistor.) To assure the stated low leakage, the forward bias on a left base should never exceed 100 mv. To assure the 100 mv or less in the presence of noise, an ON stage which would drive one of the bases on the left should not exceed a $V_C$ value of 75 mv. Similarly, one should be sure that no collector on the right exceeds 75 mv. The transistor specification is arranged to assure that the latter will be true if the mathematical average per-base drive is 0.5 ma. Thus, the most "allowance" a base or collector will need is 0.5 ma. Therefore, a total of seven bases and collectors can be connected to a node.

If one of the circuits on the right in Fig. 3 were a series circuit, 75 mv (or less) on the top collector would still be needed. With a two-level series circuit, this represents only 37.5 mv per transistor. Assuming typical high-frequency germanium-alloy transistors, this can be expected to require about two and a half times as much base drive current allowance for *every* base on a node driving a series circuit, that is, 1.25 ma per base.

### Choice of Current Level

There are several circuit reasons for using a relatively low node-supply current, and several circuit reasons for using a relatively high current. It appears that a node current of about 4 ma is quite a good compromise for germanium-alloy transistors.

Considerations that urge the choice of a low current are:

1) To minimize power-supply current.
2) To minimize the effect of ohmic transistor resistances $r_c'$, $r_e'$, and $r_b'$. One effect of $r_b'$ is to slow the turnoff of the transistor in question. Low current acts in a rather back-handed way to minimize this $r_b'$ effect, as follows. The transient reverse base current may be somewhat independent of the node current; its maximum value is fixed by $r_b'$. A low node-current means a low forward base current and low collector current when a transistor is on, which, with a relatively fixed value of transient reverse base current, results in faster turnoff.

Considerations that urge the choice of a high current are:

1) To minimize the effect of capacities on switching time. (Usually a small effect.)
2) To minimize the effect of collector leakage current.
3) To reduce the variation of base currents among bases connected in parallel.[6]
4) To avoid the loss of current gain that occurs in some transistors, particularly certain silicon types, at low current levels.

### Crosstalk Problems

In any switching system, it is to be expected that normal operation will produce pulses of current in the ground system. In a high-speed system, fast rising pulses will produce voltage differences in the ground system because of ground inductance. If these voltages interfere with parts of the system, we can say that we have crosstalk, or noise trouble. One of the problems arising from crosstalk is illustrated in Fig. 4. The circuit drawn here is a part of a dctl system, that, for the moment, must stay in the state shown if the system is to work right. It can be thought of as a crosstalk receiver. Imagine that there is a bank of transistors grounded on the left side, driving a bank that is grounded on the right side. These are the crosstalk generators. When these generators switch, a pulse of current appears in the ground conductor and develops a voltage because of ground inductance. This voltage can, of course, be of

[5] J. W. Easley, "Transistor characteristics for direct-coupled transistor logic circuits," this issue p. 60. See (25) and (26); also (23) and (24).

[6] *Ibid.*

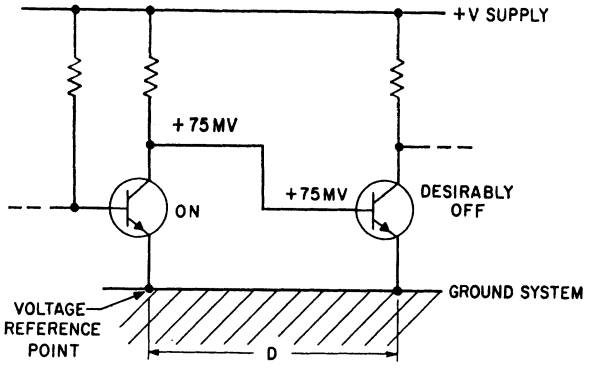


Fig. 4—The crosstalk problem.

either polarity. If the right end of the ground goes negative, the right transistor shown will tend to turn on falsely.

In one experiment, ten surface barrier transistors at the left end drove ten at the right end of a ground plate 14 inches long ($D=14$ inches) and 5 inches wide. Total current switched was 60 ma and a noise pulse of 40 mv and 0.2 μsec was generated. At 40°C, this is considered to be enough to begin to turn on (falsely) a surface-barrier transistor which has a static base voltage of 75 mv. Germanium-alloy transistors of 7 to 10-mc alpha cutoff frequency were found to generate ground noise about 1/10 the amplitude and ten times the duration of surface-barrier units.

Fortunately, a false signal, even though it propagates, would generally reach a stage that is heavily saturated. Being very brief, the false signal would not turn off the saturated stage, and would propagate no further. However, for best reliability, it seems desirable to make sure that *no* stage switches falsely. To achieve this, our approach has been to minimize ground inductance by mounting transistors very close together.

Where it is necessary to use so many transistors that the ground inductance becomes too large, the total is split into "islands," each of which has tolerably low ground inductance. Since the noise is developed on the ground inductance, and the ground resistance is negligible, the noise amplitude drops off at low frequencies. Accordingly, a low-pass filter can be used in the signal path between islands to attenuate noise. A heavily saturated transistor at the proper place in the signal path has been used for this purpose.

Silicon transistors have the possibility of tolerating a great deal more noise than germanium transistors without false turnon. This is because a silicon transistor requires a great deal of forward base voltage to give excessive collector leakage current—in the neighborhood of 650 mv at room temperature and 350 mv at 75°C.

A second effect of noise must be considered, namely, false turnoff. Where bases are connected in parallel, noise applied between the respective emitters will cause an unbalance of base currents, the bad effect being the reduction of one or more base currents. The effect can be studied in detail by noting that the noise adds to or subtracts from the transistor parameters $V_{B1}$ and $V_{B2}$ defined by Easley.[6] Storage time in transistors reduces this effect, and the effect has not been taken into account directly in the system design to be described.

## How One System Works

The rules mentioned were used to build a counter, register, and parity-check system for a core memory, with 800 transistors. In this system, 400 germanium-alloy transistors are mounted on each of two ground plates. The transistors used are Radio Receptor type RR163 (see Appendix). The $V_{B1}$ and $V_{B2}$ specifications of the RR163 have a safety margin (perhaps larger than necessary) to take care of measurement error; the margin will be seen to be 20 mv. These transistors have a minimum alpha cutoff frequency of 7 mc. It is found that signals propagate at about 0.5 μsec per stage, in general agreement with the Ebers-Moll theory.[3,4] The noise in this system is acceptably low.

Perhaps the most interesting aspect of this system is its supply voltage margins. The single supply voltage (nominal 2 volts) can be varied from 0.4 to at least 13 volts. However, changing the single supply voltage does not necessarily show up a weak component because the current ratio (input and output of a stage) tends to remain constant. How can a weak component be found? One can set up, insofar as possible, to feed resistors of alternate stages from a separate supply, and then vary the separate supply; then the current ratio of an individual stage changes so that it becomes heavily saturated or else lightly driven. When this is done, the margins are found to be 1.25 volts to 3.45 volts. It appears that these margins are usually set by transient behavior, by transistors becoming too slow.

The power dissipation of the entire 800 transistors is about 0.25 watt. The power required from the power supply is about 3 watts, most of which is, of course, dissipated in the resistors of the system.

Another piece of equipment built with the same transistors and the same logical design rules was a word generator. In temperature tests of this unit, which uses 119 transistors, operation was satisfactory over a range exceeding −50°C to +65°C. The upper temperature limit was set by the circuits slowing down due to an increase in "hole storage." The fact that the design temperature of 40°C could be exceeded so much is an indication of the size of the safety factor that results from the approach of designing for the most adverse logical design conditions (such as a maximum number of bases on a node) together with a most adverse pileup of component tolerances.

More recently, a complete computer (Leprechaun) has been built[7] using the logical design rules and the form of transistor specification described herein.

[7] J. A. Githens, "The Tradic Leprechaun computer," *Proc. Eastern Joint Computer Conference*, AIEE Special Publication T92, p. 29; December 10–12, 1956.

## Conclusion

The object was to evolve design rules for dctl which would assure proper switching and freedom from crosstalk noise trouble under some worst pileup of conditions. By grouping many transistors together on a very small ground plate, and using special circuits between ground plates, crosstalk noise appears tractable. Proper switching can be assured by 1) rules restricting the number of bases and a collectors on a node and 2) the use of transistors which meet a specification evolved for dctl.

## Appendix

### Electrical Specification—Radio Receptor RR163—July 26, 1955

All values appropriate to measurements at room temperature (25°C).

1) $f_\alpha(V_{CB}=-1.5\text{v}, I_c=-1\text{ ma})\geq 5$ mc
   $f_\alpha(V_{CB}=-6, \quad I_c=-1\text{ ma})\geq 7$ mc.

2) $C_c(V_{CB}=-6)\leq 25$ mmf.

3) Storage time[8]

$T_1(I_c=-5\text{ ma}, I_{B1}=-0.5\text{ ma}, I_{B2}=0.5\text{ ma}) \leq 0.5\ \mu\text{sec}.$

4) $|I_c|(V_B=V_E=0,\ V_c=-1.5\text{v})\leq 5\mu\text{a}.$

5) $|V_{B1}|_{\min}\geq |V_{B2}|_{\max}+0.02\text{v},$

where the subscripts min and max indicate the minimum acceptable absolute value of $V_{B1}$ and the maximum acceptable absolute value of $V_{B2}$ for a given transistor type. $V_{B1}$ and $V_{B2}$ are defined as follows.

$$V_{B1}=V_{BE}(I_c=-5.0\text{ ma}, I_B=-0.5\text{ ma})$$

$$V_{B2}=V_{BE}(I_c=-5.0\text{ ma}, V_c=-75\text{ mv}).$$

For the RR163, $|V_{B1}|_{\min}=220$ mv, $|V_{B2}|_{\max}=200$ mv.

6) Punch-through voltage, not less than 5 volts.

[8] For definition of $T_1$, $I_{B1}$, and $I_{B2}$, see Moll, *op. cit.*

# Transistor Characteristics for Direct-Coupled Transistor Logic Circuits*

JAMES W. EASLEY†

***Summary*—The basic requirement for stability of a direct-coupled transistor logic (dctl) circuit is that a voltage margin exist between the maximum collect-emitter voltage of an "on" unit in the system environment and the minimum base-emitter voltage required for a transistor to be sufficiently "off." This margin has been expressed in terms of the fundamental device parameters: common-base forward and inverse current gain, $\alpha_N$ and $\alpha_I$; ohmic body resistances of the emitter, collector, and base regions, $r_e'$ and $r_c'$, $r_{bIII}$; collector saturation current, $I_{CO}$; and the ratio of the value of $\alpha$ in the vicinity of the "off" state to its value in the vicinity of the "on" state.**

**In addition, the connection of bases in parallel results in a dependence of stability on the magnitude of $\alpha_I$ and of $r_{bIII}$ and on the variations of $\alpha_N$, $\alpha_I$, $r_{bIII}$, and $I_{CO}$ among units connected in this manner. Circuit stability requirements have been expressed in terms of these parameters and the effect of their variations is considered.**

**Methods for the specification of acceptance requirements for dctl transistors and the relation of these specifications to logic design rules are discussed.**

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## I. Introduction

THE design and performance of direct-coupled transistor logic circuits of the type described by Beter, *et al.*,[1] depend to a large extent on the characteristics of the transistors employed. It is reasonable to consider that the circuit elements which are interconnected to form a switching system are the transistors themselves; consequently, the emphasis is shifted from the study of circuit elements such as amplifying stages and bistable circuits to the study of transistor characteristics. It is therefore of interest to relate the circuit variables which are significant in circuit design to transistor parameters, particularly to those which may be related in turn to the physical structure of the transistor through existing design theory.[2]

[1] R. H. Beter, W. E. Bradley, R. B. Brown, and M. Rubinoff, "Surface-barrier transistor switching circuits," 1955 IRE Convention Record, pt. 4, pp. 139–145.

[2] For example, J. M. Early, "Design theory of junction transistors," *Bell Sys. Tech. J.*, vol. 32, pp. 1271–1312; November, 1953.