APPENDIX 2

SIMPLIFIED DESIGN PROCEDURE FOR BISTABLE CIRCUITS

DESIGN OF A BISTABLE CIRCUIT FOR USE AT HIGH FREQUENCIES

The simplified design procedure in this appendix relates to the type of circuit shown in Fig. 170. Speed-up capacitors and recovery diodes are included in this diagram, but their effects on the operation of the circuit will not be discussed until after the basic design procedure.

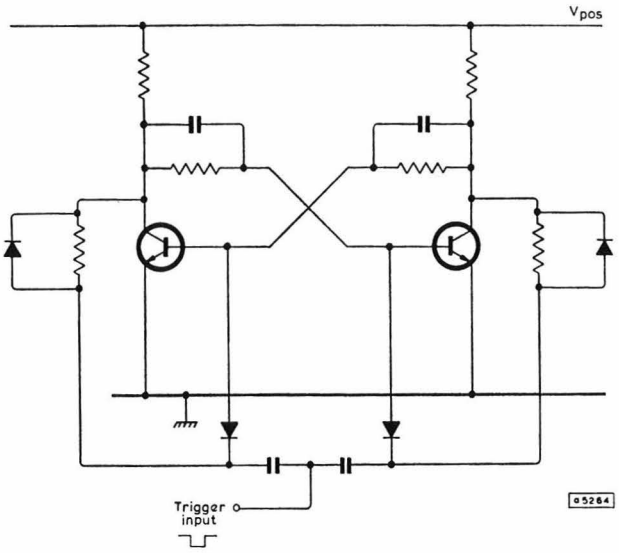

Fig. 170—Bistable circuit

D.C. Conditions

A bistable circuit is shown in Fig. 171. Circuits of this type are normally symmetrical; that is, the two base resistors are equal and the two collector resistors are equal. The value of the collector resistor depends, in practice, upon the external loading. For the purposes of this explanation, R_{cH} will be used to denote the maximum value of R_c—normally the value which is effective in the OFF state—and R_{cL} will be used to denote the effective collector load in the ON state; that is, when current is being supplied to external loads. If TR_2 is

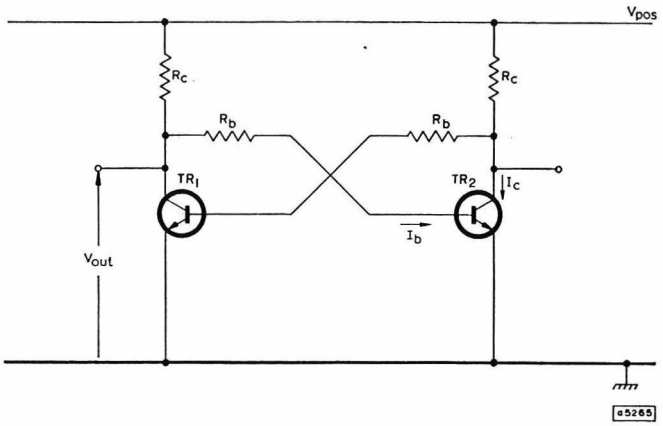

Fig. 171—Bistable circuit showing d.c. conditions

assumed to be conducting, the output voltage at the collector of TR_1 is given by

$$V_{out(high)} = \frac{(V_{pos}-V_{BE})R_b}{R_b+R_{cH}} + V_{BE}$$

or

$$V_{out(high)} = V_{pos} - \frac{(V_{pos}-V_{BE})R_{cH}}{R_{cH}+R_b}. \qquad \ldots(19)$$

For TR_2 to remain in saturation, the value of the collector current is given by:

$$I_c = \frac{V_{pos}-V_{CE\ (sat)}}{R_{cL}}, \qquad \ldots(20)$$

and the base current is given by,

$$I_b = \frac{V_{pos}-V_{BE}}{R_{cH}+R_b}. \qquad \ldots(21$$

The minimum gain that can be tolerated is given by:

$$h_{FE(sat)} = \frac{I_c}{I_b}, \qquad \ldots(22)$$

and therefore, by substituting Eqs. 20 and 21 in Eq. 22;

$$h_{FE(sat)} = \frac{(V_{pos}-V_{CE(sat)})(R_{cH}+R_b)}{(V_{pos}-V_{BE})R_{cL}}. \qquad \ldots(23)$$

The value of $h_{FE(sat)}$ obtained from Eq. 23 is the minimum value required to keep the transistor in saturation. In practice, however, to obtain maximum speed of operation, base overdrive is normally used. The base overdrive factor is usually between 2 and 5, but if the overdrive factor is γ, the minimum value of $h_{FE(sat)}$ is given by:

$$h_{FE(sat)} = \frac{\gamma(V_{pos}-V_{CE(sat)})(R_{cH}+R_b)}{(V_{pos}-V_{BE})R_{cL}}. \qquad \ldots(24)$$

The choice of suitable values for operating current and load resistors depends upon several factors.

(1) The transistor should be in a high gain region of its characteristic over the whole range of operating current—from no load to full fan-out.

(2) The value of R_c affects the speed of operation because the collector voltage rise time is partly determined by this resistance.

(3) The operating current may need to be kept low to limit the power consumption and dissipation.

In the example considered here, it is assumed that the design is for a fast counting bistable circuit using BSX20 transistors, or BSX19 transistors when a lower fan-out is required. The supply voltage is assumed to be +6V. The BSX19 and BSX20 transistors have maximum gain at currents between 7 and 15mA. In this example, it is assumed that the bistable circuit is required to drive gates which could require a total current of 15mA and that it is capable of driving further similar bistable circuits.

To obtain a short voltage rise time at the collector, the value of R_c should be low. Too low a value, however, would cause the transistor to operate at a high current where the gain is reduced, particularly with full fan-out loading. Operation at too low a current—for example, 1mA—increases the collector voltage rise time and therefore limits the speed of operation, in spite of the fact that the transistor has sufficient gain at 1mA. For this condition, the collector load would be a maximum of 6kΩ and, if C_{tc} has a value of 4·5pF and the stray capacitances a further 5pF, the collector time-constant is 57ns which is too long for operation at frequencies of 5 to 10MHz. To maintain the operating speed, therefore, a compromise must be found.

In this example, a no-load collector current of 5mA is assumed, giving a value of 1·2kΩ for R_c and a collector time-constant of about 12ns. The total operating range of collector current is then from 5 to 20mA over which range the transistor has a high gain. The minimum output voltage from the stage is required to be 4V. The outline specification of the bistable circuit is summarised in Table 79.

TABLE 79

Outline Specification of Bistable Circuit

V_{pos}	=	+6V
$V_{CE(sat)}$	=	0·1V
I_c (unloaded)	=	5mA
Fan-out current (min)	=	15mA
Output voltage (min)	=	4V
Base-emitter voltage	=	0·7V
Counting speed (min)	=	10MHz
Resistor tolerances	=	±10%

The specification given in Table 79 enables values to be substituted in the equations obtained earlier in this appendix.

Calculation of R_{cH}
The value of R_{cH} is given by

$$R_{cH} = \frac{V_{pos} - V_{CE(sat)}}{I_{C(no\ load)}},$$

therefore

$$R_{cH} = \frac{5{\cdot}9}{5} \simeq 1{\cdot}2k\Omega.$$

Calculation of R_{cL}
From Eq. 20

$$R_{cL} = \frac{V_{pos} - V_{CE(sat)}}{I_{c(max)}},$$

therefore

$$R_{cL} = 0{\cdot}3k\Omega.$$

Calculation of R_b
Rearrangement of Eq. 19 gives

$$R_b = R_{cH}\left[\frac{V_{pos} - V_{BE}}{V_{pos} - V_{out(high)}} - 1\right]. \qquad \ldots(25)$$

Therefore, by substituting in Eq. 25 with R_{cH} at its highest value within the specified tolerance

$$R_{b(min)} = 1{\cdot}32\left[\frac{6-0{\cdot}7}{6-4} - 1\right]$$
$$= 2{\cdot}17k\Omega$$

The minimum preferred value that can be used is 2·7kΩ, with a range of 2·43 to 2·97kΩ.

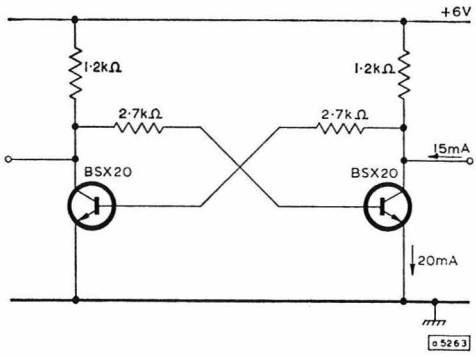

Fig. 172—D.C. circuit of bistable example

Calculation of Overdrive Factor

From Eq. 24

$$\gamma = \frac{h_{FE(sat)}(V_{pos}-V_{BE})R_{cL}}{(V_{pos}-V_{CE(sat)})(R_{cH}+R_b)}$$

The maximum values of R_{cH} and R_b are 1·32kΩ and 2·97kΩ respectively, and the minimum value of h_{FE} for a BSX20 transistor is 40. Therefore the minimum value of γ is given by

$$\gamma = \frac{40(6-0{\cdot}7)0{\cdot}3}{5{\cdot}9(1{\cdot}32+297)}$$
$$= 2{\cdot}49$$

The maximum overdrive factor with a value of h_{FE} of 120 is 7·35.

The basic d.c. circuit of the bistable element is shown in Fig. 172.

A.C. Conditions

The basic d.c. circuit, with the addition of triggering and steering elements, is shown in Fig. 173. BAX13 diodes are used because of their high operating speed.

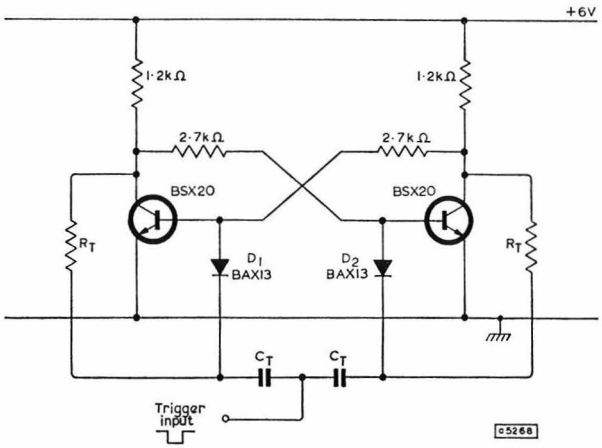

Fig. 173—Basic triggered bistable circuit

For the bistable element to be used as part of a counting circuit, it must be capable of being triggered from the output of a similar stage; that is, by a minimum voltage of 4V. However, in counting circuits using feedback or feed-forward, the trigger input may be fed via gating circuits across which a voltage drop occurs. For the purpose of this example, a minimum triggering voltage of 2·5V is assumed.

If the input pulse has a very fast negative-going edge, C_T need only be sufficiently large to turn the conducting transistor off with a 2·5V input, and to hold it off for at least the desaturation time of the transistor. From the published

data for the BSX20, the total turn-off time is 18ns when I_c is 10mA, I_b (on) is 3mA and I_b (off) is $-1{\cdot}5$mA. In the circuit derived so far, the maximum forward base current is 1·5mA and the worst case for speed consideration is when this base current is used with the minimum collector current of 4·5mA; that is, with the device heavily in saturation. In this case the effective value of h_{FE} is 3. Provided that C_T supplies sufficient reverse base current, the turn-off time may be expected to be less than 18ns.

When the input voltage falls, either D_1 or D_2 conducts. Thus, with a negative pulse of 2·5V on the input terminal, the transistor base potential falls from $+0{\cdot}7$ to $-1{\cdot}8$V. Capacitor C_T must now absorb the 1·5mA base current from the coupling resistors and must provide a reverse base current of at least 1·5mA. The current flowing through C_T during turn-off is therefore about 3mA. The voltage on C_T must not rise by more than 30% during the turn-off time, because if it did, the turn-off current would not be maintained and the turn-off time would be increased. The value of the charge, Q, is given by:

$$Q = I \times t,$$

therefore

$$Q = 3 \times 10^{-3} \times 18 \times 10^{-9} \text{ coulombs}$$
$$= 54\text{pC}$$

The change in voltage on C_T has been assumed to be less than 0·66V.

Now the value of C is given by

$$C_T = \frac{Q}{V},$$

therefore

$$C_T = \frac{54 \times 10^{-12}}{0{\cdot}66} \text{ farads}$$
$$= 82\text{pF}.$$

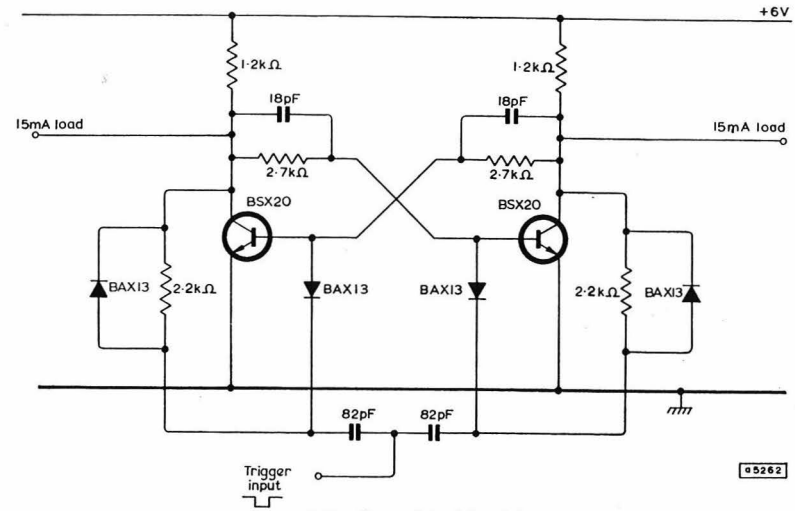

Fig. 174—Complete bistable circuit

Capacitor C_T must be able to discharge through R_S in two count periods. Therefore, for an operating frequency of 10MHz, the time-constant C_TR_T should be less than 200ns if maximum trigger sensitivity is to be maintained. Therefore;

$$R_T = \frac{200 \times 10^{-9}}{82 \times 10^{-12}} \Omega$$
$$= 2{\cdot}43k\Omega$$
$$\simeq 2{\cdot}7k\Omega.$$

To conduct the positive edges of the trigger pulses away, diodes are connected across R_T. The value of speed-up capacitance is usually between 10 and 20% of the triggering capacitance. Speed-up capacitors of 18pF provide rapid turn-on, and add little to the triggering voltage requirements. The complete circuit is shown in Fig. 174 and the measured performance is given in Table 80.

TABLE 80

Measured Performance of Bistable Circuit

Maximum counting frequency (no load)	=	25MHz
Maximum counting frequency (resistive load, I_{load} = 15mA; triggering voltage = 4V)	=	30MHz
Minimum trigger input (capacitive load, load capacitance $\leqslant$100pF, I_{load} = 15mA, f = 1MHz)	=	1·7V
Maximum input fall time (amplitude = 2·5V, f = 1MHz)	=	50ns
Output fall time	=	15ns
Maximum counting frequency as a binary counter	=	15MHz
Maximum counting frequency as a one-gate decade	=	13MHz

The circuit components may be altered to suit different operating requirements. For example, if the bistable circuit is not required to supply a d.c. load the collector resistors may be reduced to maintain good performance when driving capacitive loads and thereby to obtain a better performance as a binary counter and decade counter. If a lower operating speed is acceptable, the recovery diodes and the speed-up capacitors may be omitted.

In the example given above, the effect of omitting these components were as follows.

Omitting the recovery diodes reduced the operating frequency at the nominal input voltage of 4V to 6MHz and reducing the input voltage to 2·5V reduced the maximum operating frequency to 3MHz. These frequencies applied for a 15mA resistive load. When a 100pF load was added, the operating frequency was reduced to 4MHz with a 4V input.

Omitting the speed-up capacitors whilst retaining the recovery diodes reduced the operating frequency from 30MHz to 14MHz under full load conditions with an input between 2·5 and 4V. The waveform at the output was, however, very poor at this frequency, particularly with capacitive loading.

Omitting the speed-up capacitors and the recovery diodes reduced the operating frequency to 1·2MHz with a 5V input and 3MHz with a 7V input. The nominal input voltage of 4V failed to trigger the bistable circuit. Raising the

voltage to 5V gave an operating frequency of 1·2MHz and raising the voltage to 7V gave a frequency of 3MHz.

BISTABLE STAGE FOR MEDIUM AND LOW FREQUENCY OPERATION USING THE BC108 TRANSISTOR

The elements of a bistable stage operating from a 12V supply at medium or low frequencies are shown in Fig. 176. For this example, the required output voltage is assumed to be 8V and the required operating frequency is assumed to be 1MHz.

The value of C_{tc} for the BC108 transistor is 4·5pF, and 10pF is added for wiring capacitances because of the less critical layout of low-speed circuits. The maximum load resistor is chosen to give a collector time-constant, of about 50ns. The values of the collector resistors is, therefore, 3·3kΩ. The value of V_{BE} is again assumed to be 0·7V. These values may now be substituted in Eq. 7 to obtain the minimum value of R_b.

$$R_{b(min)} = 3{\cdot}63\left(\frac{12-0{\cdot}7}{12-8} - 1\right)k\Omega$$

$$= 6{\cdot}65k\Omega.$$

The minimum resistance of an 8·2kΩ±10% resistor is 7·38kΩ, but the minimum value of a 6·8kΩ resistor is only 6·12kΩ which is too low. If the fan-out

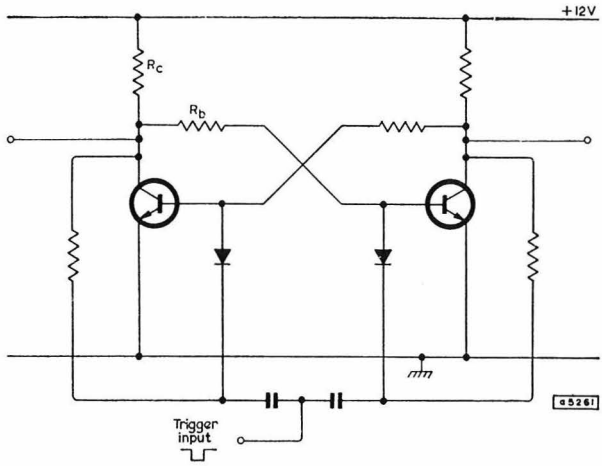

Fig. 175—Elements of a 12V bistable circuit

d.c. current is 10mA, the total effective value of R_{cL} is given by:

$$R_{cL} = \frac{V_{pos}}{\frac{V_{pos}}{R_c} + I_{load}}$$

$$= \frac{12}{\frac{12}{3{\cdot}3} + 10} \text{ k}\Omega$$

$$= 0{\cdot}87\text{k}\Omega$$

Therefore, from Eq. 24

$$\frac{h_{FE}}{\gamma} = \frac{(12-0{\cdot}1)\times(8{\cdot}2+3{\cdot}3)}{0{\cdot}87(12-0{\cdot}7)}$$

$$= 14$$

The minimum value of h_{FE} for the BC108 is about 100 at 10mA in saturation. This gives a minimum value of γ of 7·1, which is a high overdrive factor. The resistor values are shown on the circuit given in Fig. 176, and from these values the maximum value of I_b can be calculated.
From Eq. 3

$$I_{b(max)} = \frac{V_{pos}-V_{BE}}{R_{c(min)}+R_{b(min)}} = \frac{12-0{\cdot}7}{7{\cdot}38+2{\cdot}97}\text{mA}$$

$$= 1{\cdot}1\text{mA}$$

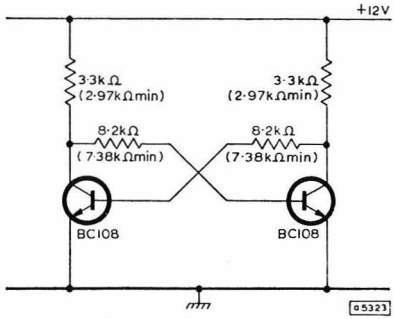

Fig. 176—Bistable circuit showing minimum values

The steering capacitors must remove this current during the desaturation time, which has a maximum value of 500ns. They must also remove a stored charge from the base of the transistor which can have a value of up to 500pC. The total charge to be removed therefore is given by

$$Q_{tot} = Q_S + I_b t_s$$

$$= 500 + 1{\cdot}1\times10^{-3}\times500\times10^{-9} \text{ coulombs}$$

$$= 1050\text{pC}$$

The output voltage level of this bistable circuit is approximately 8V and it is this voltage which is available to drive subsequent stages. Because of this high

output voltage, it is reasonable to design the stage to operate with a minimum input voltage of 5V, giving a negative base voltage of 4·3V. If the base voltage is allowed to change by 30% as a result of absorbing the total charge calculated above, the value of the capacitor may be calculated as follows. The value of C is given by

$$C = \frac{Q}{V},$$

therefore

$$C = \frac{1050 \times 10^{-32}}{1{\cdot}3}$$

$$= 800\text{pF}.$$

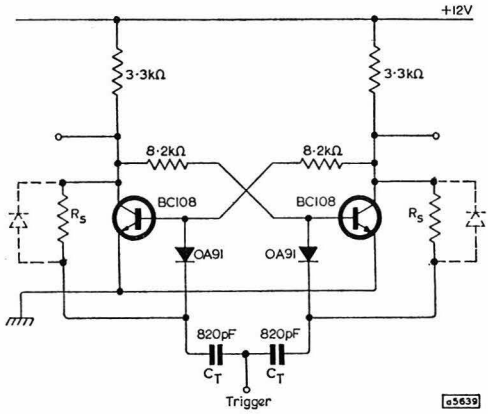

Fig. 177—Bistable circuit using a BC108 transistor

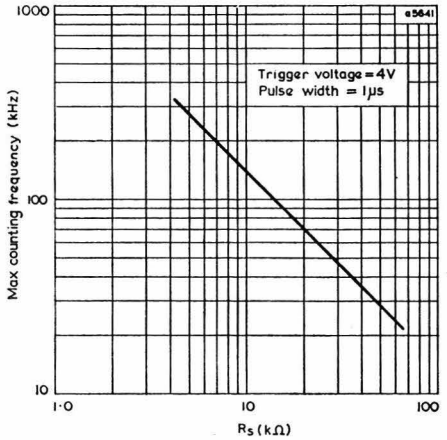

Fig. 178—Measured performance of a bistable circuit using a BC108 transistor, showing how the counting frequency depends upon the value of R_S

The steering resistors should completely discharge the trigger capacitors in two pulse periods. The use of too low a value of steering resistance causes distortion of the output waveform because R_S and R_C form a potential divider to the trigger voltage, and part of the trigger waveform appears at the collector. For this reason, it is not always practicable to use as low a value of resistor as might at first seem desirable, but better speed performance can be obtained by using a higher value of resistance together with recovery diodes.

Steering capacitances should not be reduced below about 390pF, since to do so would require excessively high input voltages in some cases.

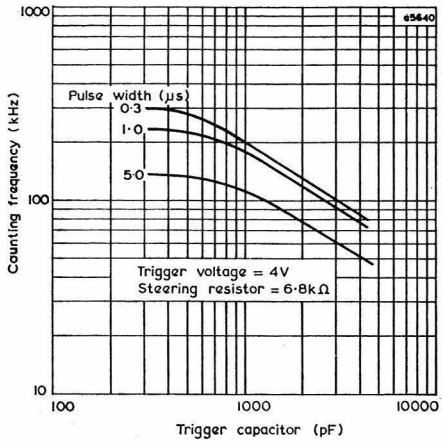

Fig. 179—Measured performance of a bistable circuit using a BC108 transistor, showing how the counting frequency depends upon the value of the trigger capacitor

A counting stage using a BC108 transistor is shown in Fig. 177. The following performance details were obtained by measurement on a prototype counting stage made to the circuit shown in Fig. 177. These performance details are included here chiefly to illustrate the effect of adding speed-up capacitors and recovery diodes and varying other values.

With the basic circuit the output voltage rise time and fall time had values of 100ns and 65ns respectively. By adding 39pF speed-up capacitors, the rise time was increased to 280ns and the fall time was reduced to 30ns. By adding recovery diodes, the maximum operating frequency is increased from 135kHz to 1·3MHz. The effect of varying R_S is shown in Fig. 178 and the effect of varying C_T with one bistable circuit feeding a second similar stage, is shown in Fig. 179.