Transistor Shift Registers*

R. H. BAKER†, I. L. LEBOW†, AND R. E. McMAHON†

Summary—**Three different types of high-speed transistor shift registers are discussed. The high speed (3 to 5 microseconds per shift pulse) is made possible by the use of nonsaturating bistable circuits. Two general shift registers are described making use of respectively one and two transistors per stage. The third register is of a specialized variety capable of shifting a single digit. In addition, an analysis is made of the triggering requirements of the register using a single transistor per stage.**

I. Introduction

IN GENERAL, shift registers are composed of a chain of interconnected bistable elements. When desired, the device may be made to perform such operations as sampling, coding, decoding, storing, etc.

This paper describes three different types of nonsaturating[1] bistable circuits, two of which may be used as the bistable elements necessary to construct shift registers. The third circuit offers a convenient method of building a sampling device such as a matrix switch. The shift-register logic is essentially the same as that used with vacuum tubes, that is, between each bistable stage is a diode "and" gate which controls the state of the succeeding stage.

In Section II, we present two of the basic circuits and describe the static bistable characteristics of each. Section III shows the shift-register logic used. Section IV gives an analysis of the single- and double-transistor bistable circuits. Section V discusses the specialized transistor shift register, and in Section VI we discuss the limitations of each as to speed, reliability, and so forth.

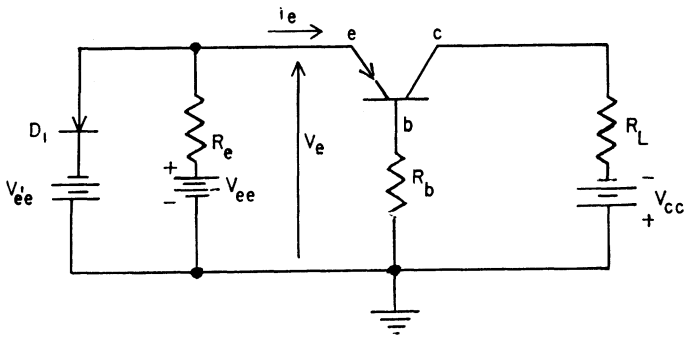

Fig. 1—Negative-resistance bistable circuit.

II. The Bistable Circuits[2]

The Negative-Resistance Bistable Circuit

In order to avoid the problems arising in saturated transistor circuits, the circuit of Fig. 1 was devised.[2]

The diode D_1, and resistor R_e, along with V_{ee} and V_{ee}', present the broken load line $R_e'R_e$ to the transistor emitter input characteristics. This is shown in Fig. 2. When the transistor is in the high conducting state (Point b, Fig. 2), the emitter voltage V_e is equal to V_{ef}. Point b is short-circuit unstable, therefore it is necessary that R_e be larger than the negative transistor input resistance $-R_N$. Moreover, the capacitance at the emitter must be kept small (see Section IV). The second point (a) occurs when the transistor is inactive. Hence we have a single-transistor bistable circuit with two nonsaturated stable states.

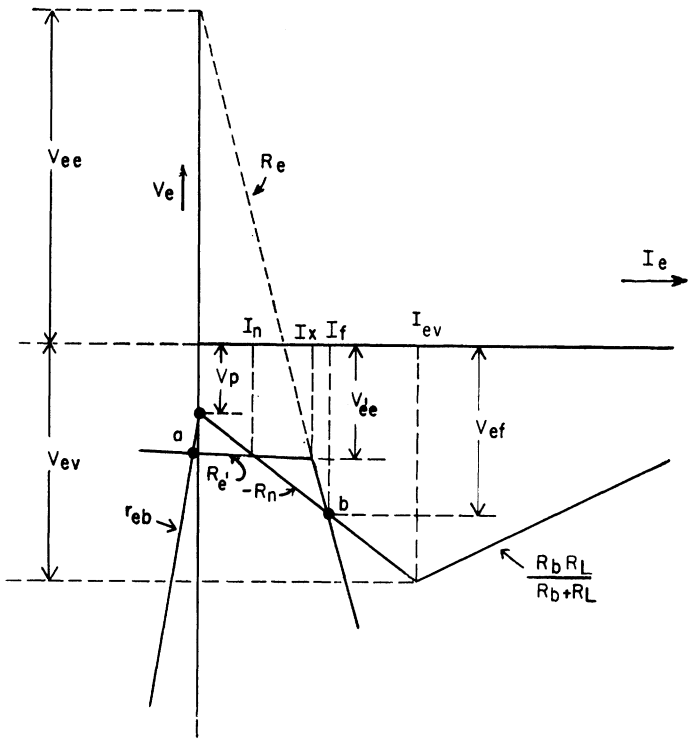

Fig. 2—Static emitter voltage-current characteristics.

The Two-Transistor Nonsaturating Flip-Flop[3]

The circuit shown in Fig. 3(a) was devised to avoid the effects of minority-carrier storage[4] that arise in saturated flip-flops. In order to explain the circuit characteristics, we break the circuit in a symmetrical way as in Fig. 3(b) and plot the input characteristics in Fig. 3(c). Points a and b are the only stable points since the positive input resistance of the "off" transistor in parallel with R_e exceeds in magnitude the negative input resistance of the "on" transistor.[2] Point c, where both transistors are on, is unstable since both transistors have negative input resistances. The current I is kept smaller than I_{ev} to avoid operation in the saturated region.

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† Lincoln Lab., Mass. Inst. of Tech., Cambridge, Mass.

[1] A bistable circuit that has active points in the negative-resistance region.

[2] I. L. Lebow, R. H. Baker, R. E. McMahon, "The Transient Response of Transistor Switching Circuits," Technical Report No. 27, Lincoln Laboratory, M.I.T., July, 1953.

[3] A. W. Carlson, "A Transistor Flip-Flop with Two Stable Nonsaturating States," AFCRC Report, December, 1952.

[4] R. A. Bradbury, "Hole Storage or Turn Off Time," AFCRC, December, 1952.

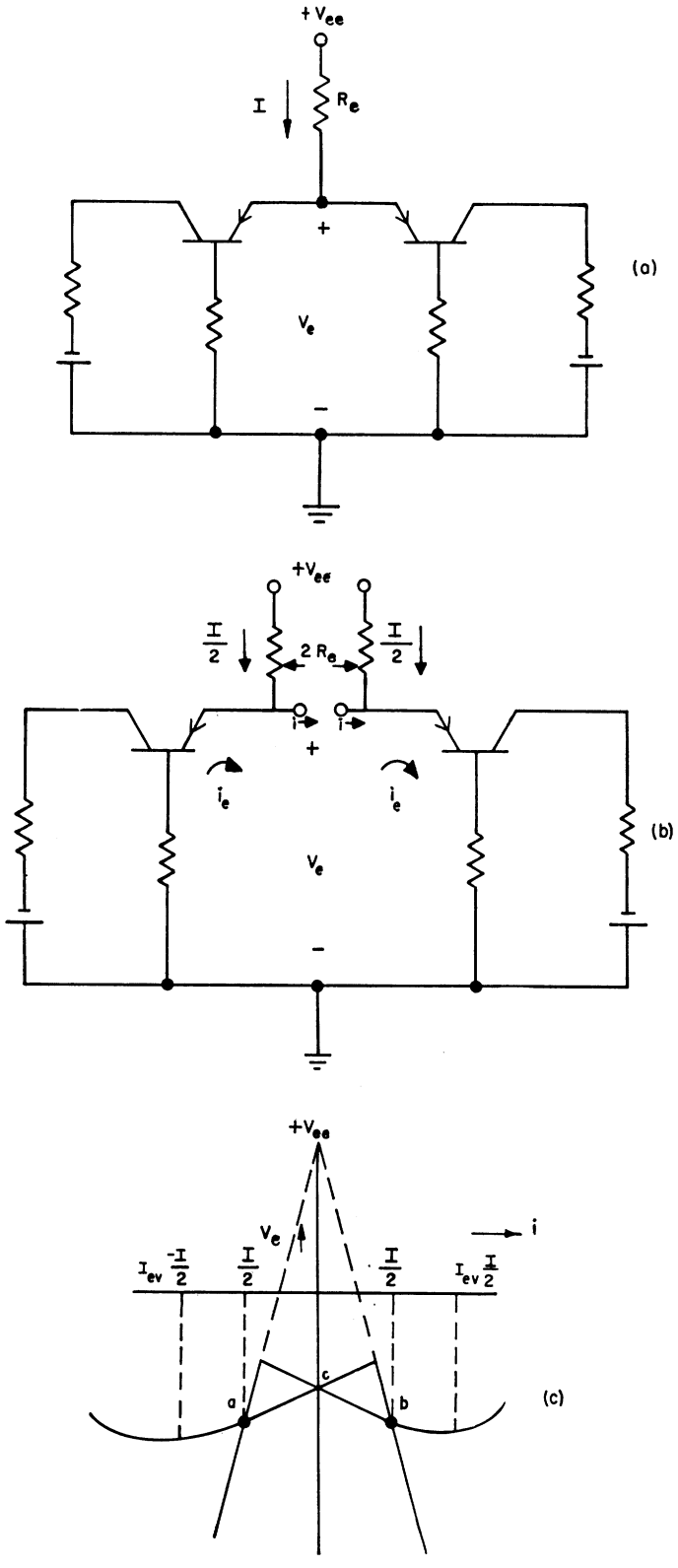


Fig. 3—Nonsaturating flip-flop.

III. The Transistor Shift Register

Single Transistor Per Stage

A shift register may be formed from the bistable element discussed in Section II by inserting diode gates between each stage. This is shown in Fig. 4. The first stage is "set" (switched from Point *a* to Point *b*, Fig. 2) by clock pulses that are controlled by the input binary code. When Stage 1 is set, the diode gate allows a clock pulse to set the second stage. Stage 2 "resets" Stage 1 and allows the next clock pulse to set the third stage, etc. In this manner, the "sense" of the first stage transfers down the chain of bistable elements.

For a detailed three-stage schematic of the shift register, see Fig. 5, Page 1154. Fig. 6, Page 1155, is an analysis of the wave-forms at various points of the circuit.

The Flip-Flop Shift Register

The flip-flop shift register is formed from the bistable elements in the same way as with vacuum-tube shift registers, that is, the inputs to a particular stage are the clock pulses that have been gated from the outputs of the previous stage; this is shown in Fig. 7 on page 1156.

IV. Analysis and Design of the One- and Two-Transistor Bistable Circuits

There are several factors that complicate the design of the transistor bistable circuits necessary to construct high-speed shift registers. First, the variations in transistor parameters from unit to unit necessitate that the basic design of the bistable circuit be stable over quite large percentage changes in operating points. Second, since most presently available transistors (Type BTL 1689) have relatively low-frequency cutoffs (less than 5 Mc), the trigger pulse must be controlled in both amplitude and width.[2,5] Third, since the input impedance of a point-contact transistor circuit is, in general, lower than output impedance, cascading stages becomes difficult.

From Figs. 5 and 6 we see that the "reset" capacitor (Point *h*) must recover through the series combination of resistances R_2 and R_s. Thus, to increase the maximum operating speed, the triggering capacitors must be made as small as possible. To determine the minimum value capacitors that will suffice to reliably switch the nonsaturating bistable circuits, a transient analysis must be made. This analysis is based upon the methods described in detail in the literature. The model is that of the large signal equivalent circuit of Adler[6] with the dynamic interpretation shown in Fig. 8 on page 1157.

Stability Conditions

In all cases we are considering circuits whose "on" stable point is in the active region of the transistor characteristic. The transistor, looking from emitter to ground, displays a negative input impedance and is short-circuit unstable. For stability the external emitter resistance must exceed in magnitude the negative input resistance. In addition, when the external emitter resistance is large, the capacitance between emitter and ground C_e, must satisfy the relation

$$C_e < \frac{\tau}{R_n} = \frac{1}{2\pi f_{co} R_N} \qquad (1)$$

[5] R. H. Baker, "Transistor Shift Register," M. S. Thesis, M.I.T., June, 1953 (E.E. Dept.).

[6] R. B. Adler, "A Large Signal Equivalent Circuit for Transistor Static Characteristics," M.I.T., R. L. E. Transistor Group Report T-2, August, 1951.

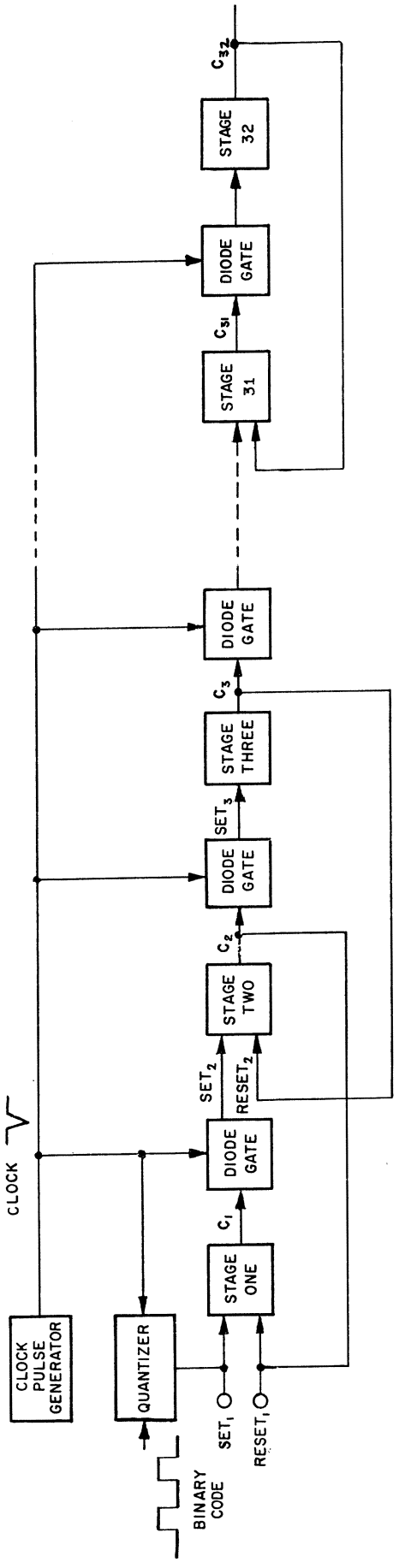


Fig. 4—Block diagram of single-transistor-per-stage shift register.

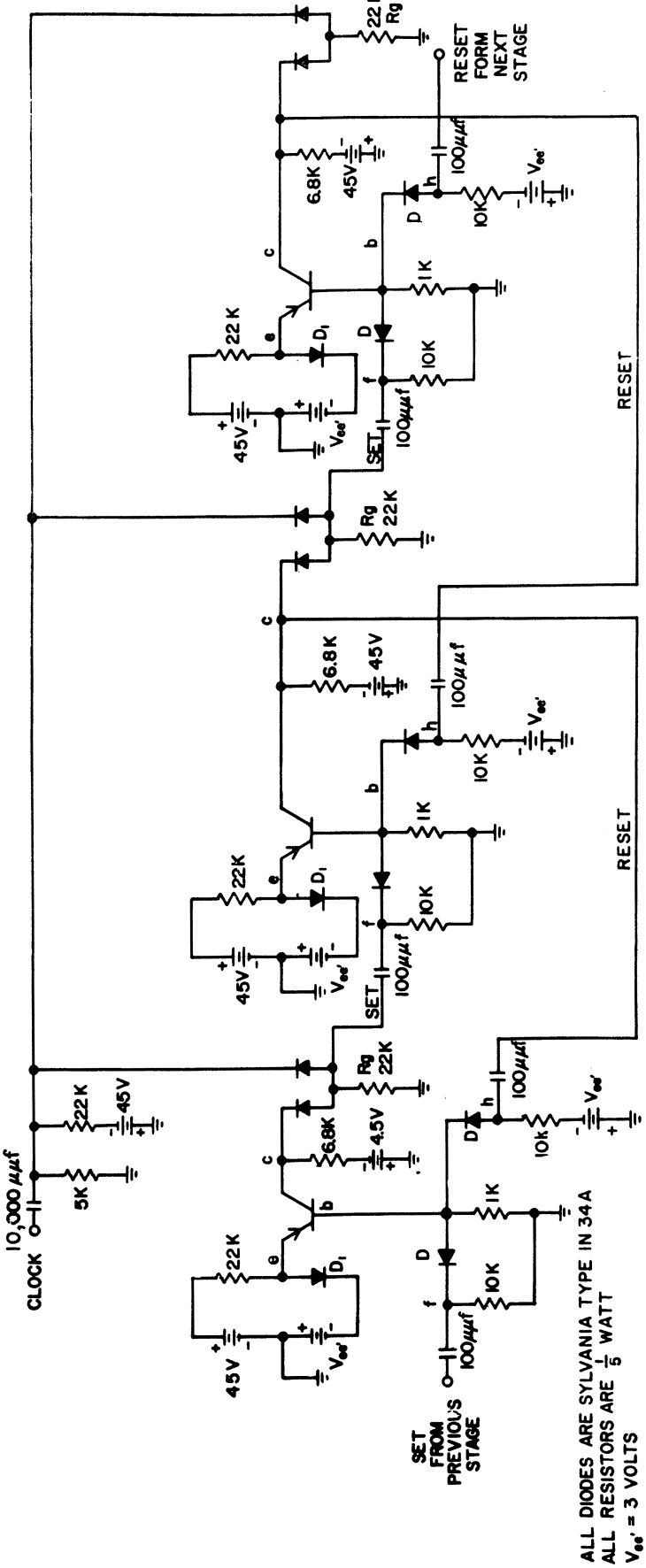
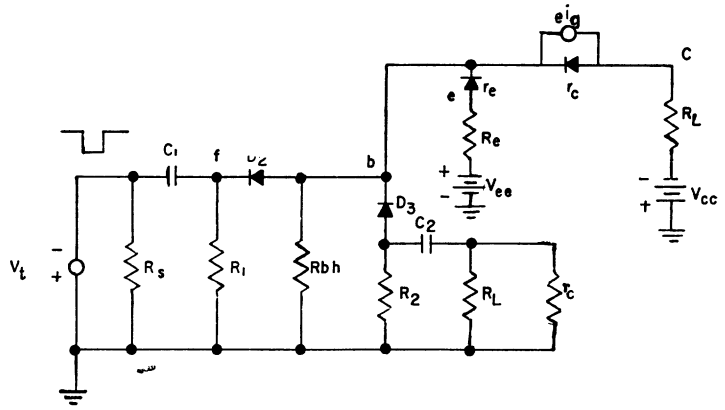
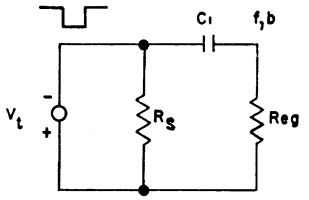
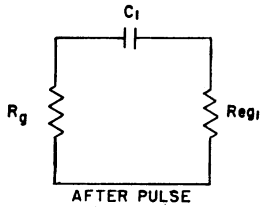


Fig. 5—Circuit diagram of single-transistor-per-stage shift register.



R_s (CLOCK SOURCE RESISTANCE) ≈ 0





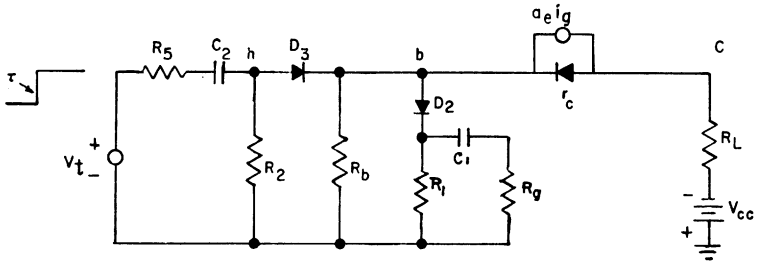
AFTER PULSE IS REMOVED

$R_s \approx 0$

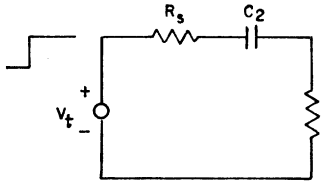
$Reg \approx R_b \,||\, R_1 \,||\, R_2 \,||\, R_L \,||\, r_c \,||\, (r_c + R_2)$

WHILE PULSE IS PRESENT

TRIGGER ON EQUIVALENT CIRCUITS

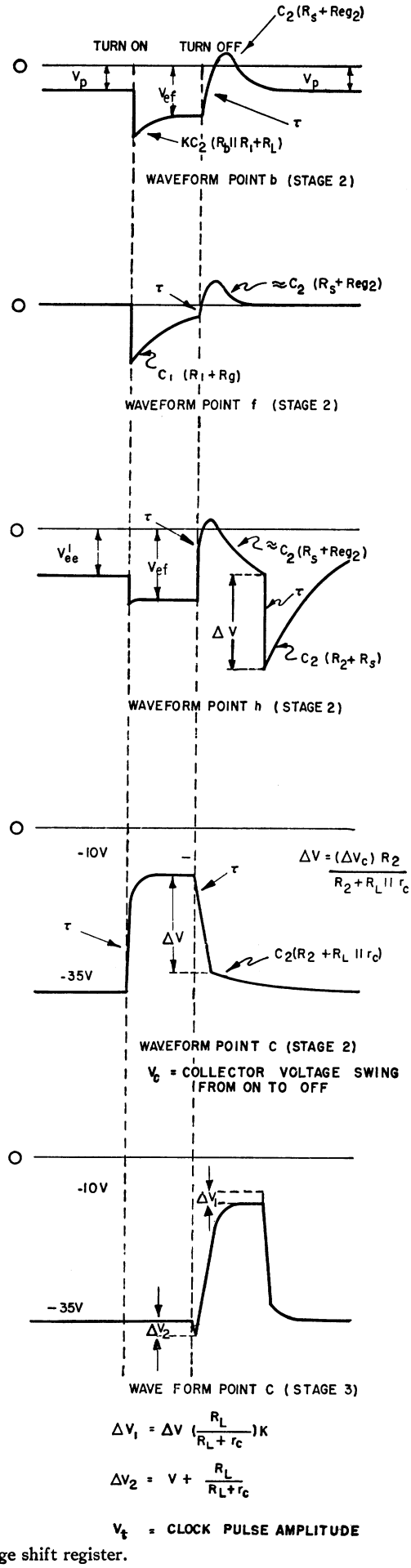


$R_s \approx R_L \,||\, r_c$



$Reg_2 \approx R_2 \,||\, R_b \,||\, R_1 \,||\, R_g \,||\, (r_c + R_L)$

TRIGGER OFF EQUIVALENT CIRCUITS



$$\Delta V_1 = \Delta V \left(\frac{R_L}{R_L + r_c}\right) K$$

$$\Delta V_2 = V + \frac{R_L}{R_L + r_c}$$

V_t = CLOCK PULSE AMPLITUDE

Fig. 6—Waveform analysis of single-transistor-per-stage shift register.

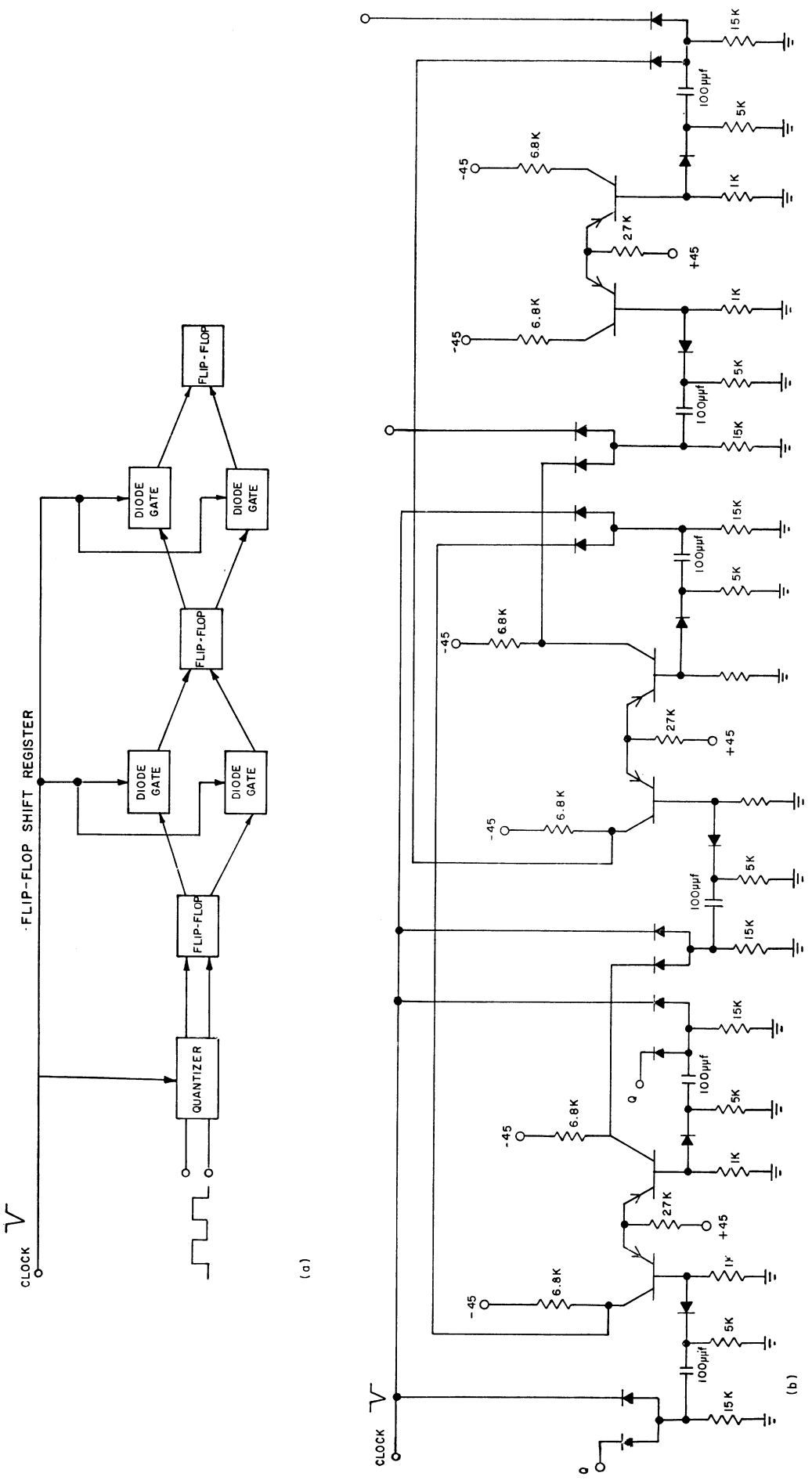


Fig. 7—Flip-flop shift register. (a) Block diagram; (b) Circuit diagram.

where f_{co} is the transistor cutoff frequency. The above relation is obtained[2,7] by demanding that the transient currents in the active region be converging exponentials.

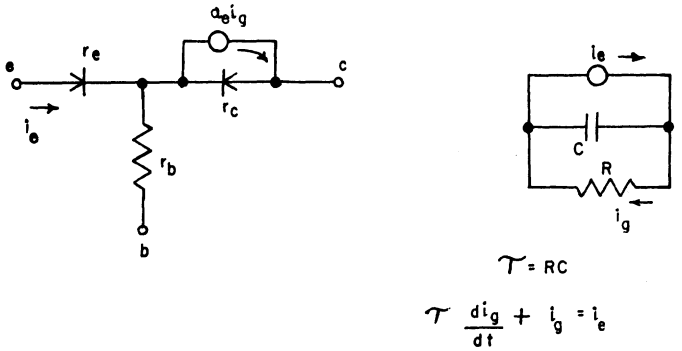


Fig. 8—Large-signal equivalent circuit for transistor dynamic characteristics.

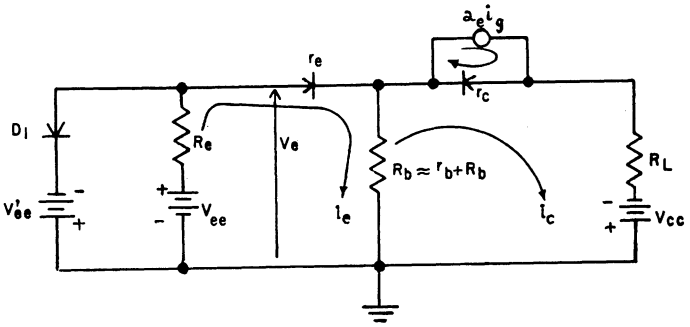


Fig. 9—Negative-resistance bistable circuit with transistor large-signal dynamic equivalent circuit.

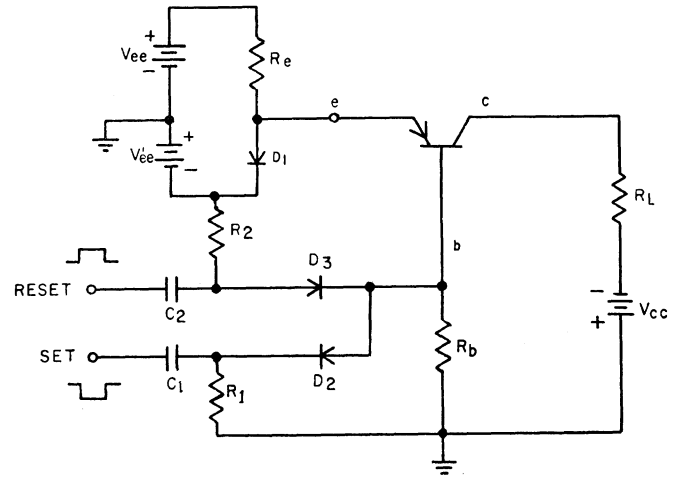


Fig. 10—Negative-resistance bistable circuit.

Triggering Requirements of the Negative-Resistance Bistable Circuit

Turn On: Consider the circuit shown in Fig. 10. In order to be sure that the negative-resistance bistable circuit will switch (change states) reliably, it is necessary that the trigger pulse exceed a given amplitude for a given period of time.[2,5] Moreover, the amplitude-width requirement is different depending upon the state of the circuit[2,5] and the frequency response of the transistor. Consider only the "set" (turn on) function of the circuit shown in Fig. 10.

[7] B. G. Farley, "Dynamics of Transistor Negative Resistance Circuits," Proc. I.R.E., vol. 40, pp. 1497–1507; November, 1952.

Solving the loop equations, the following expression may be obtained for i_g:

$$\frac{d^2 i_g}{dt^2} + \frac{di_g}{dt}\left(\frac{1}{\tau} + \frac{R_p + R_e}{C_1 R_e R_p}\right) + i_g\left(\frac{R_e - R_N}{C_1 R_e R_p \tau}\right) - \frac{V_{cc} + V_p}{C_1 R_e R_p \tau}, \tag{2}$$

where R_p is the input resistance of the transistor with $\alpha = 0$, and V_p is the magnitude of the peak point voltage. The solution of (2) is the sum of two exponentials, the frequencies of which are given by

$$\omega^2 + \omega\left(\frac{1}{\tau} + \frac{R_e + R_p}{C_1 R_e R_p}\right) + \frac{R_e - R_N}{C_1 R_e R_p \tau} = 0. \tag{3}$$

The applied set pulse opens D_1. R_e is greater than R_N. Hence, from (3) both ω's are negative. The initial shape of i_e then, is a positive step, the amplitude of which depends upon the applied trigger voltage, V_t, followed by a converging decay. Since i_g tries to follow i_e, the eventual circuit state is dependent upon the relative magnitudes of i_e and i_g as time progresses. For when i_e decays to I_x (Fig. 2), diode D_1 closes and R_e becomes R_e'. Since R_e' is less than R_N, the third term in (3) is negative and the circuit is unstable. In order for the circuit still to switch on, even though i_e becomes less than the value I_x, the rate of change of i_e must, at some time after t_x, be equal to zero (t_x is defined as the time at which i_e is equal to the value I_x).

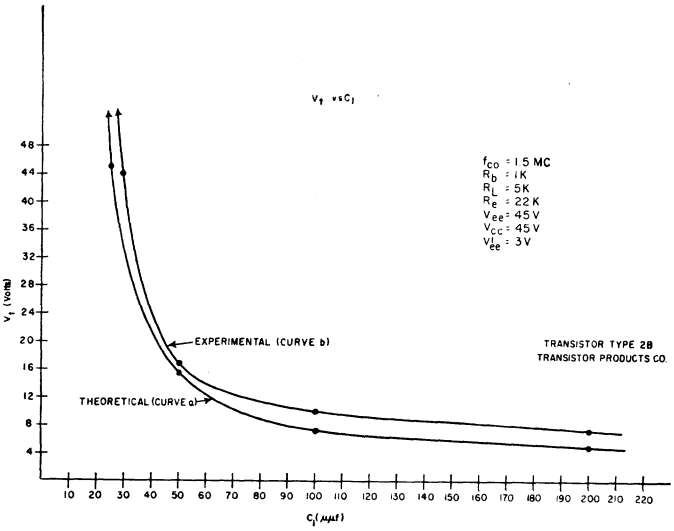


Fig. 11—Turn-on characteristic of negative-resistance bistable circuit.

The approximate criterion for triggering on is[2,5]

$$i_g(t_x) > I_N \text{ Turn on} \tag{4a}$$

$$i_g(t_x) < I_N \text{ Turn back off.} \tag{4b}$$

The values of C_1 as a function of the trigger voltage V_t that will fulfill the condition (4a) appear in Fig. 11. The results are found to be in good agreement with experimental data.

Turn-Off: The approach that may be used to determine the "turn-off" trigger requirement is the same

as for the turn-on case; using the appropriate equivalent circuit, we solve the pertinent loop equations, define the turn-off criterion, and solve for the minimum trigger voltage that will suffice to switch the circuit.

Since the circuit is turned off by applying a positive pulse to the base, the transistor emitter is instantaneously switched off and C_2 starts charging (Fig. 10). When the base voltage decays below V_{ee}', i_e starts increasing. The same arguments as in the previous section show that, in order for the circuit to switch off, i_e must go to zero. As in the case of turning on, the triggering diode D_3 will open when the rate of change of i_e is equal to zero. Hence at this time t_Δ,[2,5]

$$i_g(t_\Delta) > I_N \quad \text{Turn back on} \tag{5a}$$

$$i_g(t_\Delta) < I_N \quad \text{Turn off.} \tag{5b}$$

Fig. 12 shows a comparison between the theoretical and experimental data when V_t is plotted as a function of C_2.

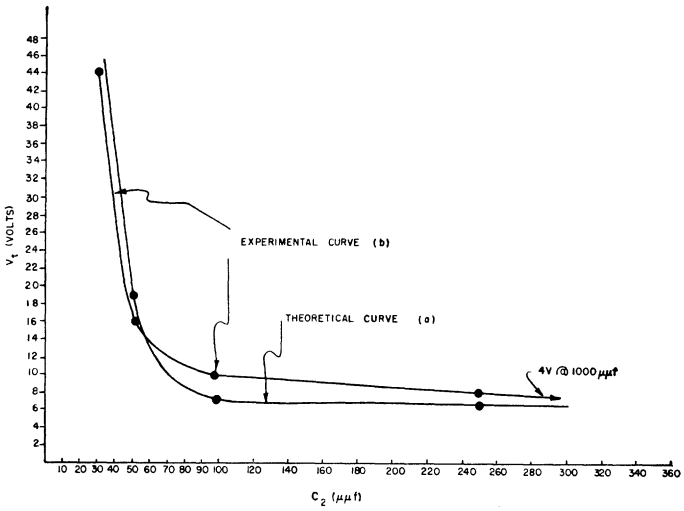


Fig. 12—Turn-off characteristics of negative-resistance bistable circuit.

The Two-Transistor Nonsaturating Flip-Flop[4]

We may replace the transistors in the circuit of Fig. 3(a) by the equivalent circuit shown in Fig. 8. When this is done, the circuit of Fig. 13 is obtained, where the battery V_t implies that we are triggering on transistor B by applying a negative pulse to the base.

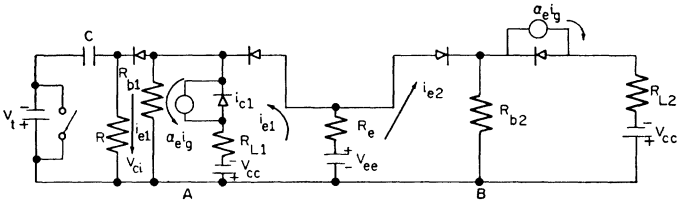


Fig. 13—Dynamic equivalent circuit of two-transistor flip-flop.

The circuit of Fig. 13 may be analyzed by the same techniques described above. The solutions for the various current equations will be of the same form, although slightly more complex due to the circuit configuration. As above, the triggering requirements have a definite minimum amplitude-width relationship. This analysis is made elsewhere,[8] therefore it will not be repeated. However, an important point should be noted: the two-transistor flip-flop will trigger on narrower pulses than will the negative-resistance bistable circuit. This is because, although we are triggering at the base of transistor A (Fig. 13), and hence, the same conditions apply as when triggering the single transistor, transistor B is being triggered at the emitter. Since the circuit is short-circuit unstable at the emitter, the currents in transistor B decay (or increase, as the case may be) with positive exponentials. This causes faster switching of transistor B, which in turn will cause the circuit to switch faster.

A Specialized Transistor Shift Register[7]

A logical extension of the circuit shown in Fig. 3(a) is the multistage circuit of Fig. 14 where several transistor stages have their emitters tied to a common load resistor. As in the two-transistor case, only one transistor can conduct at a time, since any state with more than one transistor in the negative-resistance region is unstable.

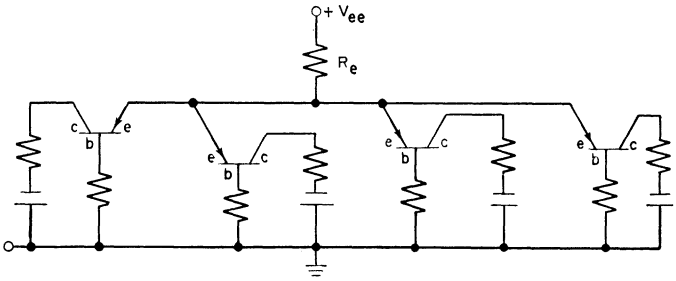


Fig. 14—Four-transistor circuit with four stable states.

A specialized shift register may be based upon this idea, as shown in Fig. 15. Suppose a negative pulse is applied to the base of the first stage. This stage will then be conducting and the other nonconducting. The sense of this first may be then propagated down the register by clock pulses gated to stages sequentially.

The number of stages that may be connected together is limited by two factors. First, the total accumulated capacitance between emitter and ground must be kept small enough to render each transistor stable (1). Second, the resistance between emitter and ground, which is reduced by the addition of more transistors, must be kept large enough to render each transistor's "on" operating point in the negative-resistance region.

As many as ten transistors may be connected in this manner with little or no difficulty. We may construct a long register, using this method, as shown in Fig. 16.

Comparison and Evaluation

An over-all analysis of the shift-register circuits reveals the following facts: first, a point-contact transistor switching circuit requires a definite, predictable, minimum pulse-height width relationship that is a function

[8] R. E. McMahon, I. L. Lebow, R. H. Baker, "A Two Transistor Shift Register," Lincoln Laboratory, M.I.T., M24-20, May, 1953.

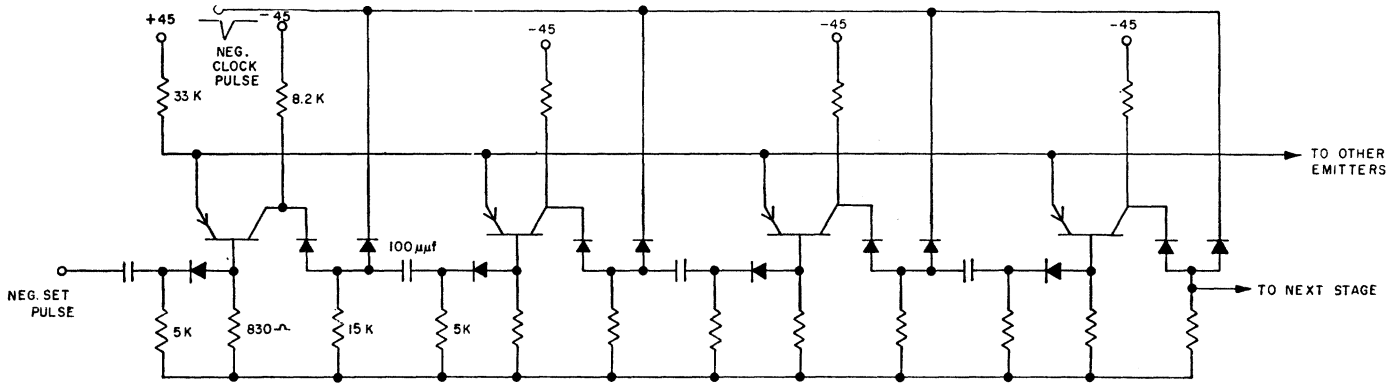


Fig. 15—Circuit diagram of specialized shift register.

of the transistor frequency response and the circuit configuration; secondly, the maximum speed of operation of a system constructed from these circuits is limited, not by the switching time of the circuits, but by the recovery time of the associated triggering capacitors. In view of this, when designing high-speed systems, it is advantageous to use circuits with (a) high input impedance, and (b) as low recovery resistance as possible for the triggering-capacitor circuits.

The above results appear to exclude the possibility of using saturated bistable circuits with a high degree of reliability due to the turn-off triggering time.[2]

Exhaustive tests have been made on each of the shift registers described above. The two-transistor flip-flop works reliably with 80 per cent of all BTL 1698 transistors at rates up to 5 μsec per shift pulse. The shift register constructed from the negative-resistance bistable circuit will operate up to 6 μsec per stage.

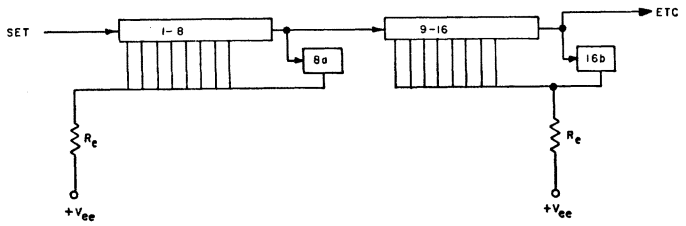


Fig. 16—Block diagram of specialized shift register showing arrangement for designing long shift registers.

However, at these fast rates, the coupling capacitors must necessarily be small, and this shift register therefore is less reliable than the flip-flop shift register. At lower rates, the coupling capacitor may be larger with correspondingly greater reliability. The specialized shift registers offer good reliability up to 3 μsec per shift pulse when a maximum of 9 stages is connected to the common bias resistor, R_e. Longer registers should be connected as shown in Fig. 16.

Comb Filters for Pulsed Radar Use*

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Summary—**This paper presents a discussion of the concepts involved in the use of "comb" filters for signal-to-noise improvement in pulsed radar systems. A "comb" filter is one whose frequency spectrum consists of a number of equi-spaced elements resembling the tines of a comb. Consideration is given to the characteristics of the frequency spectra arising from sequences of pulses varying in number from one to infinity. These results indicate that the use of comb filters may be feasible in most cases. Hence, a study is made of the use of three different types of filters to determine their effect on the signal-to-noise ratio. These filters range from the simplest type of uniform filters to the North type of matched filter. The relative merits of these filters are determined in terms of improvement in signal-to-noise ratio.**

* Decimal classification: R143.2×R537. Original manuscript received by the IRE, October 14, 1953; revised manuscript received, February 23, 1954.

† Naval Research Laboratory, Washington, D. C.

Introduction

A PAPER which appeared in the literature[1] on the detection of periodic signals in noise prompted a spirited discussion[2] which centered about the characteristics of the frequency spectra of pulsed signals and the feasibility of improving the signal-to-noise ratio by the use of comb filters. The question of the frequency spectrum of the received signal is of fundamental im-

[1] Y. W. Lee, T. P. Cheatham, Jr., and J. B. Wiesner, "Application of correlation analysis to the detection of periodic signals in noise," PROC. I.R.E., vol. 38, pp. 1165–1171; October, 1950.

[2] Discussion on "Application of correlation analysis to the detection of periodic signals in noise," by Lee, Cheatham, Jr., and Wiesner, with N. Marchand, M. Leifer, and H. R. Holloway, PROC. I.R.E., vol. 39, pp. 1094–1095; September, 1951.