Interfacing the DP8420A/21A/22A to the 68020

National Semiconductor
Application Note 539
Joe Tate and Rusty Meier
May 1989

INTRODUCTION

This application note explains interfacing the DP8420A/21A/22A DRAM controller to the 68020 microprocessor. Three different designs are shown and explained. It is assumed that the reader is already familiar with the 68020 access cycles and the DP8420A/21A/22A modes of operation.

DESIGN #1 DESCRIPTION

Design #1 is a simple circuit to interface the 68020 to the DP8420A/21A/22A and up to 64 Mbytes of DRAM. The DP8420A/21A/22A is operated in Mode 1. An access cycle begins when the 68020 places a valid address on the address bus and asserts the address strobe ($\overline{AS}$). Chip select ($\overline{CS}$) is generated by a 74AS138 decoder. If a refresh or Port B access (DP8422A only) is not in progress, the DP8420A/21A/22A will assert the proper $\overline{RAS}$ depending on the bank select inputs (B0, B1). After guaranteeing the programmed value of row address hold time, the DP8420A/21A/22A will switch the DRAM address (Q0–8, 9, 10) to the column address and assert $\overline{CAS}$. By this time, the 74AS245s have been enabled and the DRAMs place their data on the data bus. The DP8420A/21A/22A also asserts $\overline{DTACK}$ which is used to generate $\overline{DSACK}$0,1 to the 68020.

If a refresh had been in progress, the DP8420A/21A/22A would have delayed the 68020's access by inserting wait states into the access cycle until the refresh was complete and the programmed amount of precharge time was met. This circuit can run up to 16 MHz with one wait state. However, the timing parameters become close to the minimums for the DP8420A/21A/22A parameters. $\overline{ADS}$ asserted to CLK high ($400b), $\overline{CS}$ setup to $\overline{ADS}$ asserted ($401) and $\overline{ADS}$ negated held from CLK ($405). Problems can also occur if the loading on the clocks generated from the 74AS74 cause too much skew between CLK and $\overline{CLK}$. The clock must be inverted to guarantee timing parameters. A solution to this problem is to invert the CLOCK to the 68020 with a 74AS04.

Since the 68020 address strobe can end late in the access, a problem with $\overline{RAS}$ precharge can occur in back-to-back accesses. In these accesses, the DP8420A/21A/22A will guarantee the precharge time by inserting wait states. To reduce this problem, memory interleaving should be used by tying the low order address bits to the bank selects.

Timing parameters are referenced to the numbers shown in the DP8420A/21A/22A data sheet. Numbered times starting with a "$" refer to the DP8420A/21A/22A timing parameters. Numbered times starting with "#" refer to the Motorola 68020 data sheet. Equations have been given to allow the user to calculate timing based on his frequency and application. The clock has been chosen at a multiple of 2 MHz only to allow the user to hook the system clock to the PLL delay line clock (DELCLK). If you are running at a frequency that is not a multiple of 2 MHz, it is recommended that you use a clock which is a multiple of 2 MHz for DELCLK. If DELCLK is not a multiple of 2 MHz, $\overline{ADS}$ to $\overline{CAS}$ must be recalculated.

DESIGN #1 TIMING AT 16 MHz AND 12 MHz

Clock Period = Tcp16 = 62.5 ns @ 16 MHz
= Tcp12 = 83 ns @ 12 MHz

$400b: $\overline{ADS}$ Asserted Setup to CLK High
= Clock Period − 68020 Clock to $\overline{AS}$ Low Max
= Tcp16 − #9 Max
= 62.5 ns − 30 ns
= **32 ns @ 16 MHz**
= Tcp12 − #9 Max
= 83 ns −40 ns
= **43 ns @ 12 MHz**

$401: $\overline{CS}$ Setup to $\overline{ADS}$ Asserted
= 68020 Address to $\overline{AS}$ Maximum − 74AS138 Decoder Maximum
= #11 Max − Tphl Max
= 15 ns − 9 ns
= **6 ns @ 16 MHz**
= #11 Max − Tphl Max
= 20 ns − 9 ns
= **11 ns @ 12 MHz**

$407 & 404: Address Valid Setup to $\overline{ADS}$ Asserted
= 68020 Address to $\overline{AS}$ Maximum
= #11 Max
= **15 ns @ 16 MHz**
= #11 Max
= **20 ns @ 12 MHz**

$405: $\overline{ADS}$ Negated Held from CLK High
= 68020 Minimum Clock to $\overline{AS}$
= #9 Min
= **3 ns @ 16 MHz**
= #9 Min
= **3 ns @ 12 MHz**

#47A: $\overline{DSACK0}$, 1 Setup Time
= ½ Clock Period − Max 74AS74 Delay − Max 74AS32 Delay
= 31 ns − 9 ns − 5 ns
= **17 ns @ 16 MHz**
= ½ Tcp12 − Tphl Max − Tphl Max
= 41 ns − 9 ns − 5 ns
= **27 ns @ 12 MHz**

RRD-B30M115/Printed in U. S. A.

#47B: $\overline{DSACK0}$, 1 Hold Time
= ½ Clock Period + Min 74AS74 Delay + Min 74AS32 Delay
= ½ Tcp16 + Tphl Min + Tphl Min
= 31 ns + 5 ns + 1 ns
= 37 ns @ 16 MHz
= ½ Tcp12 + Tphl Min + Tphl Min
= 41 ns − 9 ns − 5 ns
= 47 ns @ 12 MHz

$\overline{RAS}$ Low during REFRESH

tRAS = Programmed Clocks − [(CLK High to Refresh $\overline{RAS}$ Asserted) − (CLK High to Refresh $\overline{RAS}$ Negated)]
= Tcp16 + Tcp16 − $55
= 62.5 ns + 62.5 ns −6 ns
= 119 ns @ 16 MHz
= Tcp12 + Tcp12 − $55
= 83.3 ns + 83.3 ns − 6 ns
= 160 ns @ 12 MHz

$\overline{RAS}$ Precharge Parameters**

$29b: $\overline{AREQ}$ Negated Setup to CLK High
= CLOCK Period − CLOCK Low to 68020 $\overline{AS}$ Negated
= Tcp16 − #12
= 62.5 ns − 30 ns
= 32 ns @ 16 MHz
= Tcp12 − #12
= 83 ns − 40 ns
= 43 ns @ 12 MHz

tRP = s5 + s0 + s1 + s2 − 68020 CLK Low to $\overline{AS}$ Negated − [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]
= 2 Tcp16 − #12 − $50
= 125 ns − 30 ns − 16 ns
= 79 ns @ 16 MHz w/8420A/21A/22A
= 81 ns @ 16 MHz w/8420A/21A/22A
= 2 Tcp12 − #12 − $50
= 166 ns − 40 ns − 16 ns
= 120 ns @ 12 MHz

****Note:** To gain more precharge program 3T.

tRAC AND tCAC TIMING FOR DRAMs

Timing is supplied for the system shown in *Figure 1 (See Figures 2, 3)*. Since systems and DRAM times vary, the user is encouraged to change the following equations to match his system requirements. Timing has been supplied for systems with 0, 1 or 2 wait states. If the DELCLK is not a multiple of 2 MHz, the timing for tRAH and tASC will increase. Because tRAH and tASC will increase, $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also increase and must be changed according to the equations given in the data sheet. The $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also have to be changed depending on the capacitance of the DRAM array.

0 Wait States

tRAC = s1 + s2 + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted
= Tcp16 + Tcp16 − #9 Max − Tphl Max − #27 Min − $402 Max
= 62.5 ns + 62.5 ns − 30ns − 7 ns − 5 ns −35 ns
= 48 ns @ 16 MHz w/8420A-20 Heavy Load
= 58 ns @ 16 MHz w/8420A-25 Light Load
= Tcp12 + Tcp12 − #9 Max − Tphl Max − #27 Min − $402 Max
= 83 ns + 83 ns − 40 ns − 7 ns − 10 ns − 35 ns
= 74 ns @ 12 MHz w/8420A-20 Heavy Load
= 84 ns @ 12 MHz w/8420A-25 Light Load

1 Wait State

tRAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted
= Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl Max − #27 Min − $402 Max
= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 7 ns − 5 ns −35 ns
= 110 ns @ 16 MHz w/8420A-20 Heavy Load
= 120 ns @ 16 MHz w/8420A-25 Light Load
= Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl Max − #27 Min − $402 Max
= 83 ns + 83 ns + 83 ns −40 ns − 7 ns − 10 ns − 35 ns
= 157 ns @ 12 MHz w/8420A-20 Heavy Load
= 167 ns @ 12 MHz w/8420A-25 Light Load

2 Wait States

tRAC = s1 + s2 + sw + sw + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted
= Tcp16 + Tcp16 + Tcp16 + Tcp16 − 9 Max − Tphl Max − #27 Min − $402 Max
= 62.5 ns + 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 7 ns −5 ns −35 ns
= 173 ns @ 16 MHz w/8420A-20 Heavy Load
= 183 ns @ 16 MHz w/8420A-25 Light Load

= Tcp12 + Tcp12 + Tcp12 + Tcp12 −9 Max − Tphl Max − #27 Min − $402 Max

= 83 ns + 83 ns + 83 ns + 83 ns −40 ns −7 ns − 10 ns −35 ns

= **240 ns @ 12 MHz** w/8420A-20 Heavy Load

= **250 ns @ 12 MHz** w/8420A-25 Light Load

0 Wait State

tCAC = s1 + s2 + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 − #9 Max − Tphl Max − #27 Min − $403a Max

= 62.5 ns + 62.5 ns − 30 ns − 7 ns −5 ns − 94 ns

= **−11 ns @ 16 MHz** w/8420A-20 Heavy Load

= **8 ns @ 16 MHz** w/8420A-25 Light Load

= Tcp12 + Tcp12 − #9 Max − Tphl Max − #27 Min − $403a Max

= 83 ns + 83 ns −40 ns − 7 ns − 10 ns − 94 ns

= **15 ns @ 12 MHz** w/8420A-20 Heavy Load

= **34 ns @ 12 MHz** w/8420A-25 Light Load

1 Wait State

tCAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl Max − #27 Min − $403a Max

= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 7 ns − 5 ns − 94 ns

= **51 ns @ 16 MHz** w/8420A-20 Heavy Load

= **70.5 ns @ 16 MHz** w/8420A-25 Light Load

= Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl Max − #27 Min − $403a Max

= 83 ns + 83 ns + 83 ns − 40 ns − 7 ns − 10 ns − 94 ns

= **98 ns @ 12 MHz** w/8420A-20 Heavy Load

= **134 ns @ 12 MHz** w/8420A-25 Light Load

2 Wait States

tCAC = s1 + s2 + sw + sw + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl Max − #27 Min − $403a Max

= 62.5 ns + 62.5 ns + 62.5 ns +62.5 ns − 30 ns − 7 ns − 5 ns − 94 ns

= **114 ns @ 16 MHz** w/8420A-20 Heavy Load

= **133 ns @ 16 MHz** w/8420A-25 Light Load

= Tcp12 + Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl Max − #27 Min − $403a Max

= 83 ns + 83 ns + 83 ns + 83 ns − 40 ns − 7 ns − 10 ns − 74 ns

= **181 ns @ 12 MHz** w/8420A-20 Heavy Load

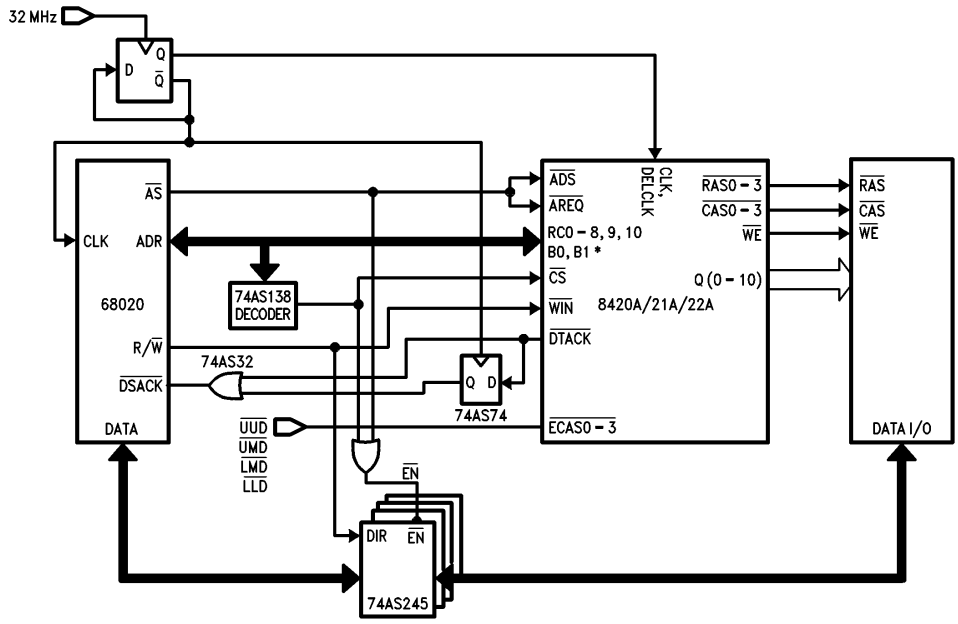
= **200 ns @ 12 MHz** w/8420A-25 Light Load

Design #1 Programming Bits

Bits	Description	Value
R0, R1	$\overline{RAS}$ Low during REFRESH = 2T $\overline{RAS}$ Precharge Time = 2T	R0 = 0 R1 = 1
R2, R3	$\overline{DTACK}$ Generation Modes for Non-Burst Accesses (½T after $\overline{RAS}$)	R2 = 0 R3 = 1
R4, R5	$\overline{DTACK}$ during Burst Mode	R4 = x R5 = x
R6	Add Wait States with WAITIN	R6 = x
R7	$\overline{DTACK}$ Mode Selected	R7 = 1
R8	Non-Interleaved Mode	R8 = 1
R9	Staggered or All REFRESH	R9 = u
C0, C1, C2	Divisor for DELCLK	C0 = s C1 = s C2 = s
C3	+30 REFRESH	C3 = 0
C4, C5, C6	$\overline{RAS}$, $\overline{CAS}$ Configuration Mode *Choose An All $\overline{CAS}$ Mode	C4 = u C5 = u C6 = u
C7	Select 0 ns Column Address Setup	C7 = 1
C8	Select 15 ns Row Address Hold	C8 = 1
C9	CAS is Delayed to Next Rising CLOCK during Writes	C9 = 1
B0	The Row/Column Bank Latches Are in Fall Through Mode	B0 = 1
B1	Access Mode 1	B1 = 1
$\overline{ECAS}$0	$\overline{CAS}$ not extended beyond $\overline{RAS}$	$\overline{ECAS}$0 = 0

x = don't care
u = user defined
s = system dependent

s @ 16 MHz	s @ 12 MHz
C0 = 0 C1 = 1 C2 = 0	C0 = 0 C1 = 0 C2 = 1



TL/F/9733–1

*Tie least significant ADR bits (A2, A3) to B0, B1.

FIGURE 1. Design # 1, 68020 up to 16 MHz with 1 Wait State

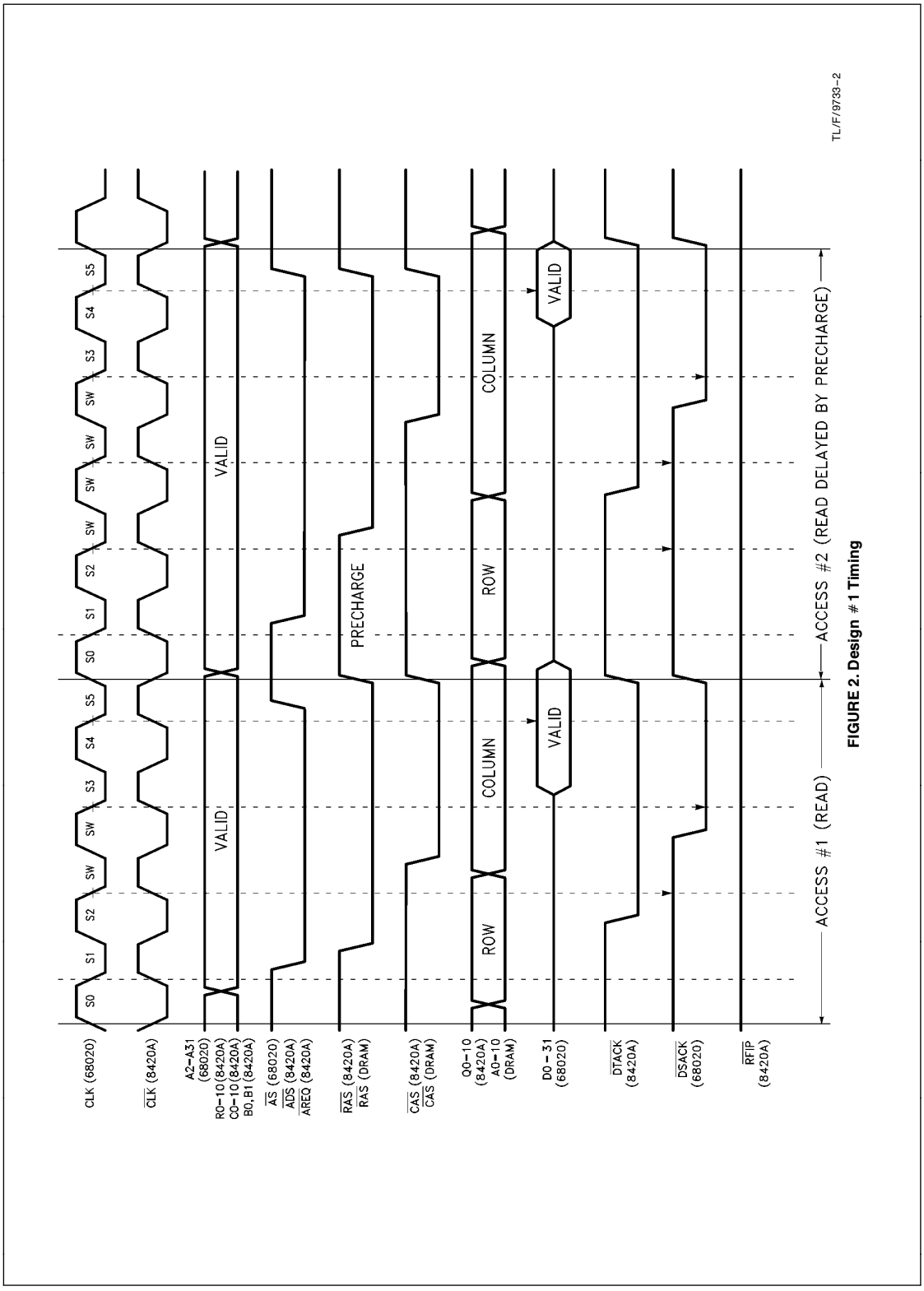


FIGURE 2. Design #1 Timing

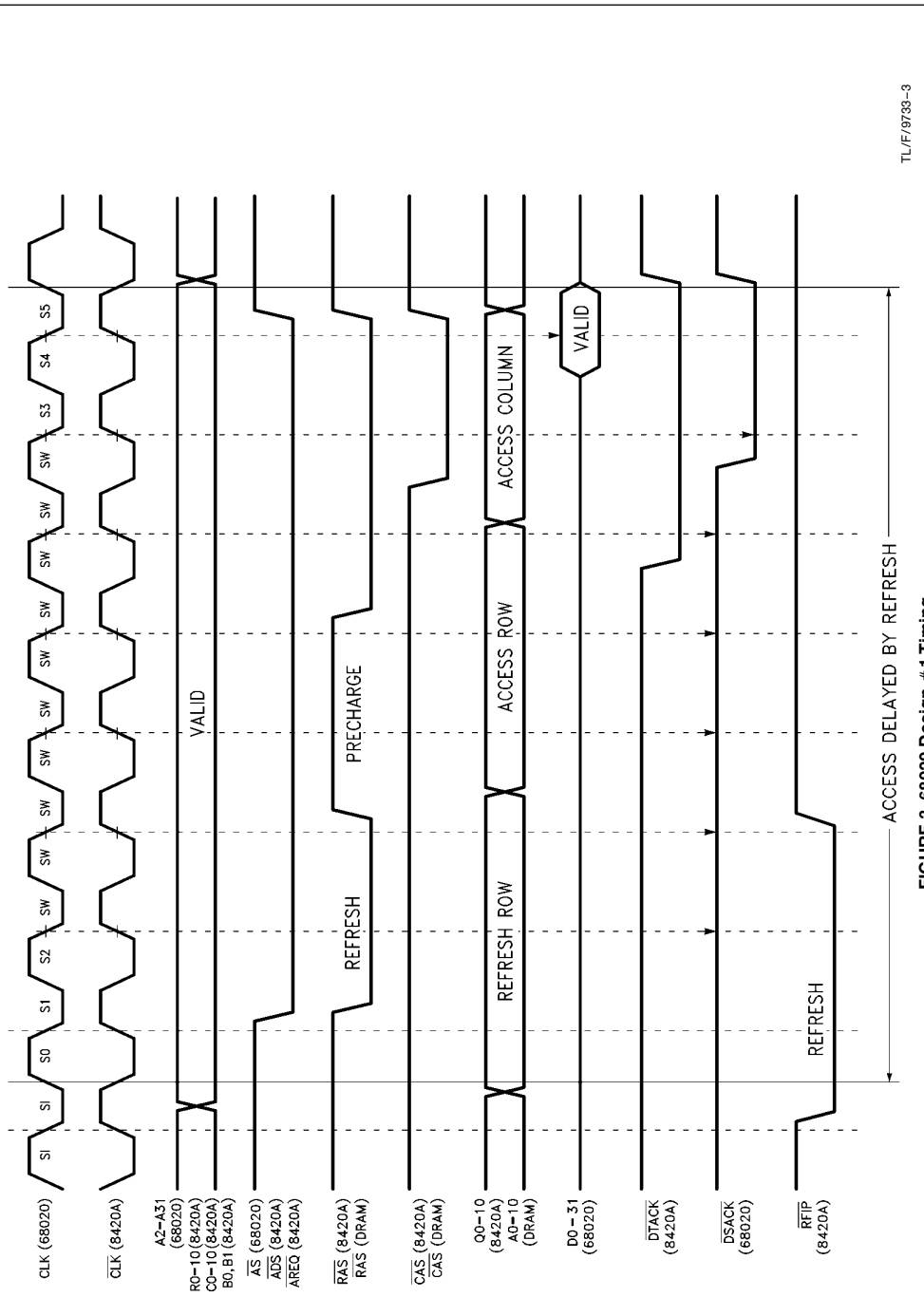


FIGURE 3. 68020 Design #1 Timing

DESIGN #2 DESCRIPTION

Design #2 is a modification of design #1. This design allows a DRAM array up to 64 Mbytes. However, driving an array with greater capacitance than specified in the data sheet requires derating the $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ times. Smaller DRAM arrays can derate times by interpolating times in the DP8420A/21A/22A data sheet timing parameters.

This design differs from design #1 in that a latch was added to produce $\overline{ADS}$ and $\overline{AREQ}$. This latch asserts $\overline{ADS}$ and $\overline{AREQ}$ at the beginning of the 68020 "S2" clock. This latch was added to increase the time from $\overline{ADS}$ asserted to CLK ($400b), $\overline{CS}$ setup to $\overline{ADS}$ asserted ($401) and $\overline{ADS}$ negated held from CLK high ($405). The DP8420/21/22 is operated in Mode 1. An access cycle begins when the 68020 places a valid address on the address bus and asserts $\overline{ADS}$. If the address is in the address space of the DRAM, the 74AS138 decoder asserts $\overline{CS}$. During the next positive clock level, the latch is set which produces $\overline{ADS}$ and $\overline{AREQ}$. If a refresh or Port B access is not in progress, the DP8420A/21A/22A will assert the proper $\overline{RAS}$ depending on programming and the bank select inputs (B0, B1). After guaranteeing the programmed value of row address hold time, the DP8420A/21A/22A will switch the DRAM address (Q0–8, 9, 10) to the column address and assert $\overline{CAS}$. By this time the 74AS245s have been enabled and the DRAMs place their data on the data bus. The DP8420A/21A/22A also asserts $\overline{DTACK}$ which is used to generate $\overline{DSACK}$0,1 to the 68020. When the 68020 negates $\overline{AS}$, the latch is cleared and the access is terminated.

If a refresh or Port B access had been in progress, the DP8420A/21A/22A would have delayed the 68020 access by inserting wait states into the access cycle until the refresh was complete and the programmed amount of precharge was met. This circuit can run up to 20 MHz with 2 wait states. It is suggested that the least significant address bits be tied to the bank select inputs (B0, B1). This will reduce the chance of having to insert wait states to guarantee $\overline{RAS}$ precharge time. To keep the delays as specified in the data sheet, it is recommended that DELCLK is a multiple of 2 MHz.

DESIGN #2 TIMING AT 20 MHz AND 16.667 MHz

Clock Period = Tcp20 = 50 ns @ 20 MHz
= Tcp16 = 60 ns @ 16.667 MHz

$400b: $\overline{ADS}$ Asserted to CLK High
= Clock Period − 74AS04 Maxhl − 74AS02 Maxlh − 74AS02 Maxhl
= Tcp20 − Tphl Max − Tplh Max − Tphl Max
= 50 ns − 4 ns − 4.5 ns − 4.5 ns
= **37 ns @ 20 MHz**
= Tcp16 − Tphl Max − Tplh Max − Tphl Max
= 60 ns − 4 ns − 4.5 ns − 4.5 ns
= **47 ns @ 16.667 MHz**

$401: $\overline{CS}$ Setup to $\overline{ADS}$ Asserted
= Clock Period + 74AS04 Minhl + 74AS02 Minlh + 74AS02 Minhl 68020 Clock to Address Max − 74AS138 Decoder Maxhl
= Tcp20 + Tphl Min + Tplh Min + Tphl Min − #6 Max − Tphl Max
= 50 ns + 1 ns + 1 ns + 1 ns − 25 ns − 9 ns
= **19 ns @ 20 MHz**
= Tcp16 + Tphl Min + Tplh Min + Tphl Min − #6 Max − Tphl Max
= 60 ns + 1 ns + 1 ns − 30 ns − 9 ns
= **24 ns @ 16.667 MHz**

$404 & $407: Address Setup to $\overline{ADS}$ Asserted
= Clock Period + 74AS04 Minhl + 74AS02 Minlh + 74AS02 Minhl 68020 Clock to Address Max
= Tcp20 + Tphl Min + Tplh Min + Tphl Min − #6 Max
= 50 ns + 1 ns + 1 ns + 1 ns − 25 ns
= **28 ns @ 20 MHz**
= Tcp16 + Tphl Min + Tplh Min + Tphl Min − #6 Max
= 60 ns + 1 ns + 1 ns + 1 ns − 30 ns
= **33 ns @ 16.667 MHz**

$405: $\overline{ADS}$ Negated Held from CLK High
= 74AS04 Minhl + 74AS02 Minlh + 74AS02 Minhl
= Tphl Min + Tplh Min + Tphl Min
= 1 ns + 1 ns + 1 ns
= **3 ns @ 20 MHz**
= Tphl Min + Tplh Min + Tphl Min
= 1 ns + 1 ns + 1 ns
= **3 ns @ 16.667 MHz**

#47A: $\overline{DSACK}$0,1 Setup Time
= ½ Clock Period − Max 74AS74 Delay − Max 74AS32 Delay ½ Tcp20 − Tphl Max − Tphl Max
= 25 ns − 9 ns − 5 ns
= **11 ns @ 20 MHz**
= ½ Tcp16 − Tphl Max − Tphl Max
= 30 ns − 9 ns − 5 ns
= **16 ns @ 16.667 MHz**

#47B: $\overline{DSACK}$0,1 Hold Time
= ½ Clock Period + Min 74AS74 Delay + Min 74AS32 Delay
= ½ Tcp20 + Tphl Min + Tphl Min
= 25 ns + 5 ns + 1 ns
= **31 ns @ 20 MHz**
= 30 ns − 5 ns − 1 ns
= **36 ns @ 16.667 MHz**

$\overline{RAS}$ Low during REFRESH

tRAS = Programmed Clocks
− [(CLK High to Refresh $\overline{RAS}$ Asserted)
− (CLK High to Refresh $\overline{RAS}$ Negated)]
= Tcp20 + Tcp20 + Tcp20
+ Tcp20 − $55
= 200 ns −6 ns

= 194 ns @ 20 MHz

= Tcp16 + Tcp16 − $55
= 120 ns − 6 ns

= 114 ns @ 16.667 MHz

$\overline{RAS}$ Precharge Parameters

$29b: $\overline{AREQ}$ Negated Setup to CLK High
= CLOCK Period − Max 74AS04 − Max 74AS02 − Max 74AS02 − Max 74AS02
= 50 ns − 5 ns − 4.5 ns − 4.5 ns − 4.5 ns

= 31.5 ns @ 20 MHz

=60 ns − 5 ns − 4.5 ns − 4.5 ns − 4.5 ns

= 41.5 ns @ 16.667 MHz

tRP = Programmed Clocks − Max 74AS04
− Max 74AS02 − Max 74AS02
− Max 74AS02 [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]
= 3 Tcp20 − Tphl − Tplh − Tphl
− Tplh − $50
= 150 ns − 4 ns − 4.5 ns − 4.5 ns
− 16 ns

= 116.5 ns @ 20 MHz

= 2 Tcp16 − Tphl − Tplh − Tphl
− Tplh − $50
= 120 ns − 4 ns − 4.5 ns − 4.5 ns
− 4.5 ns − $50

= 86.5 ns @ 16.667 MHz

*To gain more precharge @ 16.667 MHz program 3T precharge.

tRAC AND tCAC TIMING FOR DRAMs

Timing is supplied for the system shown in *Figure 4 (See Figures 5, 6)*. Since systems and DRAM times vary, the user is encouraged to change the following equations to match his system requirements. Timing has been supplied for systems with 1, 2 or 3 wait states. If the DELCLK is not a multiple of 2 MHz, the timing for tRAH and tASC will change. Because tRAH and tASC will change, $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also vary and must be changed according to the equations given in the data sheet. The $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also have to be changed depending on the capacitance of the DRAM array.

1 Wait State

tRAC = s2 + s3 + sw + sw + s4
− 74AS04 Maxhl − 74AS02 Maxlh
− 74AS02 Maxhl − 74AS245 Delay Max − 68020 Data Setup Min
− $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted
= ½ Tcp20 + Tcp20 + Tcp20 − Tphl Max
− Tplh Max − Tphl Max
− #27 Min − $402 Max
= 25 ns + 50 ns + 50 ns − 4 ns − 4.5 ns
− 4.5 ns − 7 ns − 5 ns − 35 ns

= 65 ns @ 20 MHz w/8420A-20 Heavy Load

= 75 ns @ 20 MHz w/8420A-25 Light Load

= ½ Tcp16 + Tcp16 + Tcp16 − Tphl Max
− Tplh Max − Tphl Max −
#27 Min − $402 Max
= 30 ns + 60 ns + 60 ns −4 ns − 4.5 ns
− 4.5 ns − 7 ns − 5 ns −35 ns

= 85 ns @ 16.667 MHz w/8420A-20 Heavy Load

= 95 ns @ 16.667 MHz w/8420A-25 Light Load

2 Wait States

tRAC = s2 + sw + sw + sw + sw + s3 + s4
− 74AS04 Maxhl − 74AS02 Maxlh
− 74AS02 Maxhl − 74AS245 Delay Max
− 68020 Data Setup Min
− $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted
= ½ Tcp20 + Tcp20 + Tcp20 + Tcp20
− Tphl Max − Tplh Max − Tphl Max
− #27 Min − $402 Max
= 25 ns + 50 ns + 50 ns + 50 ns
− 4 ns − 4.5 ns − 4.5 ns
− 7 ns − 5 ns − 35 ns

= 115 ns @ 20 MHz w/8420 − 20 Heavy Load

= 125 ns @ 20 MHz w/8420 − 25 Light Load

= ½ Tcp16 + Tcp16 + Tcp16 + Tcp16
− Tphl Max − Tplh Max − Tphl Max
− #27 Min − $402 Max
= 30 ns + 60 ns + 60 ns + 60 ns
− 4 ns − 4.5 ns − 4.5 ns
− 7 ns − 5 ns − 35 ns

= 150 ns @ 16.667 MHz w/8420 − 20 Heavy Load

= 160 ns @ 16.667 MHz w/8420 − 25 Light Load

3 Wait States

tRAC = s2 + sw + sw + sw + sw + sw + s3 + s4 + sw − 74AS04 Maxhl − 74AS02 Max − 74AS02 Maxhl − 74AS245 Max Delay − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted

= ½ Tcp20 + Tcp20 + Tcp20 + Tcp20 + Tcp20 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $402 Max

= 25 ns + 50 ns + 50 ns + 50 ns − 50 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 35 ns

= 165 ns @ 20 MHz w/8420 − 20 Heavy Load

= 175 ns @ 20 MHz w/8420 − 25 Light Load

= ½ Tcp16 + Tcp16 + Tcp16 + Tcp16 + Tcp16 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $402 Max

= 30 ns + 60 ns + 60 ns + 60 ns − 60 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 35 ns

= 210 ns @ 16.667 MHz w/8420 − 20 Heavy Load

= 220 ns @ 16.667 MHz w/8420 − 25 Light Load

1 Wait State

tCAC = s2 + s3 + sw + sw + s4 − 74AS04 Maxhl − 74AS04 Maxlh − 74AS02 Maxhl − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= ½ Tcp20 + Tcp20 + Tcp20 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $403a Max

= 25 ns + 50 ns + 50 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 94 ns

= 6 ns @ 20 MHz w/8420 − 20 Heavy Load

= 35 ns @ 20 MHz w/8420 − 25 Light Load

= ½ Tcp16 + Tcp16 + Tcp16 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $403a Max

= 30 ns + 60 ns + 60 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 94 ns

= 26 ns @ 16.667 MHz w/8420 − 20 Heavy Load

= 55 ns @ 16.667 MHz w/8420 − 25 Light Load

2 Wait States

tCAC = s2 + sw + sw + sw + sw + s3 + s4 + 74AS04 Maxhl − 74AS04 Maxlh − 74AS02 Maxhl − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= ½ Tcp20 + Tcp20 + Tcp20 + Tcp20 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $403a Max

= 25 ns + 50 ns + 50 ns + 50 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 94 ns

= 56 ns @ 20 MHz w/8420 − 20 Heavy Load

= 85 ns @ 20 MHz w/8420 − 25 Light Load

= ½ Tcp16 + Tcp16 + Tcp16 + Tcp16 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $403a Max

= 30 ns + 60 ns + 60 ns + 60 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 94 ns

= 91 ns @ 16.667 MHz w/8420 − 20 Heavy Load

= 120 ns @ 16.667 MHz w/8420 − 25 Light Load

3 Wait States

tCAC = s2 + sw + sw + sw + sw + sw + s3 + s4 + sw − 74AS04 Maxhl − 74AS02 Max − 74AS02 Maxhl − 74AS245 Max Delay − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= ½ Tcp20 + Tcp20 + Tcp20 + Tcp20 + Tcp20 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $403a Max

= 25 ns + 50 ns + 50 ns + 50 ns − 50 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 94 ns

= 106 ns @ 20 MHz w/8420 − 20 Heavy Load

= 135 ns @ 20 MHz w/8420 − 25 Light Load

= ½ Tcp16 + Tcp16 + Tcp16 + Tcp16 + Tcp16 − Tphl Max − Tplh Max − Tphl Max − #27 Min − $403a Max

= 30 ns + 60 ns + 60 ns + 60 ns − 60 ns − 4 ns − 4.5 ns − 4.5 ns − 7 ns − 5 ns − 94 ns

= 151 ns @ 16.667 MHz w/8420 − 20 Heavy Load

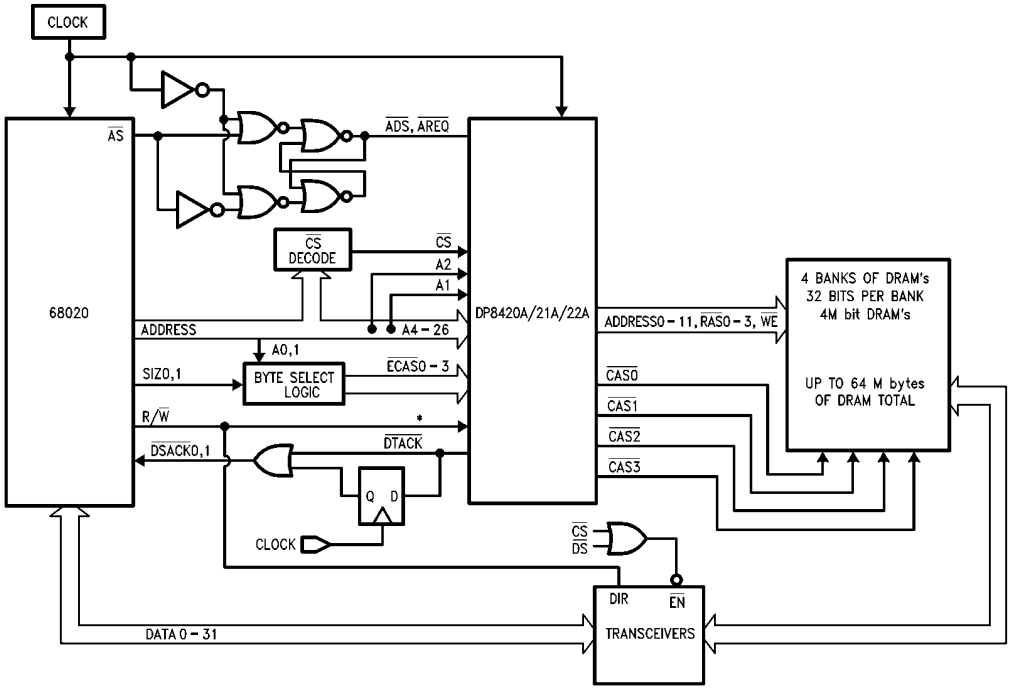
= 180 ns @ 16.667 MHz w/8420 − 25 Light Load

Programming Bits for Design #2

Bits	Description	Value
R0, R1	$\overline{RAS}$ Low during REFRESH $\overline{RAS}$ Precharge Time	R0 = s R1 = s
R2, R3	$\overline{DTACK}$ Generation Modes for Non-Burst (1T after $\overline{RAS}$)	R2 = 1 R3 = 0
R4, R5	$\overline{DTACK}$ during Burst Mode	R4 = x R5 = x
R6	Add Wait States with WAITIN	R6 = 0
R7	$\overline{DTACK}$ Mode Selected	R7 = 1
R8	Non-Interleaved Mode	R8 = 1
R9	Staggered or All REFRESH	R9 = u
C0, C1, C2	Divisor for DELCLK	C0 = s C1 = s C2 = s
C3	+30 Fine Tune	C3 = s
C4, C5, C6	$\overline{RAS}$, $\overline{CAS}$ Configuration Mode *Choose an All CAS Mode	C4 = u C5 = u C6 = u
C7	Select 0 ns Column Address Setup	C7 = 1
C8	Select 15 ns Row Address Hold	C8 = 1
C9	CAS is Delayed to Next Rising CLOCK Edge during Writes	C9 = 1
B0	The Row/Column Bank Latches are in Fall Through Mode	B0 = 1
B1	Access Mode 1	B1 = 1
$\overline{ECAS}$0	$\overline{CAS}$ not extended beyond $\overline{RAS}$	$\overline{ECAS}$0 = 0

x = don't care
u = user defined
s = system dependent

s @ 16.667 MHz		s @ 20 MHz	
R0 = 0	C0 = 0	R0 = 1	C0 = 0
R1 = 1	C1 = 1	R1 = 1	C1 = 0
	C2 = 0		C2 = 0
	C3 = 0		C3 = 0



TL/F/9733–4

*For higher clock frequencies, the $\overline{ADS}$ input and the R/$\overline{W}$ line from the 68020 should be connected logically by an OR gate for input to the $\overline{WIN}$ input on the DP8420A/21A/22A to avoid a late write during a read access.

FIGURE 4. 68020 Design #2

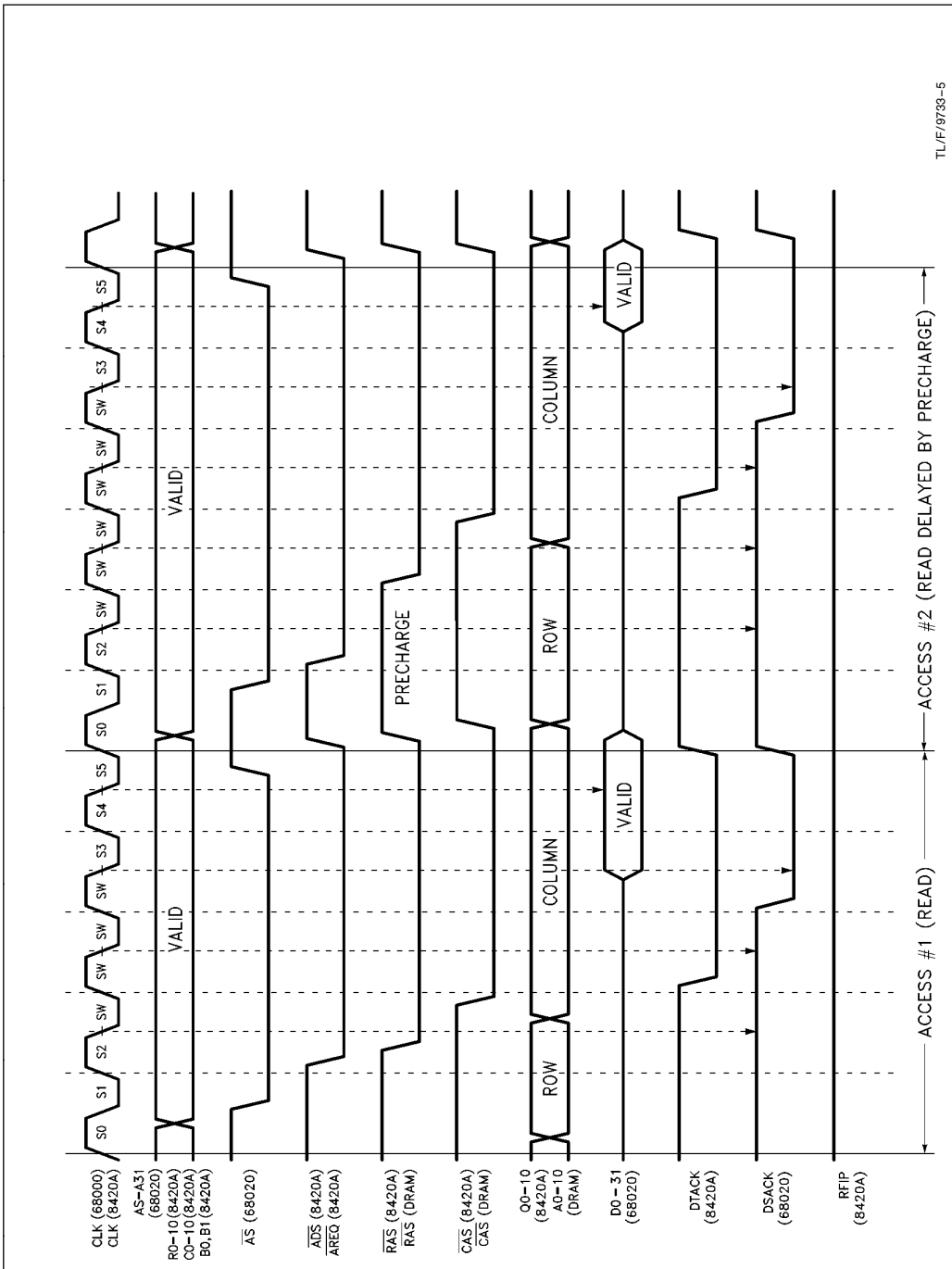


FIGURE 5. 68020 Design #2 Timing

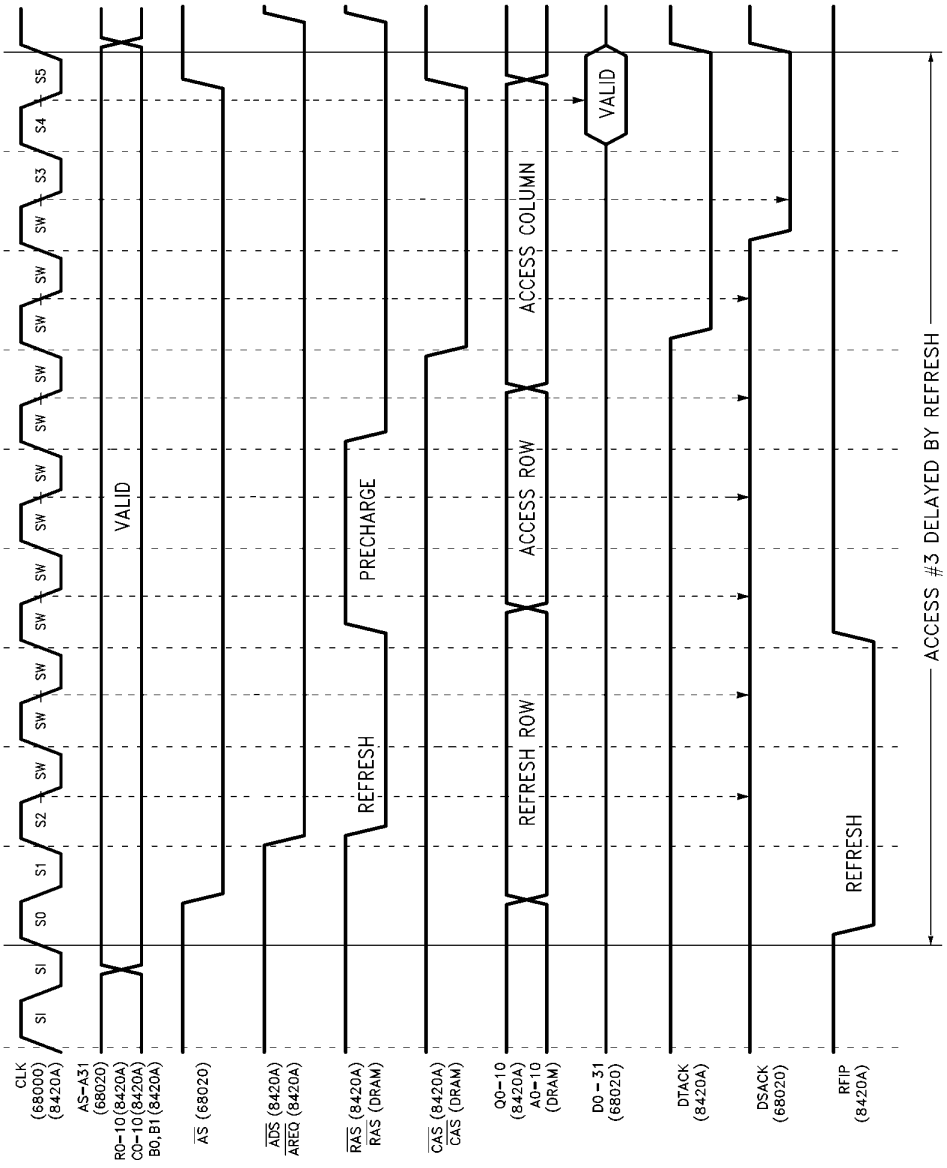


FIGURE 6. 68020 Design #2 Timing

DESIGN #3 DESCRIPTION

Design #3 uses two 68020s sharing a common DRAM array. Port A's interface is the same as design #1.

The two processors share the same CLK. By using the same CLK, the request from Port B do not have to be synchronized to the system CLK.

In this design, an access begins from Port A when the 68020 asserts $\overline{AS}$. Assuming the DP8422 has granted access to Port A through GRANTB negated, $\overline{AS}$ will assert $\overline{RAS}$. After guaranteeing the programmed value of tRAH, the DP8422 will switch the Q outputs to the column address tASC before asserting $\overline{CAS}$. By this time the 74AS245s have been enabled and the DRAM places its data on the data bus. The cycle is terminated by the DP8422 asserting $\overline{DTACK}$. The 68020 will then sample the data from the data bus and negate $\overline{AREQ}$. $\overline{AREQ}$ negated will cause $\overline{RAS}$ to be negated.

If at any time during Port A's access Port B had requested an access by asserting $\overline{AREQB}$, Port B's 68020 would have been delayed by keeping $\overline{ATACKB}$ negated. This would have inserted wait states into Port B's access. After Port A's access terminates, GRANTB is asserted to allow Port B's address through the mux. On the next rising CLOCK edge, $\overline{RAS}$ will be asserted. Again, after guaranteeing the necessary address parameters, $\overline{CAS}$ will be asserted.

Refresh will happen after the current access is completed and precharge time has been met. During this refresh, all accesses will be held off.

Since back-to-back accesses can cause precharge delays, it is recommended that the low order address bits be tied to the bank select inputs.

DESIGN #3 TIMING DESCRIPTION

Clock Period = Tcp16 = 65 ns @ 16 MHz
= Tcp12 = 83 ns @ 12 MHz

Port A Timing

$400b: $\overline{ADS}$ Asserted Setup to CLK High
= Clock Period − 68020 Clock to $\overline{AS}$ Low Max
= Tcp16 − #9 Max
= 62.5 ns − 30 ns
= **32.5 ns @ 16 MHz**
= Tcp12 − #9 Max
= 83 ns − 40 ns
= **43 ns @ 12 MHz**

$401: $\overline{CS}$ Setup to $\overline{ADS}$ Asserted
= 68020 $\overline{AS}$ Address to $\overline{AS}$ Max + 74AS244 Min − 74AS138 Decoder Max
= #11 Max + Tphl Min + Tphl Max
= 15 ns + 2 ns − 9 ns
= **8 ns @ 16 MHz**
= #11 Max + Tphl Min + Tphl Max
= 20 ns + 2 ns − 9 ns
= **13 ns @ 12 MHz**

$404 & 407: Address Valid Setup to $\overline{ADS}$ Asserted
= 68020 Address to $\overline{AS}$ + Min 74AS244 − Max 74AS244
= #11 Max + Tphl Min + Tphl Max
= 15 ns + 2 ns − 6 ns
= **11 ns @ 16 MHz**
= #11 Max + Tphl Min − Tphl Max
= 20 ns + 2 ns − 6 ns
= **16 ns @ 12 MHz**

$405: $\overline{ADS}$ Negated Held from CLK
= 68020 Min CLOCK to $\overline{AS}$
= #9 Min
= 3 ns
= **3 ns @ 16 MHz**
= #9 Min + Tphl Min
= 3 ns + 2 ns
= **3 ns @ 12 MHz**

#47A: $\overline{DSACK}$0,1 Setup Time
= ½ CLOCK Period − 74AS74 Delay Max − 74AS32 Delay Max
= ½ Tcp16 − Tphl Max − Tphl Max
= 31 ns − 9 ns − 5 ns
= **18 ns @ 16 MHz**

* Requires External Flip-Flop and OR Gate.

= ½ CLOCK Period − CLK to $\overline{DTACK}$ Asserted
= ½ Tcp − $18 Max
= 41 ns − 33 ns
= **8 ns @ 12 MHz**

*Program as DTACK of 1½ No External Flip-Flop Required.

#47B: $\overline{DSACK}$0,1 Hold Time
= ½ Clock Period + Min 74AS74 + Min 74AS32
= ½ Tcp16 + Tphl Min + Tphl Min
= 31 ns + 5 ns + 1 ns
= **37 ns @ 16 MHz**

*Requires External Flip Flop and OR Gate.

= ½ CLOCK Period + Min CLK to $\overline{DTACK}$ Asserted
= 41 ns + 0 ns
= **41 ns @ 12 MHz**

*Program as $\overline{DTACK}$ of 1½.

#450 & $454: Address Setup to CLK High
= CLOCK Period − CLK High to GRANTB Negated − 74AS04 Delay Max − 74AS00 Delay Max − 74AS00 Delay Max − 74AS244 Delay
= Tcp16 − $109 Max − Tplh − Tphl − Tphl − Tzh
= 62.5 ns − 26 ns − 5 ns − 4.5 ns − 4.5 ns − 9 ns

= 13.5 ns @ 16 MHz

= tcp12 − $109 Max − Tplh − Tphl − Tphl − Tzh
= 83 ns − 32 ns − 5 ns − 4.5 ns − 4.5 ns − 9 ns

= 34 ns @ 12 MHz

Port B Timing

$100: $\overline{\text{AREQB}}$ Held Negated from CLK High
= CLK to $\overline{\text{AS}}$ Min + 74AS32 Min
= #9 Min + Tphl Min
= 3 ns + 2 ns

= 5 ns @ 16 MHz

= #9 Min + Tphl Min
= 3 ns + 2 ns

= 5 ns @ 12 MHz

$101: $\overline{\text{AREQB}}$ Asserted Setup to CLK High
= Clock Period − CLK to $\overline{\text{AS}}$ Max − 74AS32 Max
= Tcp16 − #9 Max − Tphl Max
= 62.5 ns − 30 ns − 6 ns

= 26.5 ns @ 16 MHz

= Tcp12 − #9 Max − Tphl Max
= 83 ns − 40 ns − 6 ns

= 37 ns @ 12 MHz

$110: Row Address Setup to CLK High
= CLOCK Period − CLK High to GRANTB Asserted − 74AS04 Delay Max − 74AS00 Delay Max − 74AS244 Delay
= Tcp16 − $108 − Tplh − Tphl − Tzh
= 60 ns − 30 ns − 5 ns − 4.5 ns − 9 ns

= 11.5 ns @ 16 MHz

= Tcp12 − $108 − Tplh − Tphl − Tzh
= 80 ns − 30 ns − 5 ns − 4.5 ns − 9 ns

= 31.5 ns @ 20 MHz

$114: Address Valid Setup to $\overline{\text{AREQB}}$ Asserted
= Min Address to $\overline{\text{AS}}$ − 74AS244 Max + 74AS244 Min + 74AS32 Min
= #11 − Tphl Max + Tphl Min + Tphl Min
= 15 ns − 6 ns + 2 ns + 2 ns

= 13 ns @ 16 MHz

= #11 − Tphl Max + Tphl Min + Tphl Min
= 20 ns − 6 ns + 2 ns + 2 ns

= 18 ns @ 12 MHz

$117: $\overline{\text{AREQ}}$ Negated Pulse Width
= $\overline{\text{AS}}$ Negated Width
= #15 Min

= 40 ns @ 16 MHz

= #15 Min

= 50 ns @ 12 MHz

#47a $\overline{\text{DSACK}}$0,1 Setup Time
= ½ CLOCK Period − Max 74AS74 − Max 74AS32
= ½ Tcp16 + Min Tphl + Min Tphl
= 31 ns − 9 ns − 5 ns

= 17 ns @ 16 MHz

= ½ Tcp12 − Tphl Max − Tphl Max
= 41 ns − 9 ns − 5 ns

= 27 ns @ 12 MHz

#47B $\overline{\text{DSACK}}$0,1 Hold Time
= ½ CLOCK Period + Min 74AS74 + Min 74AS32
= ½ Tcp16 + Min Tphl + Min Tphl
= 31 ns + 5 ns + 1 ns

= 37 ns @ 16 MHz

= ½ Tcp12 + Min Tphl + Min Tphl
= 41 ns + 5 ns + 1 ns

= 47 ns @ 12 MHz

$\overline{\text{RAS}}$ Low during REFRESH

tRAS = Programmed CLOCKs − [(CLK High to Refresh $\overline{\text{RAS}}$ Asserted) − (CLK High to Refresh $\overline{\text{RAS}}$ Negated)]
= Tcp16 + Tcp16 − $55
= 62.5 ns + 62.5 ns −6 ns

= 119 ns @ 16 MHz

= Tcp12 + Tcp12 − $55
= 83.3 ns +83.3 ns − 6 ns

= 160 ns @ 12 MHz

$\overline{\text{RAS}}$ Precharge Parameters

$29b: $\overline{\text{AREQ}}$ Negated Setup to CLK High
= CLOCK Period − CLOCK Low to $\overline{\text{AS}}$ Negated
= 62.5 ns − 30 ns

= 32 ns @ 16 MHz

= Tcp12 − #12
= 83 ns − 40 ns

= 43 ns @ 12 MHz

tRP = ss + s0 + s1 + s2 − 68020 CLK Low to $\overline{AS}$ Asserted − [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]

= 2 Tcp16 − # 12 − $50

= 125 ns − 30 ns − 16 ns

= **79 ns @ 16 MHz** w/8420A-20

= **81 ns @ 16 MHz** w/8420A-25

= 2 Tcp12 − #12 − $50

= 166 ns − 30 ns − 16 ns

= **120 ns @ 12 MHz**

tRAC AND tCAC TIMING FOR DRAMs

Timing is supplied for the system shown in *Figure 7 (See Figure 8)*. Since systems and DRAM times vary, the user is encouraged to change the following equations to match his system requirements. Timing has been supplied for systems with 1 or 2 wait states. If DELCLK is not a multiple of 2 MHz, the timing for tRAH and tASC will change and must be calculated and changed according to the equations in the DP8420A/21A/22A data sheet.

Port A

1 Wait State

tRAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl − Tphl − #27 Min − $402 Max

= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 6.2 ns − 7 ns − 5 ns − 29 ns

= **110 ns @ 16 MHz** w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12

= #9 Max − Tphl − Tphl − #27 Min − $402 Max

= 83.3 ns + 83.3 ns + 83.3 ns − 40 ns − 6.2 ns − 7 ns − 10 ns −35 ns

= **163 ns @ 12 MHz** w/8420A-20 Heavy Load

2 Wait States

tRAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl − Tphl #27 Min − $402 Max

= 62.5 ns + 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 6.2 ns − 7 ns −5 ns − 29 ns

= **172.8 ns @ 16 MHz** w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl − Tphl − #27 Min − $402 Max

= 83.3 ns + 83.3 ns + 83.3 ns + 83.3 ns − 40 ns − 6.2 ns −7 ns − 10 ns −35 ns

= **240 ns @ 12 MHz** w/8420A-20 Heavy Load

Port B

1 Wait State

tRAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS32 Delay Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{AREQB}$ Asserted to $\overline{RAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl Max − Tphl Max − Tphl Max − #27 Min − $102 Max

= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 6.2 ns − 5 ns − 7 ns − 5 ns − 34 ns

= **110 ns @ 16 MHz** w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl Max − Tphl Max − Tphl Max − #27 Min − $102 Max

= 83.3 ns + 83.3 ns + 83.3 ns − 40 ns − 6.2 ns − 5 ns − 7 ns − 10 ns − 42 ns

= **139 ns @ 12 MHz** w/8420A-20 Heavy Load

2 Wait States

tRAC = s1 + s2 + sw + sw + sw + sw − 68020 CLK to $\overline{AS}$ Max − 74AS32 Delay Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{AREQB}$ Asserted to $\overline{RAS}$ Aserted

= Tcp16 + Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl Max − Tphl Max − #27 Min − $102 Max

= 62.5 ns + 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 6.2 ns − 5 ns − 7 ns − 5 ns − 34 ns

= **167 ns @ 16 MHz** w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl Max − Tphl Max − Tphl Max − #27 Min − $102 Max

= 83.3 ns + 83.3 ns + 83.3 ns + 83.3 ns −40 ns − 6.2 ns − 5 ns − 7 ns − 10 ns −42 ns

= **223 ns @ 12 MHz** w/8420A-20 Heavy Load

Port A

1 Wait State

tCAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl − Tphl − #27 Min − $403a Max

= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 6.2 ns − 7 ns −5 ns − 82 ns

= 57 ns @ 16 MHz w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 = #9 Max − Tphl − Tphl − #27 Min − $403a Max

= 83.3 ns + 83.3 ns + 83.3 ns −40 ns − 6.2 ns − 7 ns − 10 ns − 94 ns

= 92 ns @ 12 MHz w/8420A-20 Heavy Load

2 Wait States

tCAC = s1 + S2 + sw + sw + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl − Tphl − #27 Min − $403a Max

= 62.5 ns + 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 6.2 ns − 7 ns − 5 ns − 82 ns

= 119 ns @ 16 MHz w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl − Tphl − #27 Min − $403a Max

= 83.3 ns + 83.3 ns + 83.3 ns + 83.3 ns − 40 ns − 6.2 ns − 5 ns − 7 ns − 10 ns − 94 ns

= 171 ns @ 12 MHz w/8420A-20 Heavy Load

Port B

1 Wait State

tCAC = s1 + s2 + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS32 Delay Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl − Tphl − Tphl − #27 Min − $118

= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 5 ns − 6.2 ns − 7 ns −5 ns − 88 ns

= 46 ns @ 16 MHz w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 = #9 Max − Tphl − Tphl − Tphl − #27 Min − $118a

= 83.3 ns + 83.3 ns + 83.3 ns −40 ns − 5 ns − 6.2 ns − 7 ns − 10 ns − 103 ns

= 78 ns @ 12 MHz w/8420A-20 Heavy Load

2 Wait States

tCAC = s1 + s2 + sw + sw + sw + sw + s3 + s4 − 68020 CLK to $\overline{AS}$ Max − 74AS32 Delay Max − 74AS244 Delay Max − 74AS245 Delay Max − 68020 Data Setup Min − $\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted

= Tcp16 + Tcp16 + Tcp16 + Tcp16 − #9 Max − Tphl − Tphl − Tphl − #27 Min − $118a Max

= 62.5 ns + 62.5 ns + 62.5 ns − 30 ns − 5 ns − 6.2 ns − 5 ns − 7 ns − 5 ns − 84 ns

= 109 ns @ 16 MHz w/8420A-25 Heavy Load

= Tcp12 + Tcp12 + Tcp12 + Tcp12 − #9 Max − Tphl − Tphl − Tphl − #27 Min − $118 Max

= 83.3 ns + 83.3 ns + 83.3 ns + 83.3 ns − 40 ns − 5 ns − 6.2 ns − 7 ns − 10 ns − 103 ns

= 162 ns @ 12 MHz w/8420A-20 Heavy Load

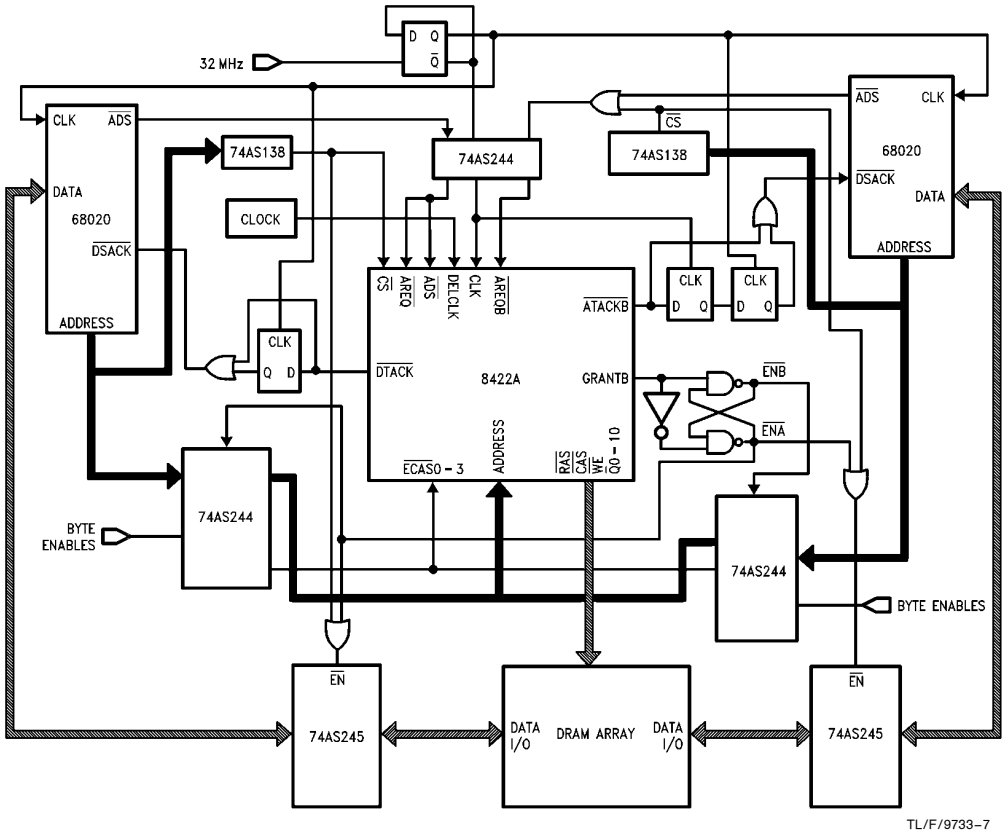


FIGURE 7. 68020 Dual Port System up to 16 MHz

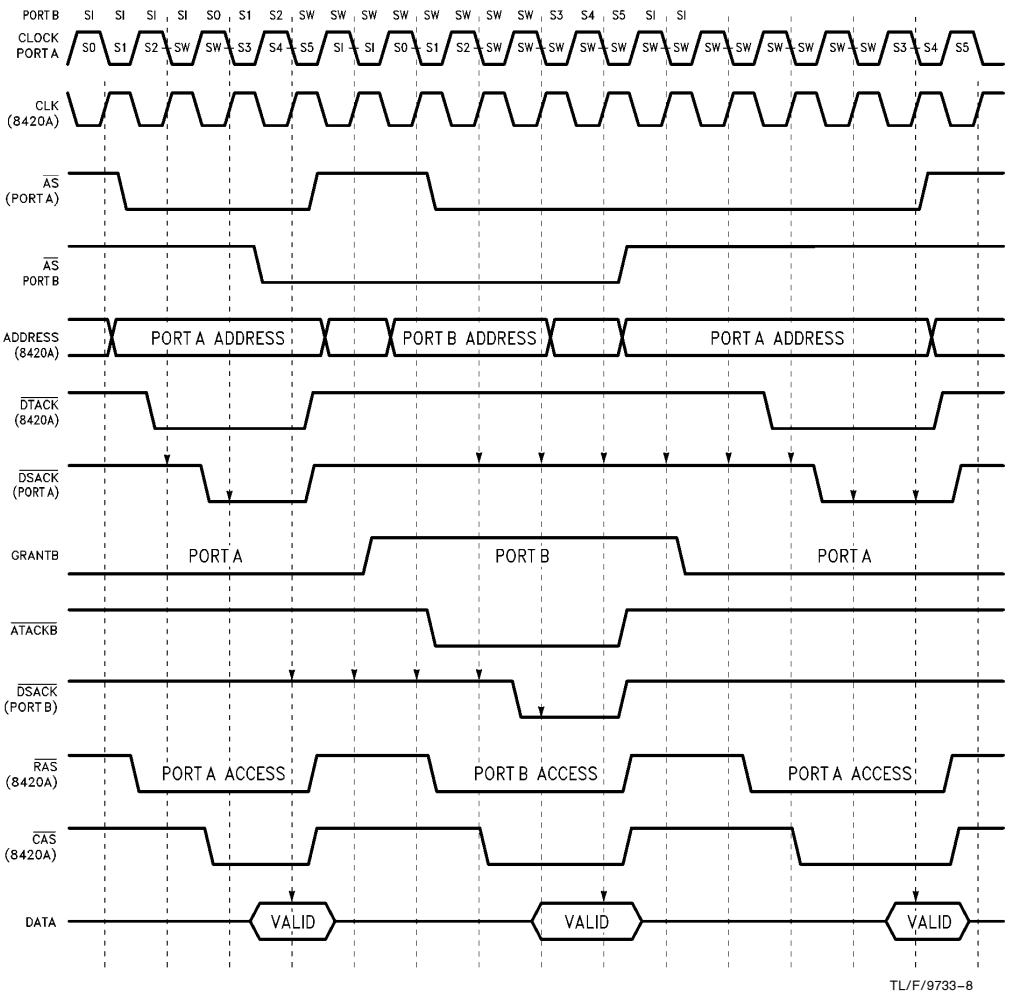
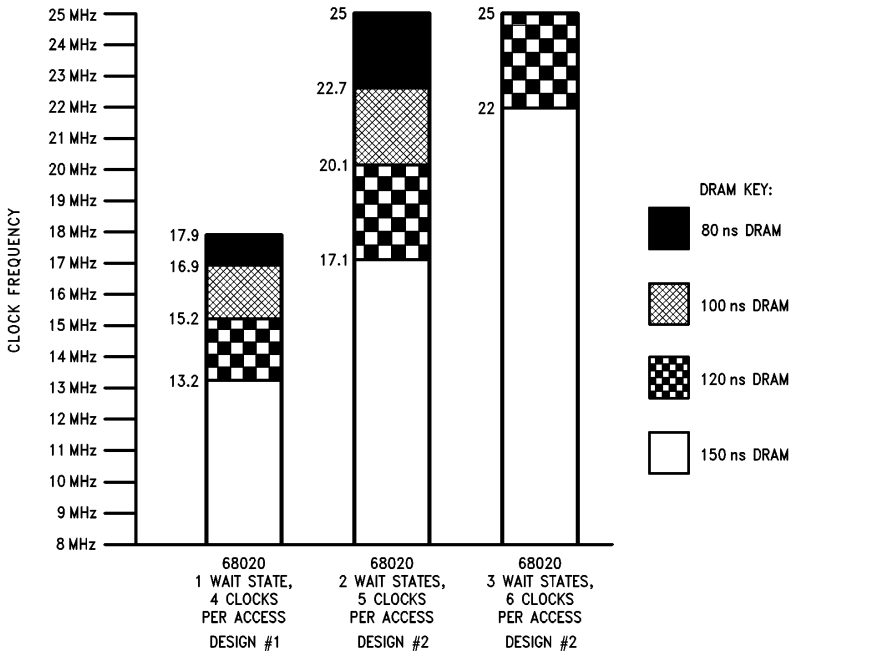


FIGURE 8. 68020 Design #3 Timing, Delayed Dual Port Accesses

DRAM Speed Versus Processor Speed. (DRAM Speed References the RAS Access Time, t_{RAC}, of the DRAM, Using DP8422A-25 Timing Specifications.)



TL/F/9733–9

Lit. # 100539

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408