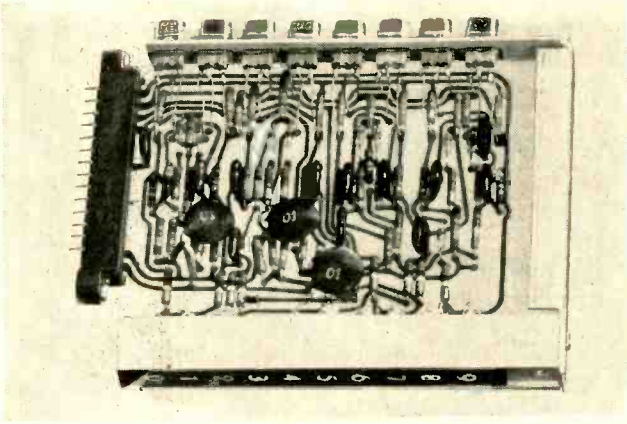

Printed-circuit techniques permit compact packaging of counter

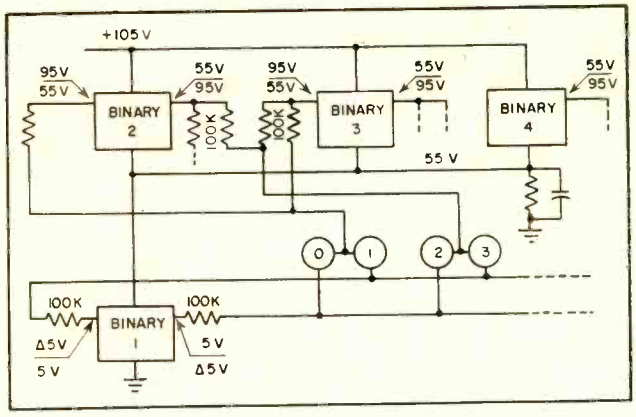

FIG. 1—Indicator system for counter uses NE-2A neon lamps

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HIGH-RELIABILITY Transistorized Counter

SUMMARY —— Cascaded silicon-junction transistor binary stages energize neon-lamp indicators for digital frequency meter at counting rates up to 100,000 per second. Step-by-step calculations are shown for design of binary stages. Counter has logged 14,600 hours of continuous operation with no component failures or waveform deterioration

TRANSISTOR COUNTING CIRCUITS are readily designed, but systems for count indication have led to considerable complexity. However, owing to the unique transistor characteristic of minute saturation resistance evident in switching applications, it is practical to cascade binary circuits to obtain a decade counter. Such a system, as described in this article, provides potentials sufficient to reliably operate neon lamps by direct near-conventional methods.

Readout Indicators

Experience has shown that long-term repeated operation of the NE-2A neon lamp requires ionization potentials of at least 85 v and extinguishing potentials must be less than 55 v. For a decade counter, it is possible to operate the lamps with an effective 50-v bias and a superposed 40-v swing.

The basic counter is shown in Fig. 1. Input is at binary 1, which triggers binary 2 once for every two input pulses. In turn, binary 2 triggers binary 3 once for every two of its own input pulses and similarly, binary 3 triggers binary 4.

The resistor matrix for only four lamps is shown to simplify the illustration. The matrix terminations at the blocks are, by implication, directed to the left and right-hand collectors of the two transistors composing each binary. The upper voltage indicates d-c collector potential at zero count, while the lower voltage indicates the potential of the second stable state of the binary. The output voltage of each binary swings 40 v. The neon lamps are operated at 0.2 ma by potentials which vary at both of their terminations.

Binary 1 operates to select the odd or even numbered lamp, while the other binaries select pairs of lamps through the resistor matrix. The system can best be understood by considering the situation at zero count.

Binary 1 applies a five-volt potential to the even-numbered lamps and a 45-v potential to the odd-numbered lamps. The potential at

the junction between pairs of lamps is an average of the potential existing at the binary ends of the resistors. The resistors connecting the zero-one lamp pair are each terminated at potentials of 95 v. Therefore, before ionization occurs the zero lamp has 90 v applied and the one lamp has 50 v applied; the zero lamp will ionize while the one lamp cannot.

Current flow through the zero lamp is limited by the series resistors. The resistor matrix is arranged such that for the indicated voltages, a 90-v potential cannot exist across any of the other lamps.

A single pulse input to the counter triggers binary 1 to its second stable state and reverses the potentials applied to the even and odd-numbered lamps. The zero lamp is extinguished while the one lamp is ionized. Succeeding pulses cause the binaries to assume combinations of steady state voltages which ionize the lamp corresponding to the count stored in the decade counter.

Transistor Requirements

As the counting rate expressed as a frequency is 100 kc, it is desirable to have pulse rise times on the order of 1 μsec. In order that the transistor not be a limiting factor, its alpha cut-off frequency must then be 2 or 3 mc.

High current gain is not necessary and, in fact, would require larger binary crossover resistances to limit base current. This would increase waveform decay time and limit maximum counting frequencies.

Operating temperatures include the range from −20 C to +50 C. The former requires that the selected transistor retain a practical value of large signal gain at the coldest temperature. The high temperature requires that transistor leakage current I_{co} not increase to a large value and cause loss in output amplitude. Such a loss would seriously affect the neon lamp operating potentials.

The requirements of high operating voltage and high alpha cut-off frequency are met by the type 903 silicon-junction transistor. Maximum rated voltage for this unit is 30 v, but the collector junction has a breakdown voltage in excess of 50 v.

Binary Design

Since the binaries are of the saturating type, it is particularly important to know the base current requirements for the conditions of lowest gain and poorest operating conditions. The 903 transistor has a beta range of 9 to 19. Of more significance in binary circuit design is the large signal gain, B, which varies for this type from 7.5 to approximately 17. For complete interchangeability of transistors the binary is required to function with all values of B; therefore, it was necessary to design with the lowest value.

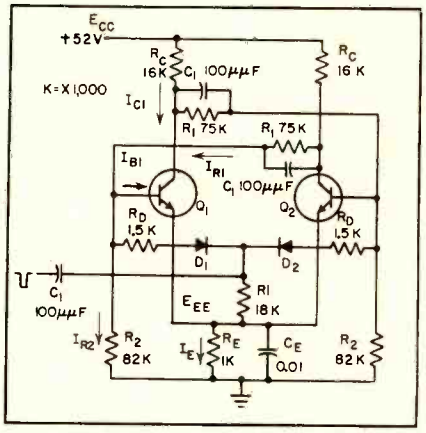

FIG. 2—Basic binary counter circuit

From the actual characteristic curves for many 903 transistors operated at −20 C, it was determined that the base current must be increased by 50 percent over the current value at 25 C to insure stability. Under this condition, a transistor with a B of 7.5 would saturate to a minor degree and transistors of higher gain would saturate in proportion to their large signal B.

Emperical data indicated that the transistors would exhibit a change in current gain of two to one over the specified temperature range. This data, when related to the normal two-to-one spread of beta, demanded that the binary circuit accommodate a total gain change of at least four to one.

The binary circuit is illustrated in Fig. 2. The design calculations are based on the following values: $V_o = 40$v; $E_{EE} = 3$v; $I_c = 2.5$ ma (assumed); $B = 7.5$ min.

The design procedure begins with a required output voltage, V_o, and establishes a supply voltage as the last step. Collector load $R_c = V_o/I_c = 16{,}000$ ohms.

Assuming transistor Q_1 on and Q_2 off: $I_{B1} = I_{C1}/B_{min} = 333$ μa at 25 C ambient. At −20 C, $I_{B1} = (333)\ (150\%) = 500$ μa.

Assuming $I_{R2} = 50$ μa, $I_{R1} = I_{B1} + I_{R2} = 550$ μa; $R_1 = V_o/I_{R1} \cong 75{,}000$ (assumes $V_{B1} = V_{C1}$ on); $R_2 = V_{B1}/I_{R2} = 4/50 \cong 82{,}000$ where $V_{B1} = E_{EE} + V_{CE}$ (sat) and V_{CE} at current saturation is 1 v. Neglecting minor leakage currents of the cut-off transistor: $I_E = I_{C1} + I_{B1} = 3.0$ ma; $R_E = E_{EE}/I_E = 1{,}000$ ohms and R_E is adequately bypassed when $C_E = 0.01$ μf.

Resistor R_2 establishes a reverse bias at the base of the transistor in a cut-off condition. Neglecting leakage currents, the reverse bias potential can be computed as follows: $V_{B2} = R_2\ (E_{EE} + V_{CE})/(R_1 + R_2) = 2.1$ v; reverse bias $= V_{B2} - E_{EE} = 2.1 - 3 = -0.9$v.

The supply voltage is computed as a summation of the common emitter level, the output voltage swing, and the product of the collector load and the base driving current. The crossover capacitances improve the rise time characteristics of the binary waveforms. Larger values sharpen the rise time, but also increase the time constant for the decay characteristic.

With $C_1 = 100$ $\mu\mu$f rise times on the order of 1 μsec were obtained with fall times of approximately 3 μsec.

Complete Circuit

The complete schematic of the decade counter is given in Fig. 3. The grouping of the four binaries is the same as that indicated in Fig. 1; the binaries are identical with only minor differences existing in their drive circuits. The resistors of the indicator lamp matrix shunt the 18-kilohm collector load resistors to an effective value of 16 kilohms.

The upper value of potential for each collector is for the zero count

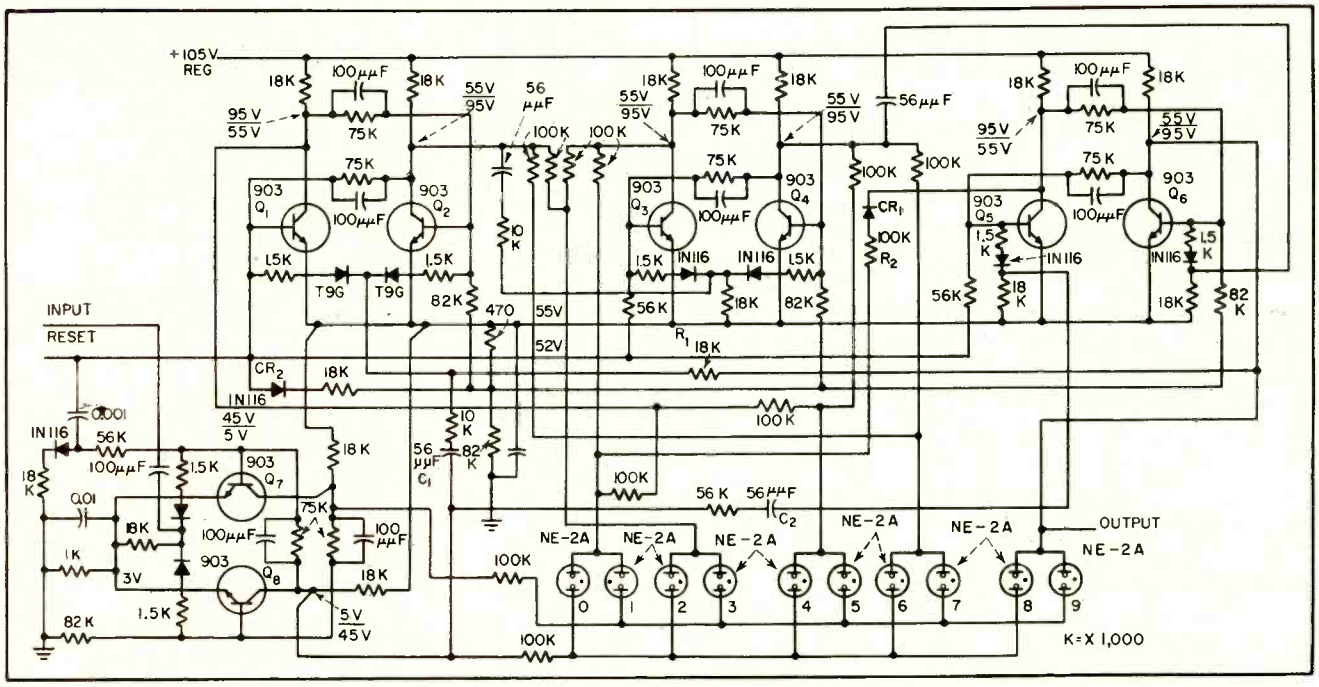

FIG. 3—Decade counter for digital frequency meter has four cascaded stages of two-transistor binary counters

state and the lower potential is the value to which the binary switches in proper sequence.

A basic four-binary counter scales to a count of 16. To scale to a count of 10, the counter is gated after the eighth input pulse and then, after the tenth pulse, returned to the zero count conditions. The first three binaries scale in a normal manner up to the eighth input pulse.

After the eighth input pulse binary 4 is triggered to its second stable state. The collector potential of transistor Q_6 rises to 95 v and is applied through R_1 to the juncture of the steering diodes in binary No. 2. The diodes are hereafter reverse biased by approximately 40 v and input pulses from binary 1 through coupling capacitor C_1 are effectively blocked. With these conditions, lamp 8 is ionized.

The ninth counter input triggers binary 1 and switches the ionizing potential from lamp 8 to lamp 9. The tenth input pulse resets binary 1 to its normal steady state. During this regenerative switching, a pulse is applied through capacitor C_2 to the base drive circuit of transistor Q_5 in the fourth binary, which returns to its normal steady state and completes the cycle of 10 counts. An output pulse may be taken from the fourth binary to drive a second decade counter which will then indicate the tens count.

D-C Gating

The d-c gating method of the counter is simple and reliable. The two steering diodes in binary 2 are special only in that their reverse impedance and breakdown voltage are sufficiently high to withstand the 40-v reverse bias.

Relatively large leakage current here is sufficient, under certain counting conditions, to trigger binary 2 and nullify the gating function. Silicon junction diodes at this circuit point are unsatisfactory because the diode-junction capacitance is large enough to transfer triggering pulses under certain operating conditions.

At zero count the even numbered transistors, or right-hand units, are in the on condition and lamp 0 is ionized. On count 8, the right-hand transistors of the first three binaries return to the on condition. Two high potentials now exist attempting to ionize lamps 0 and 8. Lamp 0 is prevented from ionizing by the application of a 55-v potential at transistor Q_5 through diode CR_1 and R_2 to the 0-1 lamp junction.

In addition, a current-limiting resistor is omitted in the path from the collector of Q_6 to the 8-9 lamp junction. These two lamps then operate at a 300-μa current level, as limited by the matrix resistors connected to binary 1. The result is a rise in the potentials applied to the lower side of the odd and even numbered lamps and an assist in preventing lamp 0 from ionizing.

Reset

The reset circuit is composed of two networks performing identical functions. The desired condition at reset is 0 count in which the right-hand transistors are conducting. This is accomplished by application of a pulse which will switch-off the left-hand transistors should they happen to be conducting. In the base return circuit corresponding to R_2 of the computations, a diode is inserted.

A negative pulse applied to the anode of the diode drives the transistor to a nonconducting state. The base return resistors of binaries 2, 3 and 4 are returned together through common diode CR_2 to the common bias potential. The reset pulse must be of 50-v amplitude and 40-μsec duration.

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